FAIRCHILD
SEMICONDUCTOR ™

August 1986
Revised April 2000

DM74S138 • DM74S139
Decoder/Demultiplexer

General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The DM74S138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-LOW and one active-HIGH enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The DM74S139 comprises two separate two-line-to-four-line decoders in a single package. The active-LOW enable input can be used as a data line in demultiplexing applications.

All of these decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.
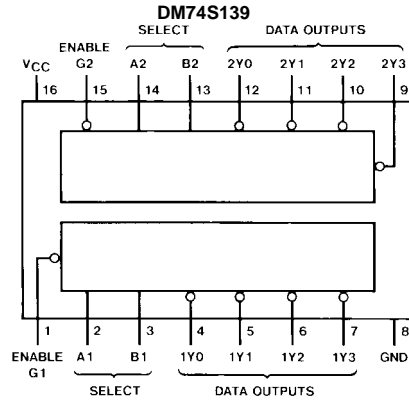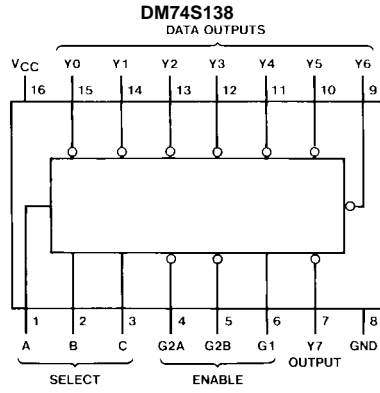
Features

■ Designed specifically for high speed:
  Memory decoders
  Data transmission systems
■ DM74S138 3-to-8-line decoders incorporates 3 enable inputs to simplify cascading and/or data reception
■ DM74S139 contains two fully independent 2-to-4-line decoders/demultiplexers
■ Schottky clamped for high performance
■ Typical propagation delay time (3 levels of logic)
  DM74S138   8 ns
  DM74S139   7.5 ns
■ Typical power dissipation
  DM74S138   245 mW
  DM74S139   300 mW

Ordering Code:

| Order Number	Package Number	Package Description
DM74S138N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
DM74S139N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Connection Diagrams

DM74S138

DATA OUTPUTS

V_{CC}	Y0	Y1	Y2	Y3	Y4	Y5	Y6
16	15	14	13	12	11	10	9

1	2	3	4	5	6	7	8
A	B	C	G2A	G2B	G1	Y7	GND

SELECT ENABLE OUTPUT

DM74S139

ENABLE SELECT DATA OUTPUTS

V_{CC}	G2	A2	B2	2Y0	2Y1	2Y2	2Y3
16	15	14	13	12	11	10	9

1	2	3	4	5	6	7	8
ENABLE G1	A1	B1	1Y0	1Y1	1Y2	1Y3	GND

SELECT DATA OUTPUTS

Function Tables

DM74S138

Inputs					Outputs							
Enable		Select										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

DM74S139

Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

* G2 = G2A + G2B
H = HIGH level
L = LOW level
X = don't care (either LOW or HIGH logic level)

Logic Diagrams

DM74S138

DM74S139
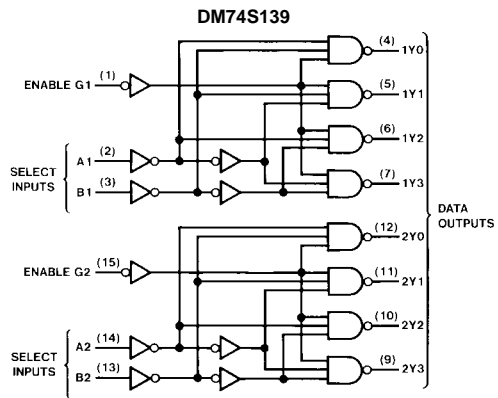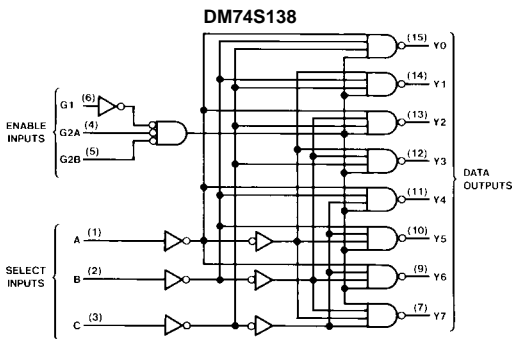
Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0° C to +70°C
Storage Temperature Range	−65° C to +150° C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−1	mA
I_{OL}	LOW Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			50	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.5V			−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−40		−100	mA
I_{CC}	Supply Current (DM74S138)	V_{CC} = Max (Note 4)		49	74	mA
I_{CC}	Supply Current (DM74S139)	V_{CC} = Max (Note 4)		60	90	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

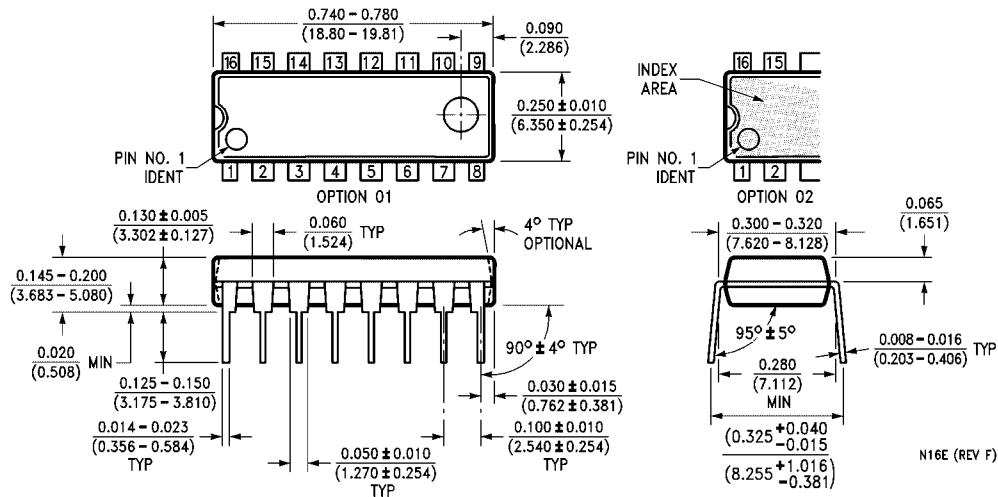**Note 4:** I_{CC} is measured with all outputs enabled and OPEN.

DM74S138 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	Levels of Delay	R_L = 280Ω				Units
				C_L = 15 pF		C_L = 50 pF		
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Select to Output	2		7		9	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Select to Output	2		10.5		14	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Select to Output	3		12		14	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Select to Output	3		12		15	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Enable to Output	2		8		10	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Enable to Output	2		11		14	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Enable to Output	3		11		13	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Enable to Output	3		11		14	ns

DM74S139 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	Levels of Delay	R_L = 280Ω				Units
				C_L = 15 pF		C_L = 50 pF		
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Select to Output	2		7.5		10	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Select to Output	2		10		13	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Select to Output	3		12		13	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Select to Output	3		12		15	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Enable to Output	2		8		10	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Enable to Output	2		10		13	ns

Physical Dimensions inches (millimeters) unless otherwise noted

0.740 – 0.780
(18.80 – 19.81)

0.090
(2.286)

0.250 ± 0.010
(6.350 ± 0.254)

PIN NO. 1 IDENT

OPTION 01

INDEX AREA

PIN NO. 1 IDENT

OPTION 02

0.130 ± 0.005
(3.302 ± 0.127)

0.060
(1.524) TYP

4° TYP OPTIONAL

0.145 – 0.200
(3.683 – 5.080)

0.020
(0.508) MIN

0.125 – 0.150
(3.175 – 3.810)

0.014 – 0.023
(0.356 – 0.584) TYP

0.050 ± 0.010
(1.270 ± 0.254) TYP

90° ± 4° TYP

0.030 ± 0.015
(0.762 ± 0.381)

0.100 ± 0.010
(2.540 ± 0.254) TYP

0.300 – 0.320
(7.620 – 8.128)

0.065
(1.651)

95° ± 5°

0.280
(7.112) MIN

0.008 – 0.016
(0.203 – 0.406) TYP

$(0.325 {}^{+0.040}_{-0.015})$

$(8.255 {}^{+1.016}_{-0.381})$

N16E (REV F)

16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com