

August 1986 Revised March 2000

DM74LS26

Quad 2-Input NAND Gatewith High Voltage Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

These gates feature high-voltage output ratings (up to 15V) for interfacing with 12V systems. Although the outputs are rated for 15V, the device supply is still rated for 5V.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{O} (Min) - V_{OH}}{N_{1} (I_{OH}) + N_{2} (I_{IH})}$$

$$\mathsf{R}_{\mathsf{MIN}} = \frac{\mathsf{V}_{\mathsf{O}}\left(\mathsf{Max}\right) - \mathsf{V}_{\mathsf{OL}}}{\mathsf{I}_{\mathsf{OL}} - \mathsf{N}_{\mathsf{3}}\left(\mathsf{I}_{\mathsf{IL}}\right)}$$

Where:

 $N_1 \ (I_{OH}) = total \ maximum \ output \ high \ current$ for all outputs tied to pull-up resistor

 $N_2 \; (I_{IH}) = total \; maximum \; input \; high \; current \; for \; all \; inputs \; tied \; to \; pull-up \; resistor$

 N_3 (I_{II}) = total maximum input low current for

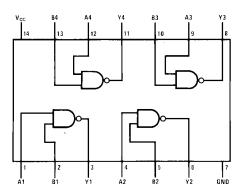
all inputs tied to pull-up resistor

Ordering Code:

Order Number	Package Number	Package Description
DM74LS26M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS26N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$$Y = \overline{AB}$$

Inp	Output		
Α	В	Υ	
L	L	Н	
L	Н	Н	
Н	L	Н	
Н	Н	L	

H = HIGH Logic Level L = LOW Logic Level

Absolute Maximum Ratings(Note 1)

7V Supply Voltage 7V Input Voltage Output Voltage 15V Operating Free Air Temperature Range 0°C to $+70^{\circ}\text{C}$

Storage Temperature Range $-65^{\circ}C$ to $+150^{\circ}C$ Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{IH}	HIGH Level Input Voltage	2			V
V _{IL}	LOW Level Input Voltage			0.8	V
V _{OH}	HIGH Level Output Voltage			15	V
I _{OL}	LOW Level Output Current			8	mA
T _A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

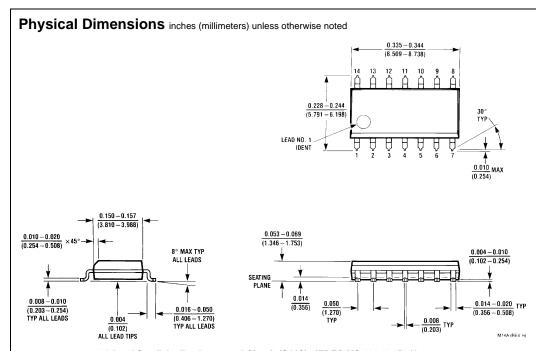
Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units	
VI	Input Clamp Voltage	$V_{CC} = Min, I_I = -18 \text{ mA}$				-1.5	V	
I _{CEX}	HIGH Level	V _{CC} = Min	V _O = 15V			1000	00	
	Output Current	$V_{IL} = Max$	V _O = 12V			50	μА	
V _{OL}	LOW Level	V _{CC} = Min, I _{OL} = Max			0.35 0.5			
	Output Voltage	V _{IH} = Min			0.33	0.5	V	
		I _{OL} = 4 mA, V _{CC} = Min			0.25	0.4		
II	Input Current @ Max	$V_{CC} = Max, V_I = 7V$			0.1		mA	
	Input Voltage	$V_I = 5.5V$					IIIA	
I _{IH}	HIGH Level Input Current	$V_{CC} = Max, V_I = 2.7V$				20	μΑ	
I _{IL}	LOW Level Input Current	$V_{CC} = Max, V_I = 0.4V$				-0.36	mA	
I _{CCH}	Supply Current with Outputs HIGH	V _{CC} = Max			0.8	1.6	mA	
I _{CCL}	Supply Current with Outputs LOW	V _{CC} = Max			2.4	4.4	mA	

Note 2: All typicals are at $V_{CC} = 5V$, $T_A = 25^{\circ}C$.

Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25^{\circ}C$

	Parameter					
Symbol		C _L = 15 pF		C _L = 50 pF		Units
		Min	Max	Min	Max	
t _{PLH}	Propagation Delay Time		20		45	ns
	LOW-to-HIGH Level Output		20		45	115
t _{PHL}	Propagation Delay Time		15		20	ns
	HIGH-to-LOW Level Output		15			



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.770 (18.80 - 19.56)0.090 (2.286) 14 13 12 11 10 9 8 14 13 12 INDEX AREA 0.250 ± 0.010 (6.350 ± 0.254) PIN NO. 1 PIN NO. 1 IDENT 1 2 3 4 5 6 7 1 2 3 $\frac{0.092}{(2.337)}$ DIA 0.030 MAX (0.762) DEPTH OPTION 1 OPTION 02 $\frac{0.135 \pm 0.005}{(3.429 \pm 0.127)}$ 0.300 - 0.320 $\frac{0.630 - 8.128}{(7.620 - 8.128)}$ 0.060 0.145 - 0.2004° TYP Optional (1.651) (3.683 - 5.080) $\frac{0.008 - 0.016}{(0.203 - 0.406)}$ TYP 0.020 (0.508) 0.125 - 0.150 0.075 ± 0.015 $\overline{(3.175 - 3.810)}$ (1.905 ± 0.381) (7.112) MIN 0.014 - 0.0230.100 ± 0.010 (2.540 ± 0.254) (0.356 - 0.584) $\frac{0.050 \pm 0.010}{(1.270 - 0.254)}$ TYP 0.325 ^{+0.040} -0.015 8.255 + 1.016

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A

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N144 (REV.F)