FAIRCHILD SEMICONDUCTOR™

August 1986
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DM74LS221 Dual Non-Retriggerable One-Shot with Clear and Complementary Outputs

General Description

The DM74LS221 is a dual monostable multivibrator with Schmitt-trigger input. Each device has three inputs permitting the choice of either leading-edge or trailing-edge triggering. Pin (A) is an active-LOW trigger transition input and pin (B) is an active-HIGH transition Schmitt-trigger input that allows jitter free triggering for inputs with transition rates as slow as 1 volt/second. This provides the input with excellent noise immunity. Additionally an internal latching circuit at the input stage also provides a high immunity to V_{CC} noise. The clear (CLR) input can terminate the output pulse at a predetermined time independent of the timing components. This (CLR) input also serves as a trigger input when it is pulsed with a low level pulse transition (⌐⌙). To obtain the best and trouble free operation from this device please read operating rules as well as the Fairchild Semiconductor one-shot application notes carefully and observe recommendations.

Features

- A dual, highly stable one-shot
- Compensated for V_{CC} and temperature variations
- Pin-out identical to DM74LS123 (Note 1)
- Output pulse width range from 30 ns to 70 seconds
- Hysteresis provided at (B) input for added noise immunity
- Direct reset terminates output pulse
- Triggerable from CLEAR input
- DTL, TTL compatible
- Input clamp diodes

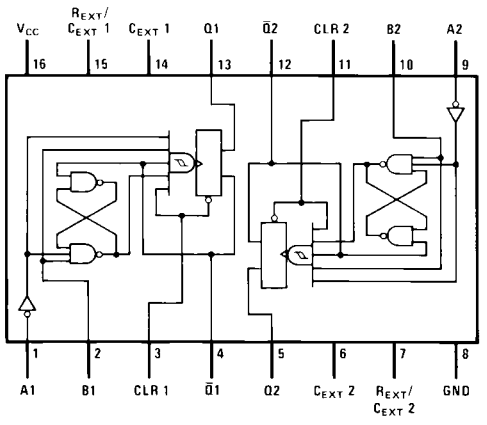
Note 1: The pin-out is identical to DM74LS123 but, functionally it is not; refer to Operating Rules #10 in this datasheet.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS221M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS221SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS221N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

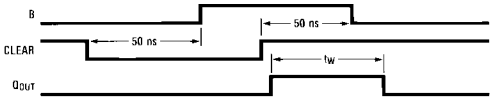


Function Table

Inputs			Outputs	
CLEAR	**A**	**B**	**Q**	**$\overline{Q}$**
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⌐⌙	⌐⌙
H	↓	H	⌐⌙	⌐⌙
↑ (Note 2)	L	H	⌐⌙	⌐⌙

H = HIGH Logic Level
L = LOW Logic Level
X = Can Be Either LOW or HIGH
↑ = Positive Going Transition
↓ = Negative Going Transition
⌐⌙ = A Positive Pulse
⌐⌙ = A Negative Pulse

Note 2: This mode of triggering requires first the B input be set from a LOW-to-HIGH level while the CLEAR input is maintained at logic LOW level. Then with the B input at logic HIGH level, the CLEAR input whose positive transition from LOW-to-HIGH will trigger an output pulse.



Functional Description

The basic output pulse width is determined by selection of an external resistor (R_X) and capacitor (C_X). Once triggered, the basic pulse width is independent of further input transitions and is a function of the timing components, or it may be reduced or terminated by use of the active low CLEAR input. Stable output pulse width ranging from 30 ns to 70 seconds is readily obtainable.

Operating Rules

1. An external resistor (R_X) and an external capacitor (C_X) are required for proper operation. The value of C_X may vary from 0 to approximately 1000 µF. For small time constants high-grade mica, glass, polypropylene, polycarbonate, or polystyrene material capacitor may be used. For large time constants use tantalum or special aluminum capacitors. If timing capacitor has leakages approaching 100 nA or if stray capacitance from either terminal to ground is greater than 50 pF the timing equations may not represent the pulse width the device generates.
2. When an electrolytic capacitor is used for C_X a switching diode is often required for standard TTL one-shots to prevent high inverse leakage current. This switching diode is not needed for the DM74LS221 one-shot and should not be used.

   Furthermore, if a polarized timing capacitor is used on the DM74LS221, the positive side of the capacitor should be connected to the "C_{EXT}" pin (Figure 1).
3. For $C_X >> 1000$ pF, the output pulse width (t_W) is defined as follows:

   $t_W = KR_X C_X$

   where [R_X is in kΩ]

   [C_X is in pF]

   [t_W is in ns]

   $K \approx Ln2 = 0.70$
4. The multiplicative factor K is plotted as a function of C_X for design considerations: (See Figure 4).
5. For $C_X < 1000$ pF see Figure 3 for t_W vs. C_X family curves with R_X as a parameter.
6. To obtain variable pulse widths by remote trimming, the following circuit is recommended: (See Figure 2).
7. Output pulse width versus V_{CC} and temperatures: Figure 5 depicts the relationship between pulse width variation versus V_{CC}. Figure 6 depicts pulse width variation versus temperatures.
8. Duty cycle is defined as $t_W/T \times 100$ in percentage, if it goes above 50% the output pulse width will become shorter. If the duty cycle varies between LOW and HIGH values, this causes output pulse width to vary, or jitter (a function of the R_{EXT} only). To reduce jitter, R_{EXT} should be as large as possible, for example, with $R_{EXT} = 100k$ jitter is not appreciable until the duty cycle approaches 90%.
9. Under any operating condition C_X and R_X must be kept as close to the one-shot device pins as possible to minimize stray capacitance, to reduce noise pick-up, and to reduce I-R and Ldi/dt voltage developed along their connecting paths. If the lead length from C_X to pins (6) and (7) or pins (14) and (15) is greater than 3 cm, for example, the output pulse width might be quite different from values predicted from the appropriate equations. A non-inductive and low capacitive path is necessary to ensure complete discharge of C_X in each cycle of its operation so that the output pulse width will be accurate.
10. Although the DM74LS221's pin-out is identical to the DM74LS123 it should be remembered that they are not functionally identical. The DM74LS123 is a retriggerable device such that the output is dependent upon the input transitions when its output "Q" is at the "High" state. Furthermore, it is recommended for the DM74LS123 to externally ground the C_{EXT} pin for improved system performance. However, this pin on the DM74LS221 is not an internal connection to the device ground. Hence, if substitution of an DM74LS221 onto an DM74LS123 design layout where the C_{EXT} pin is wired to the ground, the device will not function.
11. V_{CC} and ground wiring should conform to good high-frequency standards and practices so that switching transients on the V_{CC} and ground return leads do not cause interaction between one-shots. A 0.01 µF to 0.10 µF bypass capacitor (disk ceramic or monolithic type) from V_{CC} to ground is necessary on each device. Furthermore, the bypass capacitor should be located as close to the V_{CC}-pin as space permits.

Operating Rules (Continued)

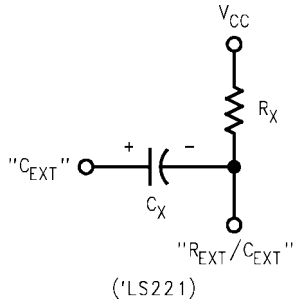
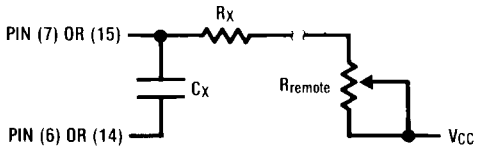


FIGURE 1.



Note: "R_{remote}" should be as close to the one-shot as possible.

FIGURE 2.

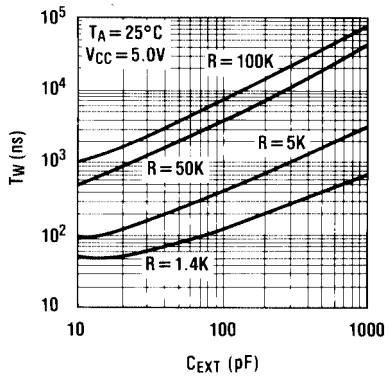


FIGURE 3.

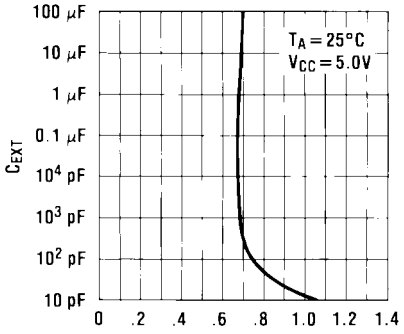


FIGURE 4.

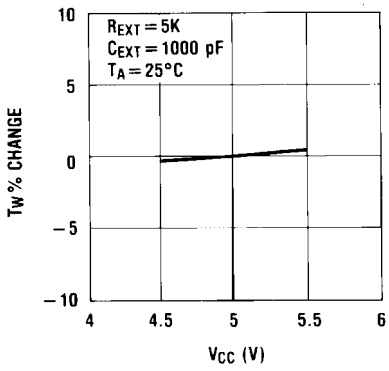


FIGURE 5.

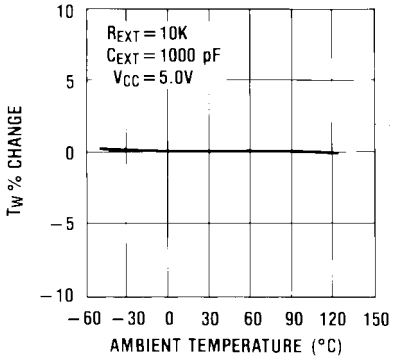


FIGURE 6.

Note: For further detailed device characteristics and output performance, please refer to the Fairchild Semiconductor one-shot application note AN-372.

Absolute Maximum Ratings(Note 3)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 3: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage at the A Input (V_{CC} = Min)			1	2	V
V_{T-}	Negative-Going Input Threshold Voltage at the A Input (V_{CC} = Min)		0.8	1		V
V_{T+}	Positive-Going Input Threshold Voltage at the B Input (V_{CC} = Min)			1	2	V
V_{T-}	Negative-Going Input Threshold Voltage at the B Input (V_{CC} = Min)		0.8	0.9		V
I_{OH}	HIGH Level Output Current				−0.4	mA
I_{OL}	LOW Level Output Current				8	mA
t_W	Pulse Width	Data	40			ns
	(Note 4)	Clear	40			
t_{REL}	Clear Release Time (Note 4)		15			ns
$\frac{dV}{dt}$	Rate of Rise or Fall of Schmitt Input (B) (Note 4)				1	$\frac{V}{s}$
$\frac{dV}{dt}$	Rate of Rise or Fall of Logic Input (A) (Note 4)				1	$\frac{V}{\mu s}$
R_{EXT}	External Timing Resistor (Note 4)		1.4		100	kΩ
C_{EXT}	External Timing Capacitance (Note 4)		0		1000	μF
DC	Duty Cycle	R_T = 2 kΩ			50	%
	(Note 4)	$R_T = R_{EXT}$ (Max)			60	
T_A	Free Air Operating Temperature		0		70	°C

Note 4: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 5)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = –18 mA				–1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min			0.35	0.5	V
		V_{CC} = Min, I_{OL} = 4 mA				0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max V_I = 0.4V	A1, A2			–0.4	mA
			B			–0.8	
			Clear			–0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 6)		–20		–100	mA
I_{CC}	Supply Current	V_{CC} = Max	Quiescent		4.7	11	mA
			Triggered		19	27	

Note 5: All typicals are at V_{CC} = 5V, T_A = 25°C.

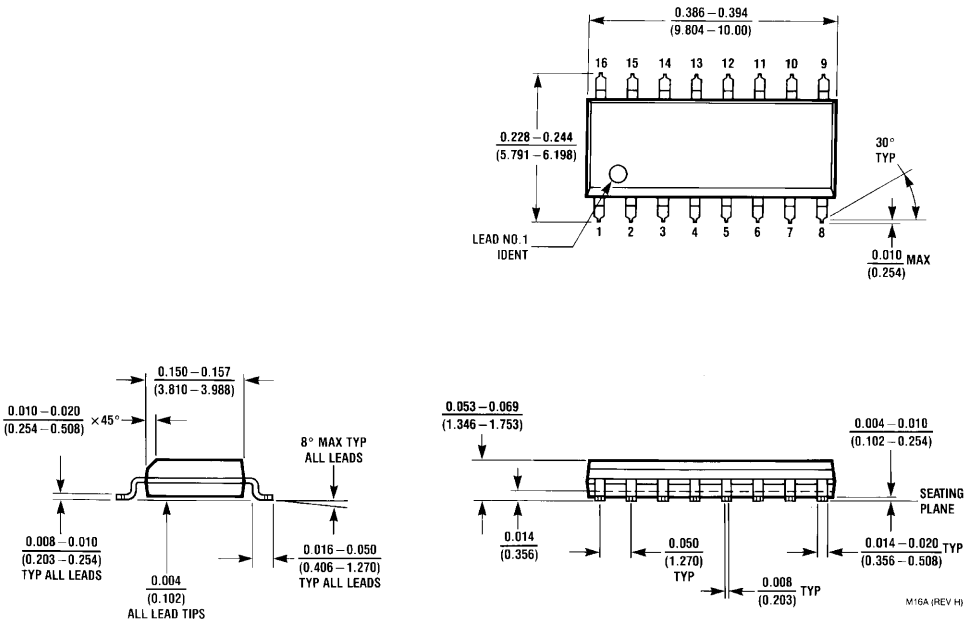
Note 6: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

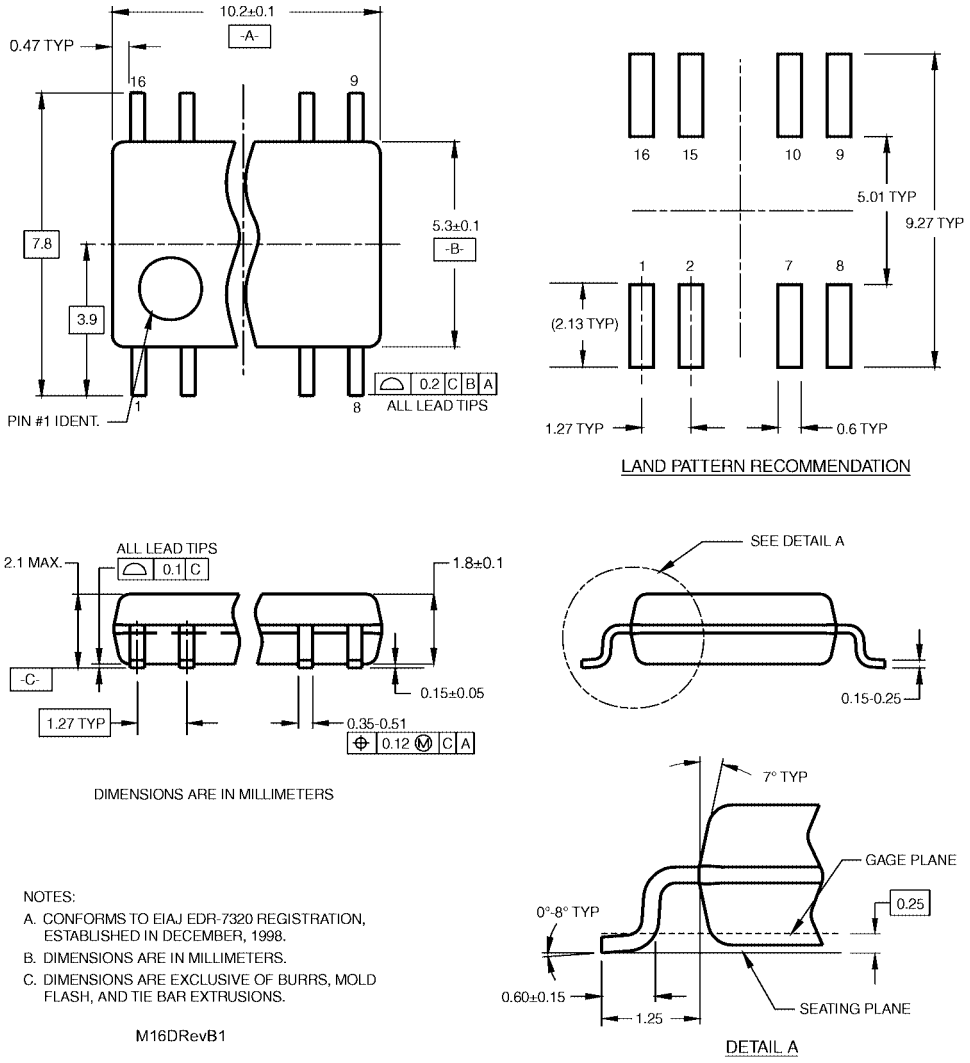
Symbol	Parameter	From (Input) To (Output)	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	A1, A2 to Q	C_{EXT} = 80 pF R_{EXT} = 2 kΩ C_L = 15 pF R_L = 2 kΩ		70	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	B to Q			55	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	A1, A2 to Q			80	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	B to $\overline{Q}$			65	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clear to $\overline{Q}$			65	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Q			55	ns
$t_{W(out)}$	Output Pulse Width Using Zero Timing Capacitance	A1, A2 to Q, $\overline{Q}$	C_{EXT} = 0 R_{EXT} = 2 kΩ R_L = 2 kΩ C_L = 15 pF	20	70	ns
$t_{W(out)}$	Output Pulse Width Using External Timing Resistor	A1, A2 to Q, $\overline{Q}$	C_{EXT} = 100 pF R_{EXT} = 10 kΩ R_L = 2 kΩ C_L = 15 pF	600	750	ns
			C_{EXT} = 1 µF R_{EXT} = 10 kΩ R_L = 2 kΩ C_L = 15 pF	6	7.5	ms
			C_{EXT} = 80 pF R_{EXT} = 2 kΩ R_L = 2 kΩ C_L = 15 pF	70	150	ns

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

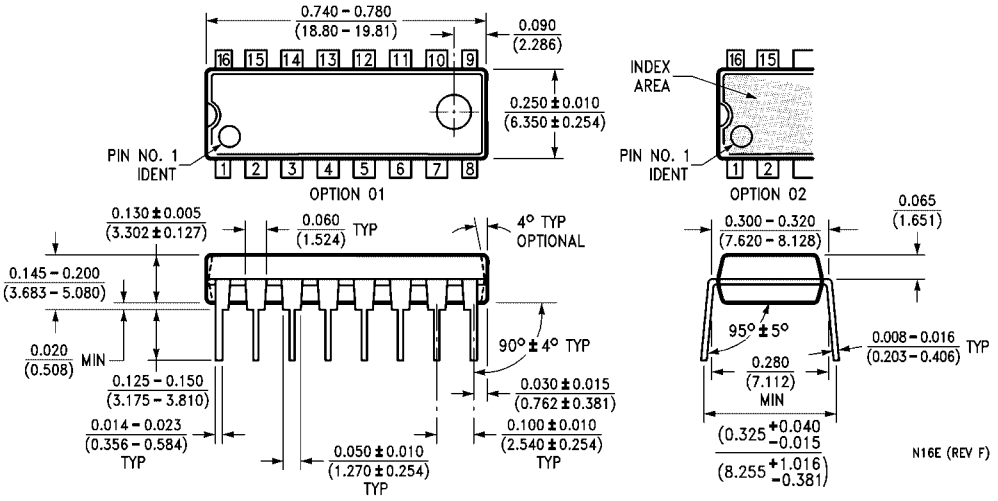
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1

16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E