

October 1986 Revised June 2001

DM74ALS652 Octal 3-STATE Bus Transceiver and Register

General Description

This device incorporates an octal transceiver and an octal D-type register configured to enable transmission of data from bus to bus or internal register to bus.

This bus transceiver features totem-pole 3-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high level logic drive provide this device with the capability of being connected directly to and driving the bus lines in a bus organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The registers in the DM74ALS652 are edge-triggered D-type flip-flops. On the positive transition of the clock (CAB or CBA), the input data is stored into the appropriate register. The CAB input controls the transfer of data into the A register and the CBA input controls the B register.

The SAB and SBA control pins are provided to select whether real-time data or stored data is transferred. A LOW input level selects real-time data and a HIGH level selects stored data. The select controls have a "make before break" configuration to eliminate a glitch which would normally occur in a typical multiplexer during the transition between stored and real-time data.

The enable (GAB and $\overline{G}BA$) control pins provide four modes of operation: real-time data transfer from bus A to B, real-time data transfer from bus B to A, real-time bus A and/or B data transfer to internal storage, or internal stored data transfer to bus A and/or B.

Features

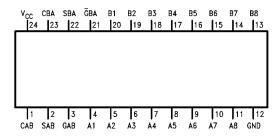
- Switching specifications at 50 pF
- \blacksquare Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- 3-STATE buffer-type outputs drive bus lines directly
- Independent registers and enables for A and B buses
- Multiplexed real-time and stored data

Ordering Code:

Order Number	Package Number	Package Description
DM74ALS652WM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
DM74ALS652NT	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

	Inputs			Data I/O (Note 1)		Operation or Franction		
GAB	GBA	CAB	СВА	SAB	SBA	A1 thru A8	B1 thru B8	Operation or Function
Х	Н	1	H/L	Х	Х	Input	Not Specified	Store A, Hold B
L	Х	H/L	1	X	X	Not Specified	Input	Store B, Hold A
L	Н	1	1	Х	Х	Input	Input	Store A and B Data
L	Н	H/L	H/L	Х	Х	Input	Input	Isolation, Hold Storage
L	L	Х	Х	Х	L	Output	Input	Real-Time B Data to A Bus
L	L	Х	H/L	Х	Н	Output	Input	Stored B Data to A Bus
Н	Н	Х	Χ	L	Х	Input	Output	Real-Time A Data to B Bus
Н	Н	1	1	Х	Х	Input	Output	Stored A Data to B Bus
Н	Н	1	1	X (Note 2)	Х	Input	Output	Store A in both Registers
L	L	↑	↑	Х	X (Note 2)	Output	Input	Store B in both Registers
Н	L	H or L	H or L	Н	Н	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

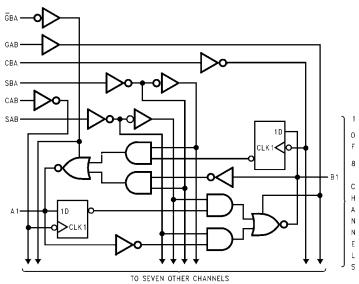
H = HIGH Logic Level

Note 1: The data output functions may be enabled or disabled by various signals at the \overline{G} and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.

Note 2: Select control = L; clocks can occur simultaneously

 $\label{eq:Select control} \textbf{Select control} = \textbf{H}; \ \textbf{clocks must be staggered in order to load both registers}.$

Logic Diagram



H = HIGH Logic Level
L = LOW Logic Level
X = Don't Care (Either LOW or HIGH Logic Levels, including transitions)
H/L = Either LOW or HIGH Logic Level excluding transitions
↑ = Positive-going edge of pulse

Absolute Maximum Ratings(Note 3)

Supply Voltage 7V

Input Voltage

7V Control Inputs 5.5V

I/O Ports

0°C to +70°C Operating Free-Air Temperature Range -65°C to +150°C

Storage Temperature Range

Typical θ_{JA}

44.5°C/W N Package

80.5°C/W M Package

Note 3: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions

for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units	
V _{CC}	Supply Voltage	4.5	5	5.5	V	
V _{IH}	HIGH Level Input Voltage	2			V	
V _{IL}	LOW Level Input Voltage			0.8	V	
I _{OH}	HIGH Level Output Current			-15	mA	
I _{OL}	LOW Level Output Current			24	mA	
f _{CLK}	Clock Frequency	0		40	MHz	
t _W	Pulse Duration, Clocks LOW or HIGH	12.5			ns	
t _{SU}	Data Setup Time, A before CAB or B before CBA (Note 4)	10↑			ns	
t _H	Data Hold Time, A after CAB or B after CBA (Note 4)	0↑			ns	
T _A	Free Air Operating Temperature	0		70	°C	

Note 4: ↑ = with reference to the LOW-to-HIGH transition of the respective clock.

Electrical Characteristics

over recommended free air temperature range

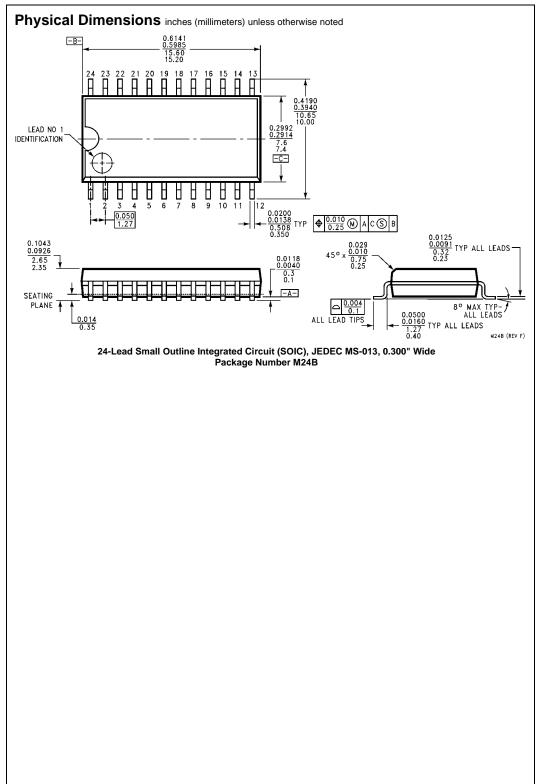
Symbol	Parameter	Test C	Test Conditions			Max	Units	
V _{IK}	Input Clamp Voltage	$V_{CC} = Min, I_I = -18 \text{ mA}$			-1.2	V		
V _{OH}	HIGH Level	$V_{CC} = 4.5V \text{ to } 5.5V$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} – 2				
	Output Voltage	V _{CC} = Min	$I_{OH} = -3 \text{ mA}$	2.4	3.2		V	
			I _{OH} = Max	2				
V _{OL}	LOW Level	V _{CC} = Min	I _{OL} = 12 mA		0.25	0.4		
	Output Voltage		$I_{OL} = 24 \text{ mA}$		0.35	0.5	V	
			$I_{OL} = 48 \text{ mA}$		0.35	0.5		
I _I	Input Current at Maximum	V _{CC} = Max	I/O Ports, $V_I = 5.5V$			100	μА	
	Input Voltage		Control Inputs, $V_I = 7V$			100	μА	
I _{IH}	HIGH Level Input Current	V _{CC} = Max, V _I = 2.7V, (N	V _{CC} = Max, V _I = 2.7V, (Note 5)			20	μΑ	
I _{IL}	LOW Level	V _{CC} = Max,	Control Inputs			-200	^	
	Input Current	V _I = 0.4V (Note 5)	I/O Ports			-200	μА	
I _O	Output Drive Current	$V_{CC} = Max, V_O = 2.25V$	$V_{CC} = Max$, $V_O = 2.25V$			-112	mA	
Icc	Supply Current	V _{CC} = Max	Outputs HIGH		47	76		
			Outputs LOW		55	88	mA	
			Outputs Disabled		55	88		

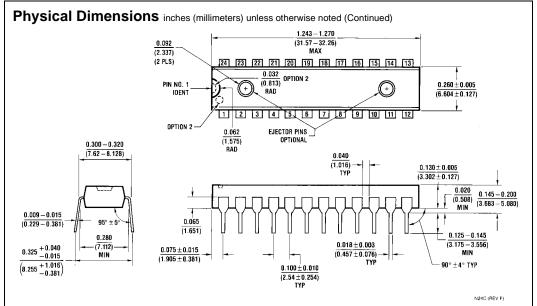
Note 5: For I/O ports the 3-STATE output currents (I_{OZH} and I_{OZL}) are included in the I_{IH} and I_{IL} parameters.

Switching Characteristics over recommended operating free air temperature range (Note 6)

Symbol	Parameter	Conditions	From (Input) To (Output)	Min	Max	Units
t _{PLH}	Propagation Delay Time	$V_{CC} = 4.5V \text{ to } 5.5V,$	CBA or CAB			
	LOW-to-HIGH Level Output	$C_L = 50 \text{ pF},$	to A or B	10	30	ns
t _{PHL}	Propagation Delay Time	$R_1 = R_2 = 500\Omega,$	CBA or CAB	_	4-7	
	HIGH-to-LOW Level Output	T _A = Min to Max	to A or B	5	17	ns
t _{PLH}	Propagation Delay Time		A or B to	-	40	
	LOW-to-HIGH Level Output		B or A	5	18	ns
t _{PHL}	Propagation Delay Time		A or B to		40	
	HIGH-to-LOW Level Output		B or A	3	12	ns
t _{PLH}	Propagation Delay Time					
	LOW-to-HIGH Level Output		SBA or SAB	12	35	ns
	(with A or B LOW) (Note 6)		to A or B			
t _{PHL}	Propagation Delay Time					
	HIGH-to-LOW Level Output		SBA or SAB	6	20	ns
	(with A or B LOW) (Note 6)		to A or B			
t _{PLH}	Propagation Delay Time					
	LOW-to-HIGH Level Output		SBA or SAB	6	25	ns
	(with A or B HIGH) (Note 6)		to A or B			
t _{PHL}	Propagation Delay Time					
	HIGH-to-LOW Level Output		SBA or SAB	5	20	ns
	(with A or B HIGH) (Note 6)		to A or B			
t _{PZH}	Output Enable Time		GBA to	_		
	to HIGH Level Output		Α	3	17	ns
t _{PZL}	Output Enable Time		GBA to			
TZL	to LOW Level Output		А	5	18	ns
t _{PHZ}	Output Disable Time		GBA to			
'PHZ	from HIGH Level Output		A	1	10	ns
	· '		GBA to			
t _{PLZ}	Output Disable Time			2	16	ns
	from LOW Level Output		A GAB to			
t _{PZH}	Output Enable Time		GAB to B	6	22	ns
	to HIGH Level Output		GAB to			
t _{PZL}	Output Enable Time to LOW Level Output		GAB to B	6	18	ns
t	Output Disable Time		GAB to			
t _{PHZ}	from HIGH Level Output		GAB to B	1	10	ns
+	Output Disable Time		GAB to			
t _{PLZ}	from LOW Level Output		B GAB to	2	16	ns
	nom Low Level Output		D		1	

Note 6: These parameters are measured with the internal output state of the storage register opposite to that of the bus input.





24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N24C

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