

# DM74ALS165

## 8-Bit Parallel In/Serial Out Shift Register

### Features

- Complementary outputs
- Direct overriding load (data) inputs
- Gated clock inputs
- Parallel-to-serial data conversion

### General Description

The DM74ALS165 is an 8-bit serial register that, when clocked, shifts the data toward serial output,  $\overline{Q}_H$ . Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the  $\overline{SH}/\overline{LD}$  input. The DM74ALS165 also features a clock inhibit function and a complemented serial output,  $\overline{Q}_H$ .

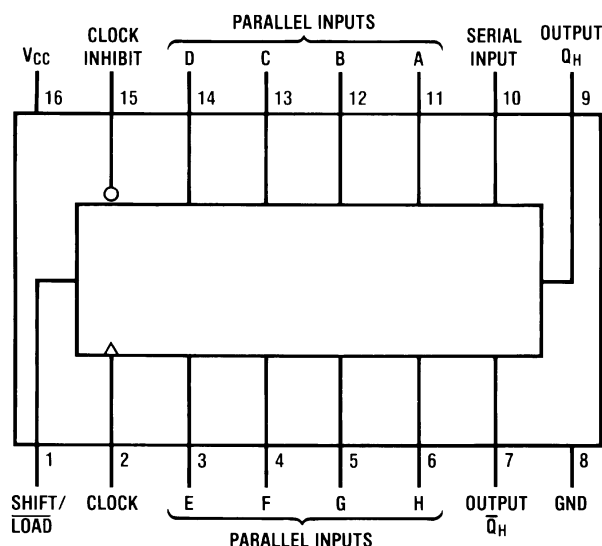
Clocking is accomplished by a LOW-to-HIGH transition of the CLK input while  $\overline{SH}/\overline{LD}$  is held HIGH and CLK INH is held LOW. The functions of the CLK and CLK INH (clock inhibit) inputs are interchangeable. Since a LOW CLK input and a LOW-to-HIGH transition of CLK INH will also accomplish clocking, CLK INH should be changed to the high level only while the CLK input is HIGH. Parallel loading is inhibited when  $\overline{SH}/\overline{LD}$  is held HIGH. The parallel inputs to the register are enabled while  $\overline{SH}/\overline{LD}$  is LOW independently of the levels of CLK, CLK INH, or SER inputs.

### Ordering Information

Order Number	Package Number	Package Description
DM74ALS165M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering number.

### Connection Diagram



Function Table

Inputs					Internal Outputs		Output $Q_H$
Shift/Load	Clock Inhibit	Clock	Serial	Parallel A...H	$Q_A$	$Q_B$	
L	X	X	X	a...h	a	b	h
H	L	L	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{H0}$
H	L	$\uparrow$	H	X	H	$Q_{An}$	$Q_{Gn}$
H	L	$\uparrow$	L	X	L	$Q_{An}$	$Q_{Gn}$
H	$\uparrow$	L	H	X	H	$Q_{An}$	$Q_{Gn}$
H	$\uparrow$	L	L	X	L	$Q_{An}$	$Q_{Gn}$
H	H	X	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{H0}$

H = HIGH Level (steady-state)

L = LOW Level (steady-state)

X = Don't Care (any input, including transitions)

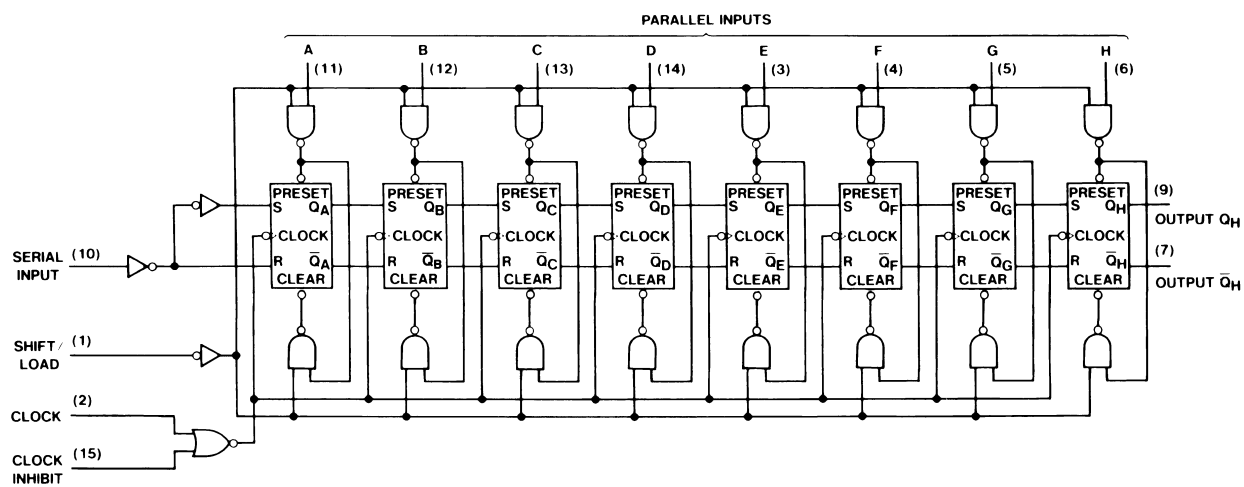
$\uparrow$  = Transition from LOW-to-HIGH level

a...h = The level of steady-state input at inputs A through H, respectively

$Q_{A0}$ ,  $Q_{B0}$ ,  $Q_{H0}$  = The level of  $Q_A$ ,  $Q_B$ , or  $Q_H$ , respectively, before the indicated steady-state input conditions were established

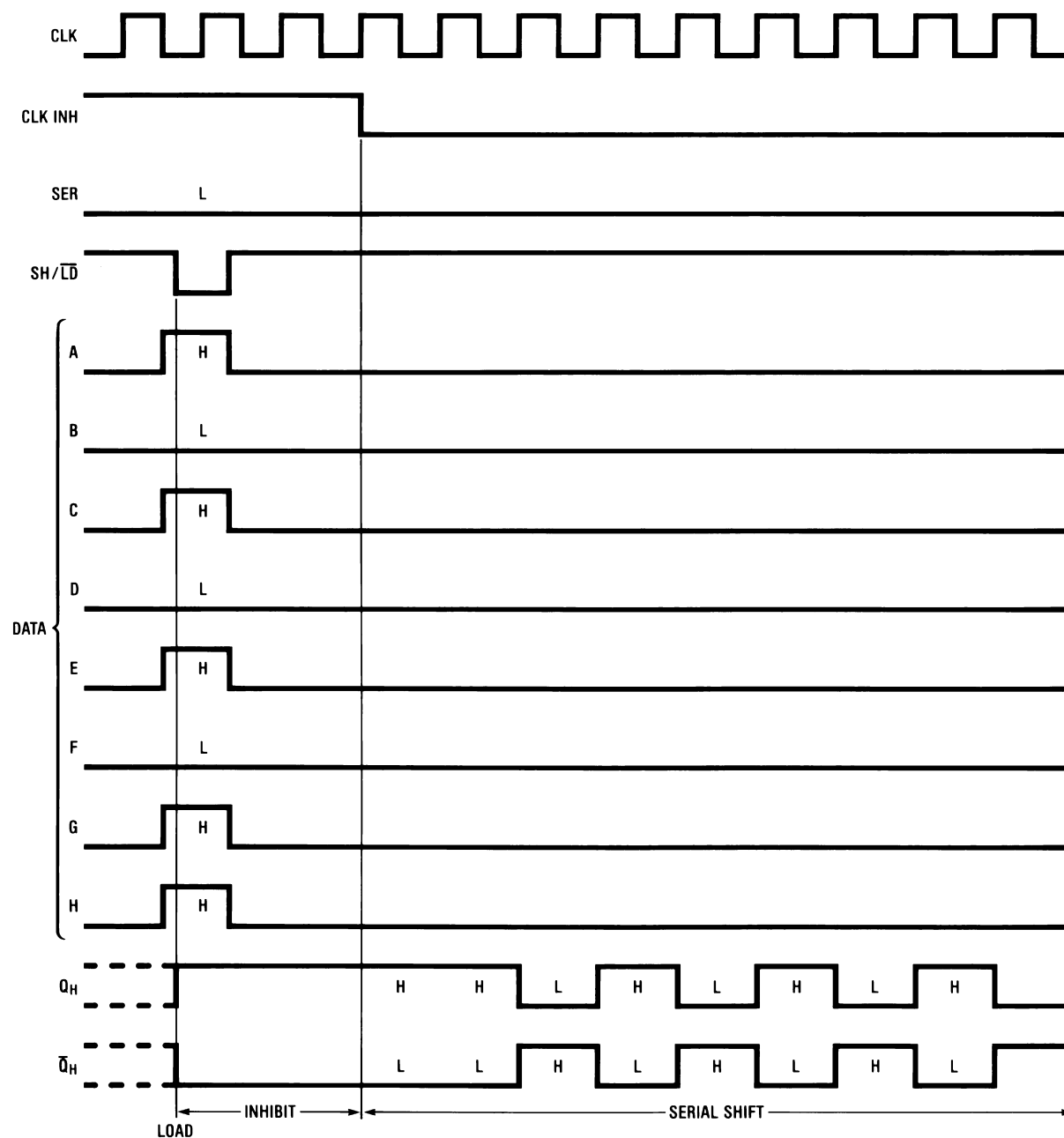
$Q_{An}$ ,  $Q_{Gn}$  = The level of  $Q_A$  or  $Q_G$ , respectively, before the most recent  $\uparrow$  transition of the clock

Logic Diagram



## Timing Diagram

Typical Shift, Load, and Inhibit Sequences



## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	7V
$V_I$	Input Voltage	7V
$T_A$	Operating Free Air Temperature Range	0°C to +70°C
$T_{STG}$	Storage Temperature Range	–65°C to +150°C
$\theta_{JA}$	Typical Thermal Resistance	104.0°C/W

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter		Min.	Typ.	Max.	Units
$V_{CC}$	Supply Voltage		4.5	5	5.5	V
$V_{IH}$	HIGH Level Input Voltage		2			V
$V_{IL}$	LOW Level Input Voltage				0.8	V
$I_{OH}$	HIGH Level Output Current				–0.4	mA
$I_{OL}$	LOW Level Output Current				8	mA
$f_{CLOCK}$	Clock Frequency		45			MHz
$t_W$	Pulse Duration	CLK HIGH	11			ns
		CLK LOW	11			
		Load	12			
$t_{SU}$	Setup Time	SH/ $\overline{LD}$	10			ns
		Data	10			
$t_{SU}$	Setup Time	CLK INH ↓ before CLK	11			ns
		Serial before CLK	10			
$t_H$	Hold Time		4			ns
$T_A$	Operating Free Air Temperature		0		70	°C

## Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted).

Symbol	Parameter	Conditions	Min.	Typ. <sup>(1)</sup>	Max.	Units
$V_{IK}$	Input Clamp Voltage	$V_{CC} = 4.5V$ , $I_I = -18mA$			-1.5	V
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -0.4mA$ $V_{CC} = 4.5V$ to $5.5V$	$V_{CC} - 2$			V
$V_{OL}$	LOW Level Output Voltage	$V_{CC} = 4.5V$ $I_{OL} = 4mA$ $I_{OL} = 8mA$		0.25 0.35	0.4 0.5	V
$I_I$	Input Current at Max Input Voltage	$V_{CC} = 5.5V$ , $V_I = 7V$			0.1	mA
$I_{IH}$	HIGH Level Input Current	$V_{CC} = 5.5V$ , $V_I = 2.7V$			20	$\mu A$
$I_{IL}$	LOW Level Input Current	$V_{CC} = 5.5V$ , $V_I = 0.4V$			-0.1	mA
$I_O^{(2)}$	Output Drive Current	$V_{CC} = 5.5V$ , $V_O = 2.25V$	-30		-112	mA
$I_{CC}$	Supply Current	$V_{CC} = 5.5V^{(3)}$		16	24	mA

### Notes:

1. All typical values are at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ .
2. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .
3. With the outputs open, CLK INH and CLK at 4.5V, and a clock pulse applied to the SH/ $\overline{LD}$  input,  $I_{CC}$  is measured first with the parallel inputs at 4.5V, then with the parallel inputs grounded.

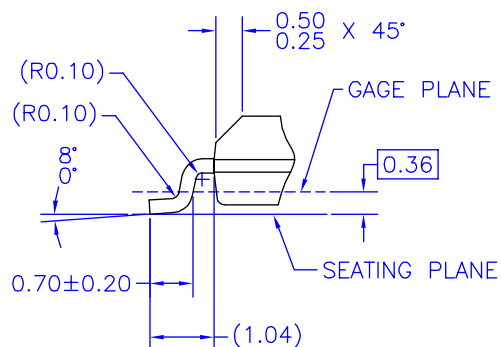
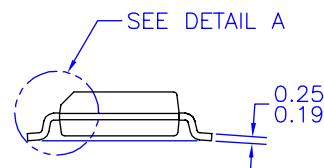
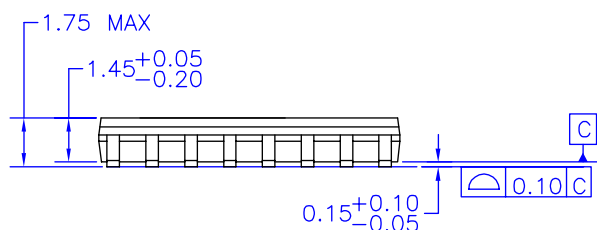
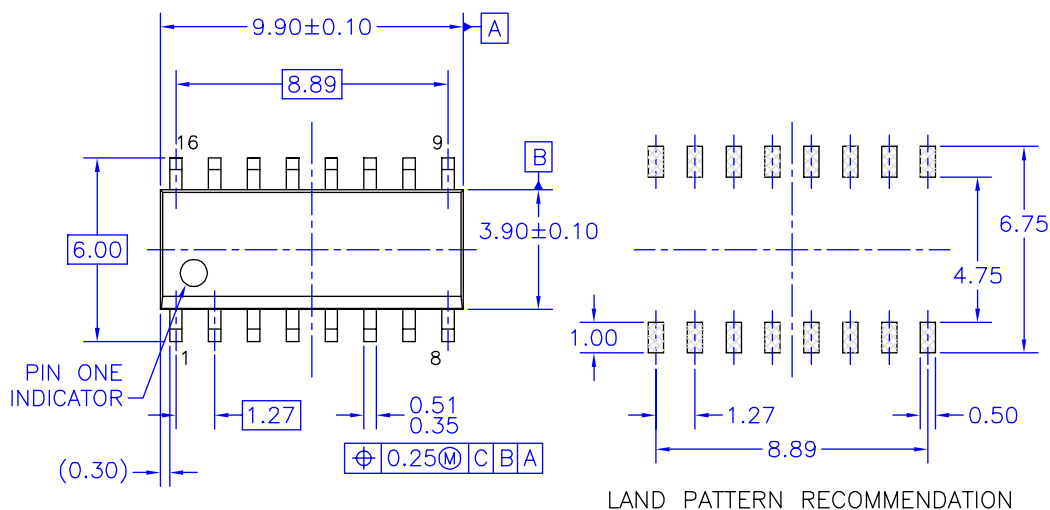
## Switching Characteristics

Over recommended free air temperature range. All typical values are measured at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ .

Symbol	Parameter	Input	Output	Conditions	Min.	Typ.	Max.	Units
$f_{MAX}$	Maximum Frequency			$V_{CC} = 4.5V$ to $5.5V$ , $C_L = 50pF$ , $R_L = 500\Omega$ $T_A = \text{Min. to Max.}$	45	60		MHz
$t_{PLH}$	Propagation Delay Time, LOW-to-HIGH Level Output	Load	$Q_H$ or $\overline{Q}_H$		4	13	20	ns
$t_{PHL}$	Propagation Delay Time, HIGH-to-LOW Level Output	Load	$Q_H$ or $\overline{Q}_H$		4	14	22	ns
$t_{PLH}$	Propagation Delay Time, LOW-to-HIGH Level Output	CLK	$Q_H$ or $\overline{Q}_H$		3	7	13	ns
$t_{PHL}$	Propagation Delay Time, HIGH-to-LOW Level Output	CLK	$Q_H$ or $\overline{Q}_H$		3	9	14	ns
$t_{PLH}$	Propagation Delay Time, LOW-to-HIGH Level Output	H	$Q_H$		3	7	13	ns
$t_{PHL}$	Propagation Delay Time, HIGH-to-LOW Level Output	H	$Q_H$		3	9	16	ns
$t_{PLH}$	Propagation Delay Time, LOW-to-HIGH Level Output	H	$\overline{Q}_H$		2	8	15	ns
$t_{PHL}$	Propagation Delay Time, HIGH-to-LOW Level Output	H	$\overline{Q}_H$		3	9	16	ns

## Physical Dimensions

Dimensions are in millimeters unless otherwise noted.



DETAIL A  
SCALE: 2:1

NOTES: UNLESS OTHERWISE SPECIFIED


- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AC, ISSUE C, DATED MAY 1990.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) STANDARD LEAD FINISH:  
200 MICROINCHES / 5.08 MICRONS MIN.  
LEAD/TIN (SOLDER) ON COPPER.

M16AREVK

**Figure 1. 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A**

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