# **DM7474 Dual Positive-Edge-Triggered D-Type Flip-Flops** with Preset, Clear and Complementary Outputs

### **General Description**

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This device contains two independent positive-edge-triggered D-type flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the

transition time of the rising edge of the clock. The data on the D input may be changed while the clock is LOW or HIGH without affecting the outputs as long as the data setup and hold times are not violated. A LOW logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

# **Ordering Code:**

Order Number	Package Number	Package Description
DM7474M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
DM7474N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Devices also available	in Tape and Reel, Specify	y by appending the suffix letter "X" to the ordering code.

#### **Connection Diagram**

CLR 2 D2 CLK 2 GND CLR 1 n 1 CLK 1

## **Function Table**

	Inp	Outputs			
PR	CLR	CLK	D	Q	Q
L	Н	Х	Х	Н	L
Н	L	Х	Х	L	Н
L	L	х	х	H (Note 1)	H (Note 1)
н	н	$\uparrow$	н	н	L
н	н	↑ (	L	L	н
н	н	L	х	<b>Q</b> <sub>0</sub>	$\overline{Q}_0$

H = HIGH Logic Level X = Either LOW or HIGH Logic Level

L = LOW Logic Level

 $\uparrow$  = Positive-going transition of the clock.  $\rm Q_0$  = The output logic level of Q before the indicated input conditions were established.

Note 1: This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (HIGH) level.

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# Absolute Maximum Ratings(Note 2)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## **Recommended Operating Conditions**

Symbol	Pa	rameter	Min	Nom	Max	Units
V <sub>CC</sub>	Supply Voltage		4.75	5	5.25	V
V <sub>IH</sub>	HIGH Level Input Voltage		2			V
V <sub>IL</sub>	LOW Level Inpu	t Voltage			0.8	V
он	HIGH Level Output Current				-0.4	mA
lol	LOW Level Output Current				16	mA
CLK	Clock Frequency (Note 4)		0		15	MHz
tw	Pulse Width	Clock HIGH	30			
	(Note 4)	Clock LOW	37			ns
		Clear LOW	30			115
		Preset LOW	30			
SU	Input Setup Time (Note 3)(Note 4)		20↑			ns
н	Input Hold Time (Note 3)(Note 4)		5↑			ns
Γ <sub>A</sub>	Free Air Operating Temperature		0		70	°C

Note 3: The symbol  $(\uparrow)$  indicates the rising edge of the clock pulse is used for reference.

Note 4:  $T_A = 25^\circ C$  and  $V_{CC} = 5 V.$ 

### **Electrical Characteristics**

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 5)	Max	Units	
VI	Input Clamp Voltage	$V_{CC} = Min$ , $I_I = -12 \text{ mA}$				-1.5	V	
V <sub>OH</sub>	HIGH Level Output Voltage	$V_{CC} = Min, I_{OH} = Max$ $V_{II} = Max, V_{IH} = Min$		2.4	3.4		V	
V <sub>OL</sub>	LOW Level Output Voltage	$V_{CC} = Min, I_{OL} = Max$ $V_{IH} = Min, V_{IL} = Max$			0.2	0.4	V	
l <sub>l</sub>	Input Current @ Max Input Voltage	$V_{CC} = Max, V_I = 5.5V$				1	mA	
IIH	HIGH Level	V <sub>CC</sub> = Max	D			40		
	Input Current	$V_I = 2.4V$	Clock			80		
			Clear			120	μA	
			Preset			40		
IIL	LOW Level	V <sub>CC</sub> = Max	D			-1.6		
	Input Current	$V_I = 0.4V$	Clock			-3.2		
		(Note 8)	Clear			-3.2	mA	
			Preset			-1.6	1	
l <sub>os</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 6)	•	-18		-55	mA	
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = Max (Note 7)			17	30	mA	

Note 5: All typicals are at V<sub>CC</sub> = 5V,  $T_A = 25^{\circ}C$ .

Note 6: Not more than one output should be shorted at a time.

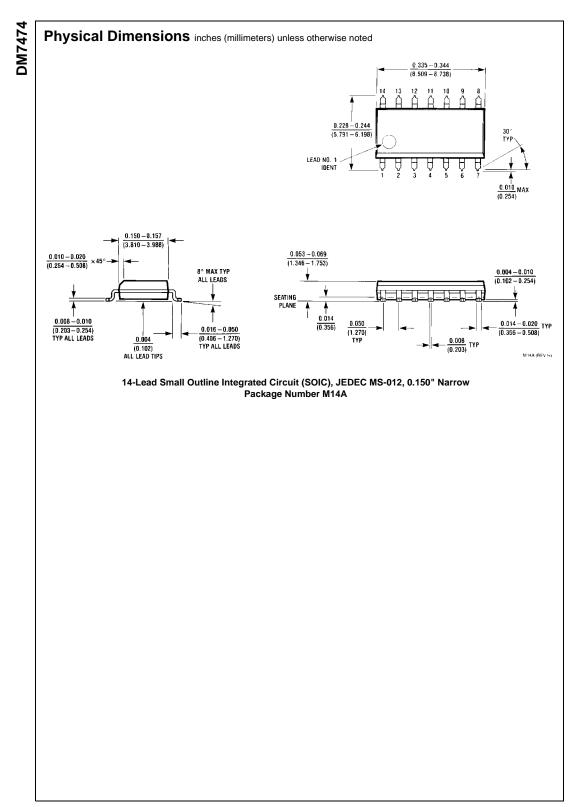
Note 7: With all outputs open,  $I_{CC}$  is measured with the Q and  $\overline{Q}$  outputs HIGH in turn. At the time of measurement the clock is grounded.

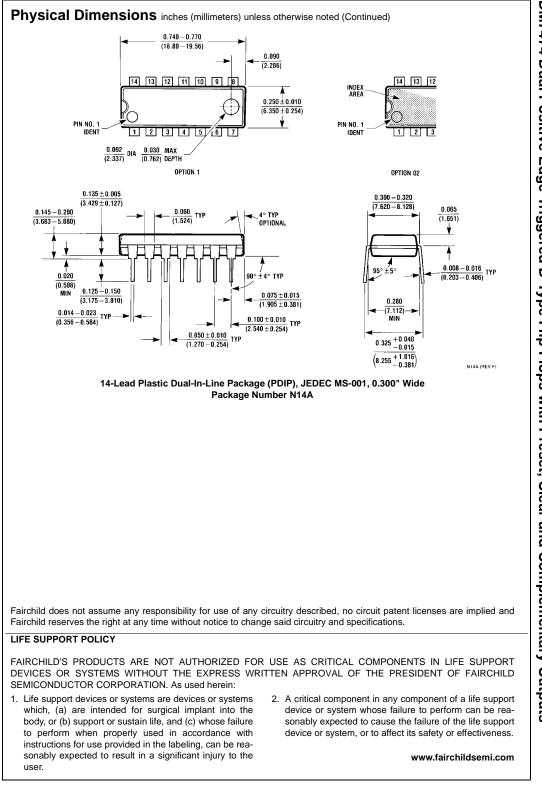
Note 8: Clear is tested with preset HIGH and preset is tested with clear HIGH.

Symbol	Parameter	From (Input)	$R_L = 400\Omega$	Units	
		To (Output)	o (Output) Min Max	Max	Units
f <sub>MAX</sub>	Maximum Clock Frequency		15		MHz
t <sub>PHL</sub>	Propagation Delay Time HIGH-to-LOW Level Output	Preset to Q		40	ns
t <sub>PLH</sub>	Propagation Delay Time LOW-to-HIGH Level Output	Preset to Q		25	ns
t <sub>PHL</sub>	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Q		40	ns
t <sub>PLH</sub>	Propagation Delay Time LOW-to-HIGH Level Output	Clear to Q		25	ns
t <sub>PHL</sub>	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Q or $\overline{Q}$		40	ns
t <sub>PLH</sub>	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Q or $\overline{Q}$		25	ns

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