

CD4010C Hex Buffers (Non-Inverting)

General Description

The CD4010C hex buffers are monolithic complementary MOS (CMOS) integrated circuits. The N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge. These gates may be used as hex buffers, CMOS to DTL or TTL interface or as CMOS current drivers. Conversion ranges are from 3V to 15V providing $V_{CC} \leq V_{DD}$. The devices also have buffered outputs which improve transfer characteristics by providing very high gain.

Features

- Wide supply voltage range: 3.0V to 15V
- Low power: 100 nW (typ.)
- High noise immunity: $0.45 V_{DD}$ (typ.)
- High current sinking: 8 mA (min.) at $V_O = 0.5V$ capability: and $V_{DD} = 10V$

Applications

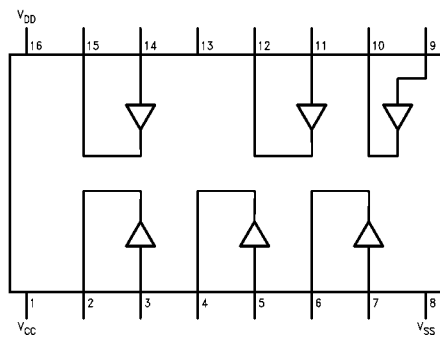
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial controls
- Remote metering
- Computers

Ordering Code:

Order Number	Package Number	Package Description
CD4010CM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4010CN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

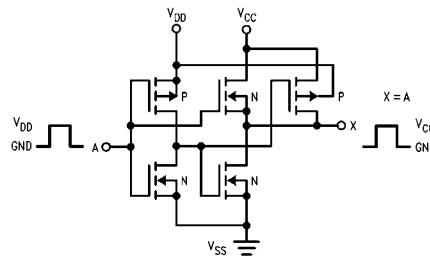
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Top View

Schematic Diagram



Hex COS/MOS to DTL or TTL converter (inverting).
Connect V_{CC} to DTL or TTL supply.
Connect V_{DD} to COS/MOS supply.

Absolute Maximum Ratings(Note 1)

Voltage at Any Pin (Note 2)	$V_{SS} - 0.3V$ to $V_{SS} + 15.5V$
Operating Temperature Range	$-55^{\circ}C$ to $+125^{\circ}C$
Storage Temperature Range (T_S)	$-65^{\circ}C$ to $+150^{\circ}C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260 $^{\circ}C$
Operating Range (V_{DD})	$V_{SS} + 3V$ to $V_{SS} + 15V$

Note 1: "Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits."

Note 2: This device should not be connected to circuits with the power on because high transient voltage may cause permanent damage.

DC Electrical Characteristics

Symbol	Characteristics	Conditions	Limits						Units	
			$-55^{\circ}C$		$+25^{\circ}C$			$+125^{\circ}C$		
			Min	Max	Min	Typ	Max	Min		Max
I_{CC}	Quiescent Device	$V_{DD} = 5.0V$		0.3		0.01	0.3		20	μA
	Current	$V_{DD} = 10V$		0.5		0.01	0.5		30	
P_D	Quiescent Device	$V_{DD} = 5.0V$		1.5		0.05	1.5		100	μW
	Dissipation/Package	$V_{DD} = 10V$		5.0		0.1	5.0		300	
V_{OL}	Output Voltage	$V_{DD} = 5.0V$		0.01		0	0.01		0.05	V
	LOW Level	$V_{DD} = 10V$		0.01		0	0.01		0.05	
V_{OH}	Output Voltage	$V_{DD} = 5.0V$	4.99		4.99	5		4.95		V
	HIGH Level	$V_{DD} = 10V$	9.99		9.99	10		9.95		
V_{NL}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V, V_O \geq 1.5$	1.6		1.5	2.25		1.4		V
		$V_{DD} = 10V, V_O \geq 3.0$	3.2		3	4.5		2.9		
V_{NH}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V, V_O \geq 3.5$	1.4		1.5	2.25		1.5		V
		$V_{DD} = 10V, V_O \geq 7.0$	2.9		3	4.5		3		
I_{DN}	Output Drive Current	$V_{DD} = 5.0V, 0.4 = V_O$	3.75		3	4		2.1		mA
	N-Channel (Note 3)	$V_{DD} = 10V, 0.5 = V_O$	10		8	10		5.6		
I_{DP}	Output Drive Current	$V_{DD} = 5.0V, 2.5 = V_O$	-1.85		-1.25	-1.75		-0.9		mA
	P-Channel (Note 3)	$V_{DD} = 10V, 9.5 = V_O$	-0.9		-0.6	-0.8		-0.4		
I_I	Input Current					10				pA

Note 3: I_{DN} and I_{DP} are tested one output at a time.

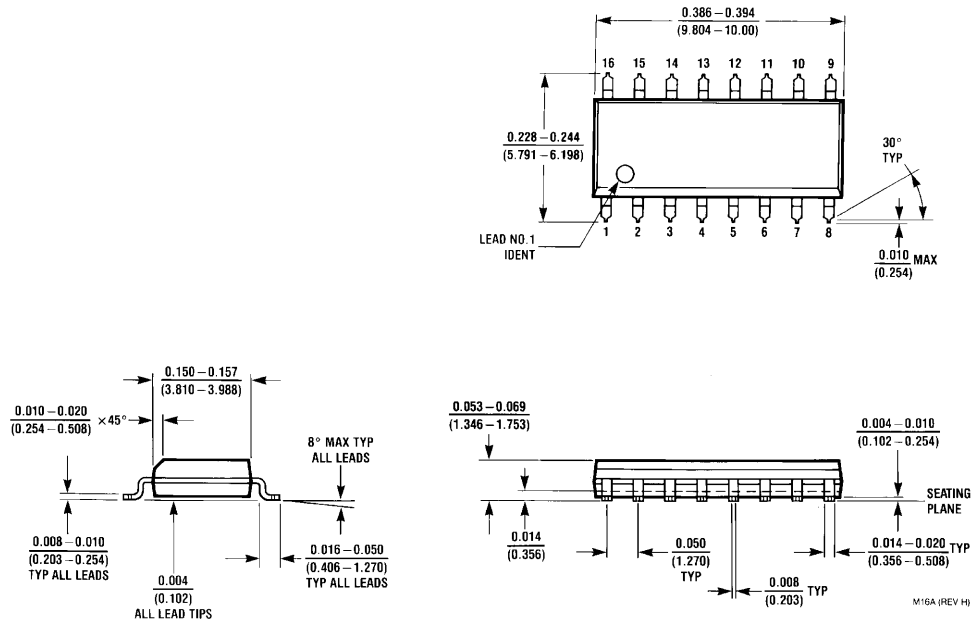
AC Electrical Characteristics (Note 4)							
T _A = 25°C, C _L = 15 pF, unless otherwise noted. Typical Temperature coefficient for all values of V _{DD} = 0.3%/°C							
Symbol	Characteristics	Test Conditions		Limits			Units
			V _{DD} (Volts)	Min	Typ	Max	
t _{PHL}	Propagation Delay Time:	V _{CC} = V _{DD}	5	—	15	70	ns
t _{PLH}	HIGH-to-LOW Level (t _{PHL})	V _{DD} = 10V V _{CC} = 5V	10	—	10	40	
	LOW-to-HIGH Level (t _{PLH})	V _{CC} = V _{DD}	5	—	50	100	ns
		V _{DD} = 10V V _{CC} = 5V	10	—	25	70	
t _{THL}	Transition Time:	V _{CC} = V _{DD}	5	—	20	60	ns
t _{TLH}	HIGH-to-LOW Level (t _{THL})	V _{CC} = V _{DD}	10	—	16	50	ns
	LOW-to-HIGH Level (t _{TLH})	V _{CC} = V _{DD}	5	—	80	160	ns
	Input Capacitance (C _I)	Any Input	10	—	50	120	pF
				—	5	—	

Note 4: AC Parameters are guaranteed by DC correlated testing.

Typical Application

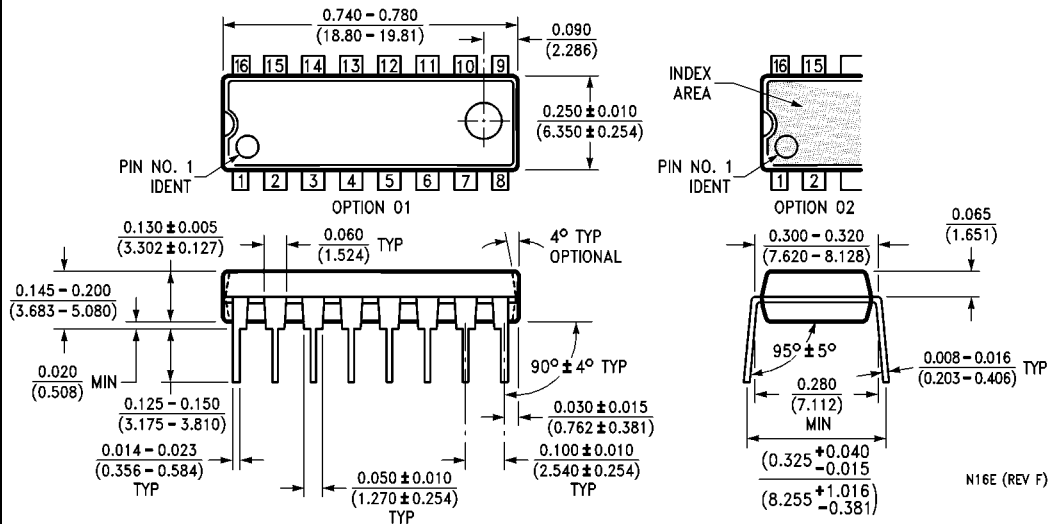
The diagram illustrates a typical application circuit. It features an inverter (represented by a triangle) and a TTL NAND gate (represented by a rectangle labeled 'TTL'). The inverter's input is connected to a signal source. Its output is connected to the input of the NAND gate. The inverter's V_{DD} pin is connected to a +5V supply, and its V_{CC} pin is connected to a common ground. The NAND gate's V_{CC} pin is connected to the +5V supply, and its V_{DD} pin is connected to the common ground. The output of the NAND gate is connected to a signal source.

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E**

N16E (REV F)

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