FAIRCHILD
SEMICONDUCTOR™

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74LVX163
Low Voltage Synchronous Binary Counter with Synchronous Clear

General Description

The LVX163 is a synchronous modulo-16 binary counter. This device is synchronously presettable for application in programmable dividers and has two types of Count Enable inputs plus a Terminal Count output for versatility in forming multistage counters. The CLK input is active on the rising edge. Both $\overline{PE}$ and $\overline{MR}$ inputs are active on low logic levels. Presetting is synchronous to rising edge of the CLK and the Clear function of the LVX163 is synchronous to the CLK. Two enable inputs (CEP and CET) and Carry Output are provided to enable easy cascading of counters, which facilitates easy implementation of n-bit counters without using external gates.

The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

Features

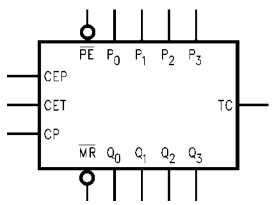
- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise and dynamic threshold performance

Ordering Code:

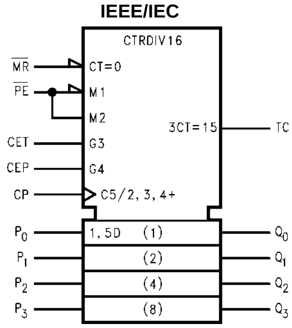
Order Number	Package Number	Package Description
74LVX163M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LVX163SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVX163MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

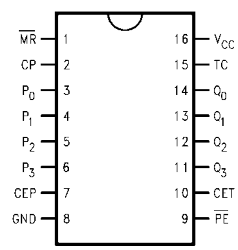
Logic Symbols



IEEE/IEC



Connection Diagram



Pin Descriptions

Pin Names	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input
$\overline{MR}$	Synchronous Master Reset Input
P_0–P_3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Inputs
Q_0–Q_3	Flip-Flop Outputs
TC	Terminal Count Output

Functional Description

The LVX163 counts in modulo-16 binary sequence. From state 15 (HHHH) it increments to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: synchronous reset, parallel load, count-up and hold. Four control inputs—Synchronous Reset ($\overline{MR}$), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The LVX163 uses D-type edge-triggered flip-flops and changing the $\overline{MR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways.

Figure 1 shows the connections for simple ripple carry, in which the clock period must be longer than the CP to $\overline{TC}$ delay of the first stage, plus the cumulative $\overline{CET}$ to $\overline{TC}$ delays of the intermediate stages, plus the $\overline{CET}$ to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry lookahead connections shown in *Figure 2* are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min in the Up mode, or min to max in the Down mode, to start its final cycle. Since this final cycle takes 16 clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock period is the CP to $\overline{TC}$ delay of the first stage plus the $\overline{CEP}$ to CP setup time of the last stage. The $\overline{TC}$ output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, registers or counters. When the Parallel Enable ($\overline{PE}$) is LOW, the parallel data outputs O_0–O_3 are active and follow the flip-flop Q outputs. A HIGH signal on $\overline{PE}$ forces O_0–O_3 to the High impedance state but does not prevent counting, loading or resetting.

Logic Equations: Count Enable = CEP • CET • $\overline{PE}$

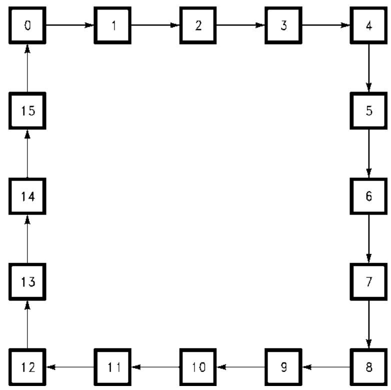
TC = $Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot$ CET

Mode Select Table

$\overline{MR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (_/‾)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
_/‾ = LOW-to-HIGH Clock Transition

State Diagram



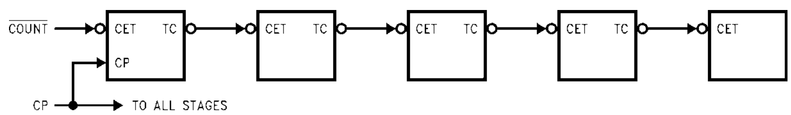


FIGURE 1.

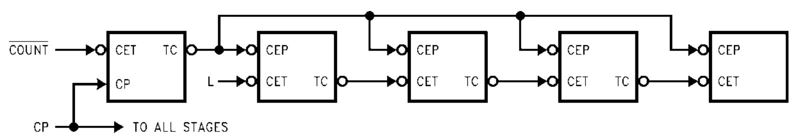
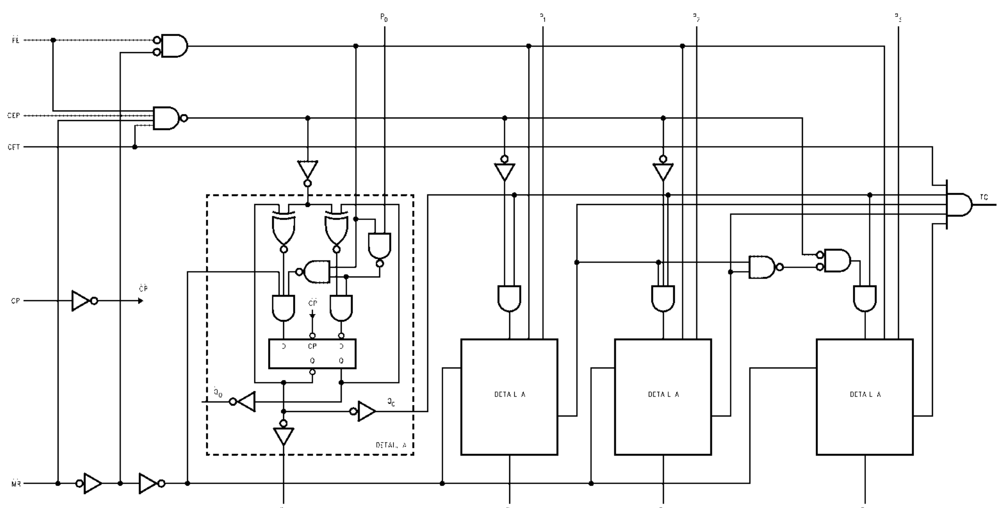


FIGURE 2.

Block Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
DC Input Voltage (V_I)	−0.5V to 7V
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation	180 mW

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time (Δt/Δv)	0 ns/V to 100 ns/V

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	HIGH Level Input Voltage	2.0	1.5			1.5		V		
		3.0	2.0			2.0				
		3.6	2.4			2.4				
V_{IL}	LOW Level Input Voltage	2.0			0.5		0.5	V		
		3.0			0.8		0.8			
		3.6			0.8		0.8			
V_{OH}	HIGH Level Output Voltage	2.0	1.9	2.0		1.9		V	$V_{IN} = V_{IL}$ or V_{IH}	$I_{OH} = -50$ µA
		3.0	2.9	3.0		2.9				$I_{OH} = -50$ µA
		3.0	2.58			2.48				$I_{OH} = -4$ mA
V_{OL}	LOW Level Output Voltage	2.0		0.0	0.1		0.1	V	$V_{IN} = V_{IL}$ or V_{IH}	$I_{OL} = 50$ µA
		3.0		0.0	0.1		0.1			$I_{OL} = 50$ µA
		3.0			0.36		0.44			$I_{OL} = 4$ mA
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	µA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	3.6			2.0		20.0	µA	$V_{IN} = V_{CC}$ or GND	

Noise Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$		Units	C_L (pF)
			Typ	Limits		
V_{OLP} (Note 3)	Quiet Output Maximum Dynamic V_{OL}	3.3	0.2	0.5	V	50
V_{OLV} (Note 3)	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.2	−0.5	V	50
V_{IHD} (Note 3)	Minimum HIGH Level Dynamic Input Voltage	3.3		2.0	V	50
V_{ILD} (Note 3)	Maximum LOW Level Dynamic Input Voltage	3.3		0.8	V	50

Note 3: Parameter guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40°C$ to $+85°C$ Min	$T_A = -40°C$ to $+85°C$ Max	Units	Conditions
t_{PLH}	Propagation Delay	2.7		9.0	14.0	1.0	16.0	ns	$C_L = 15$ pF
t_{PHL}	Time (CP–Q_n)			11.3	17.0	1.0	19.0		$C_L = 50$ pF
		3.3 ± 0.3		8.3	12.8	1.0	15.0	ns	$C_L = 15$ pF
				10.8	16.3	1.0	18.5		$C_L = 50$ pF
t_{PLH}	Propagation Delay	2.7		9.5	14.3	1.0	16.7	ns	$C_L = 15$ pF
t_{PHL}	Time (CP–TC, Count)			12.5	18.5	1.0	20.5		$C_L = 50$ pF
		3.3 ± 0.3		8.7	13.6	1.0	16.0	ns	$C_L = 15$ pF
				11.2	17.1	1.0	19.5		$C_L = 50$ pF
t_{PLH}	Propagation Delay	2.7		11.4	18.0	1.0	21.0	ns	$C_L = 15$ pF
t_{PHL}	Time (CP–TC, Load)			14.0	21.0	1.0	24.0		$C_L = 50$ pF
		3.3 ± 0.3		11.0	17.2	1.0	20.0	ns	$C_L = 15$ pF
				13.5	20.7	1.0	23.5		$C_L = 50$ pF
t_{PLH}	Propagation Delay	2.7		8.6	13.5	1.0	15.0	ns	$C_L = 15$ pF
t_{PHL}	Time (CET–TC)			11.0	16.5	1.0	18.5		$C_L = 50$ pF
		3.3 ± 0.3		7.5	12.3	1.0	14.5	ns	$C_L = 15$ pF
				10.5	15.8	1.0	18.0		$C_L = 50$ pF
f_{MAX}	Maximum Clock	2.7	75	115		65		MHz	$C_L = 15$ pF
	Frequency		50	80		45			$C_L = 50$ pF
		3.3 ± 0.3	80	130		70		MHz	$C_L = 15$ pF
			55	85		50			$C_L = 50$ pF
C_{IN}	Input Capacitance			4	10		10	pF	V_{CC} = Open
C_{PD}	Power Dissipation Capacitance			23				pF	(Note 4)

Note 4: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr) = C_{PD} * V_{CC} * f_{IN} + I_{CC}.

When the outputs drive a capacitive load, total current consumption is the sum of C_{PD}, and ΔI_{CC} which is obtained from the following formula:

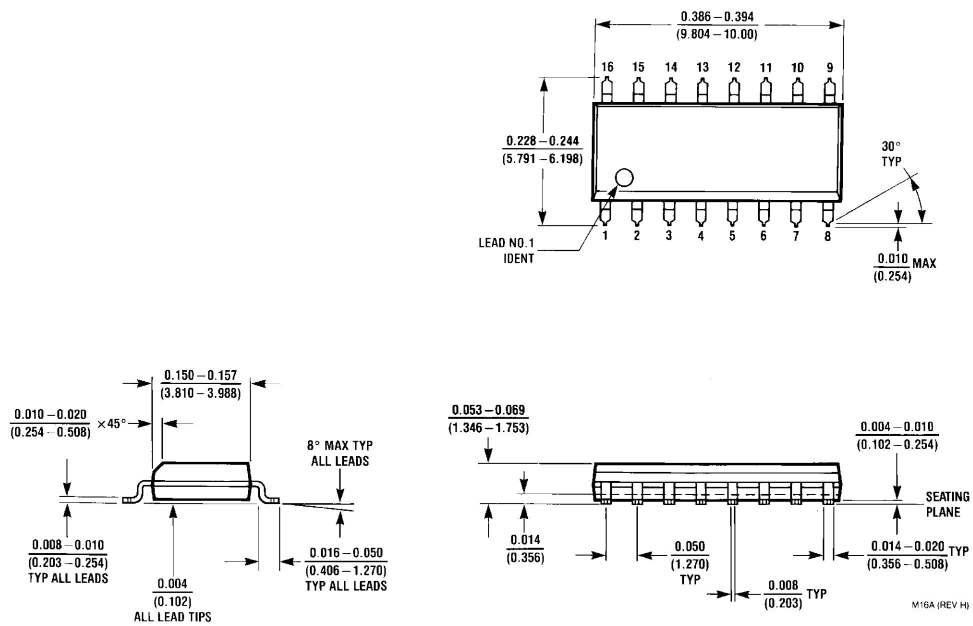
$$\Delta I_{CC} = F_{CP} \bullet V_{CC} \left(\frac{C_{Q0}}{2} + \frac{C_{Q1}}{4} + \frac{C_{Q2}}{8} + \frac{C_{Q3}}{16} + \frac{C_{TC}}{16} \right)$$

C_{Q0}–C_{Q3} and C_{TC} are the capacitances at Q0–Q3 and TC, respectively. F_{CP} is the input frequency of the CP.

AC Operating Requirements

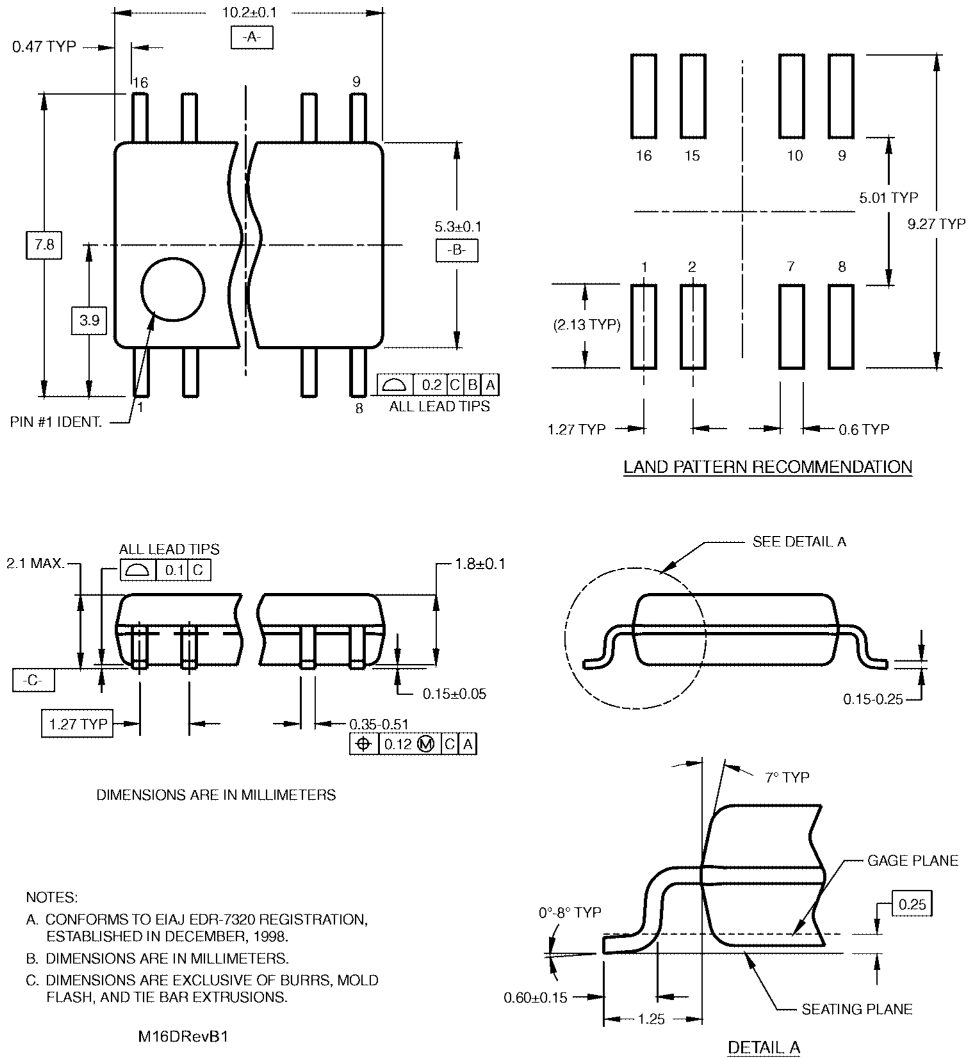
Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$	$T_A = -40°C$ to $+85°C$	Units
			Guaranteed Minimum		
t_S	Minimum Setup Time (P_n–CP)	2.7 3.3 ± 0.3	5.5 5.5	6.5 6.5	ns
t_S	Minimum Setup Time ($\overline{PE}$ –CP)	2.7 3.3 ± 0.3	8.0 8.0	9.5 9.5	ns
t_S	Minimum Setup Time (CEP or CET–CP)	2.7 3.3 ± 0.3	7.5 7.5	9.0 9.0	ns
t_S	Minimum Setup Time ($\overline{MR}$ –CP)	2.7 3.3 ± 0.3	4.0 4.0	4.0 4.0	ns
t_H	Minimum Hold Time (P_n–CP)	2.7 3.3 ± 0.3	1.0 1.0	1.0 1.0	ns
t_H	Minimum Hold Time ($\overline{PE}$ –CP)	2.7 3.3 ± 0.3	1.0 1.0	1.0 1.0	ns
t_H	Minimum Hold Time (CEP or CET–CP)	2.7 3.3 ± 0.3	1.0 1.0	1.0 1.0	ns
t_H	Minimum Hold Time ($\overline{MR}$ –CP)	2.7 3.3 ± 0.3	1.5 1.5	1.5 1.5	ns
t_W(L) t_W(H)	Minimum Pulse Width CP (Count)	2.7 3.3 ± 0.3	5.0 5.0	5.0 5.0	ns

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

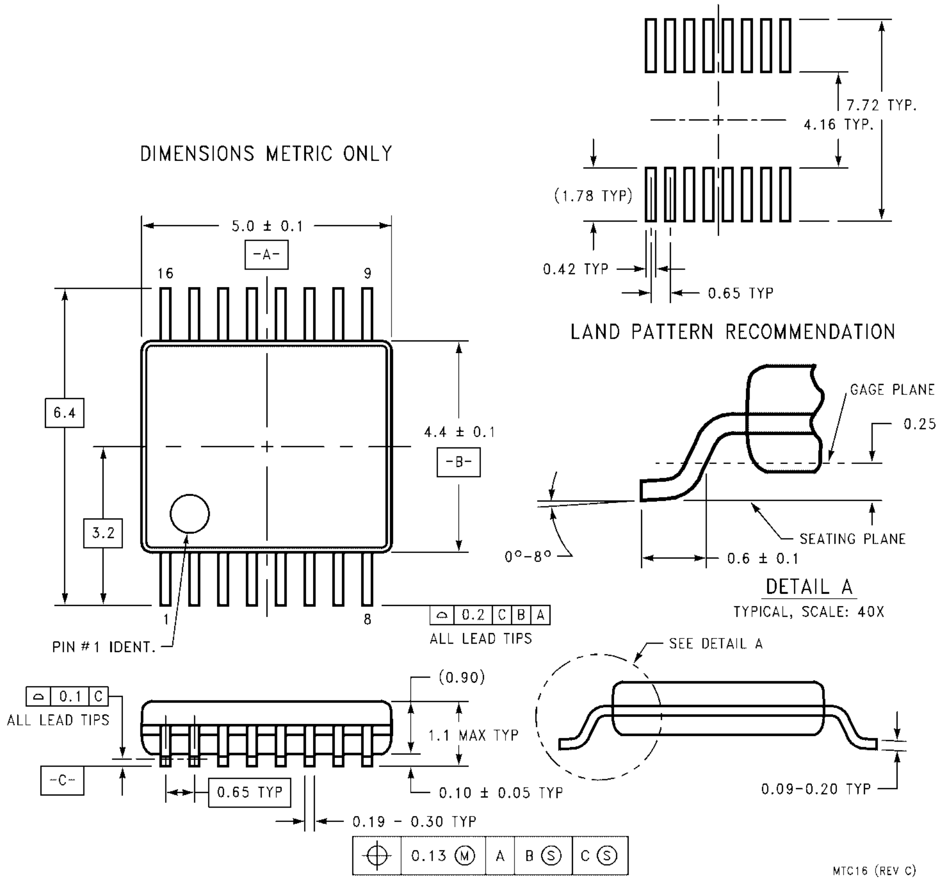
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1

16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

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