FAIRCHILD SEMICONDUCTOR™

February 1992
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74LVQ373
Low Voltage Octal Transparent Latch with 3-STATE Outputs

General Description

The LVQ373 consists of eight latches with 3-STATE outputs for bus organized system applications. The latches appear transparent to the data when Latch Enable (LE) is HIGH. When LE is low, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

Features

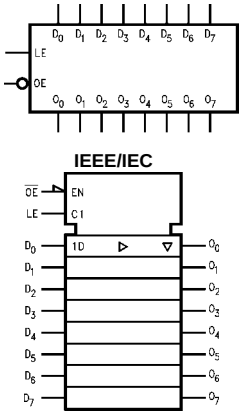
- Ideal for low power/low noise 3.3V applications
- Implements patented EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity

Ordering Code:

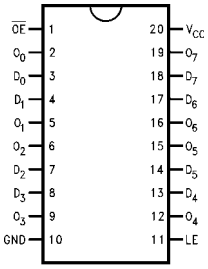
Order Number	Package Number	Package Description
74LVQ373SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LVQ373SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVQ373QSC	MQA20	20-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Pin Descriptions

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
O_0–O_7	3-STATE Latch Outputs

Truth Table

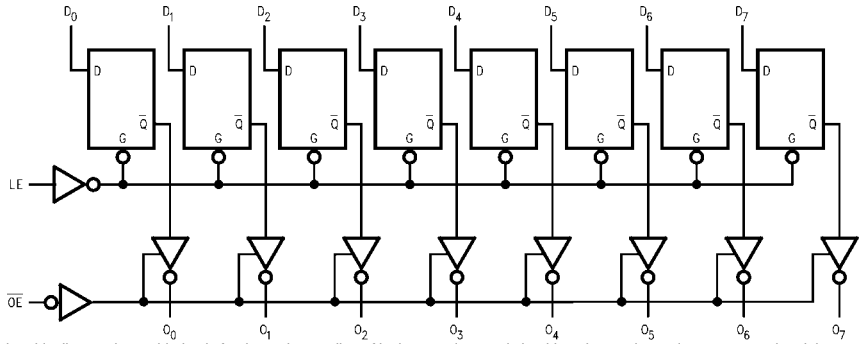
Inputs			Outputs
LE	$\overline{OE}$	D_n	O_n
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level L = LOW Voltage Level
Z = High Impedance X = Immaterial
O_0 = Previous O_0 before HIGH to Low transition of Latch Enable

Functional Description

The LVQ373 contains eight D-type latches with 3-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D-type input changes. When LE is LOW, the latches store the information that was present on the D-type inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±400 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate (ΔV/Δt)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = +25°C	T_A = −40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.58	2.48	V	V_{IN} = V_{IL} or V_{IH} (Note 3) I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.44	V	V_{IN} = V_{IL} or V_{IH} (Note 3) I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V_I = V_{CC}, GND
I_{OLD}	Minimum Dynamic Output Current (Note 4)	3.6			36	mA	V_{OLD} = 0.8V Max (Note 5)
I_{OHD}		3.6			−25	mA	V_{OHD} = 2.0V Min (Note 5)
I_{CC}	Maximum Quiescent Supply Current	3.6		4.0	40.0	μA	V_{IN} = V_{CC} or GND
I_{OZ}	Maximum 3-STATE Leakage Current	3.6		±0.25	±2.5	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.4	0.8		V	(Note 6)(Note 7)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.3	−0.8		V	(Note 6)(Note 7)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0		V	(Note 6)(Note 8)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8		V	(Note 6)(Note 8)

Note 3: All outputs loaded; thresholds on input associated with output under test.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

Note 5: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed.

Note 6: Worst case package.

Note 7: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 8: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PHL}	Propagation Delay	2.7	2.5	9.6	14.8	2.5	16.0	ns
t_{PLH}	D_n to O_n	3.3 ± 0.3	2.5	8.0	10.5	2.5	11.0	
t_{PLH}	Propagation Delay	2.7	2.5	9.6	16.9	2.5	18.0	ns
t_{PHL}	LE to O_n	3.3 ± 0.3	2.5	8.0	12.0	2.5	12.5	
t_{PZL}	Output Enable Time	2.7	2.5	10.2	18.3	2.5	19.0	ns
t_{PZH}		3.3 ± 0.3	2.5	8.5	13.0	2.5	13.5	
t_{PHZ}	Output Disable Time	2.7	1.0	10.8	20.4	1.0	21.0	ns
t_{PLZ}		3.3 ± 0.3	1.0	9.0	14.5	1.0	15.0	
t_{OSHL}	Output to Output Skew	2.7		1.0	1.5		1.5	ns
t_{OSLH}	(Note 9)	3.3 ± 0.3		1.0	1.5		1.5	

Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements

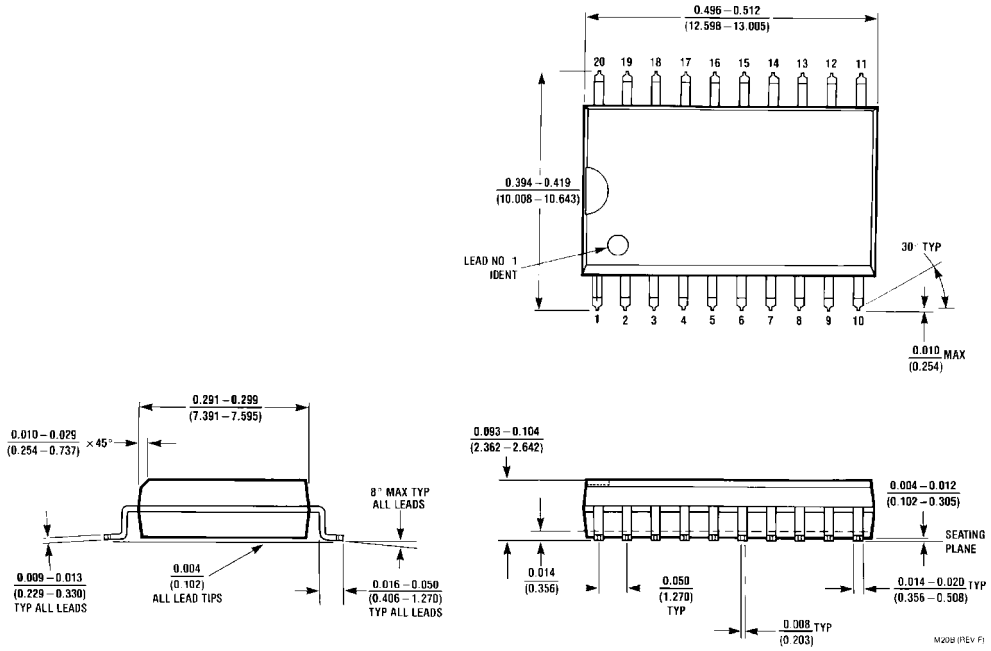
Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$, $C_L = 50$ pF		$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Typ	Guaranteed Minimum		
t_S	Setup Time,	2.7	0	4.0	4.5	ns
	HIGH or LOW	3.3 ± 0.3	0	3.0	3.0	
t_H	Hold Time,	2.7	0	1.5	1.5	ns
	HIGH or LOW	3.3 ± 0.3	0	1.5	1.5	
t_W	LE Pulse Width,	2.7	2.4	5.0	6.0	ns
	HIGH	3.3 ± 0.3	2.0	4.0	4.0	

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
C_{PD} (Note 10)	Power Dissipation Capacitance	39	pF	V_{CC} = 3.3V

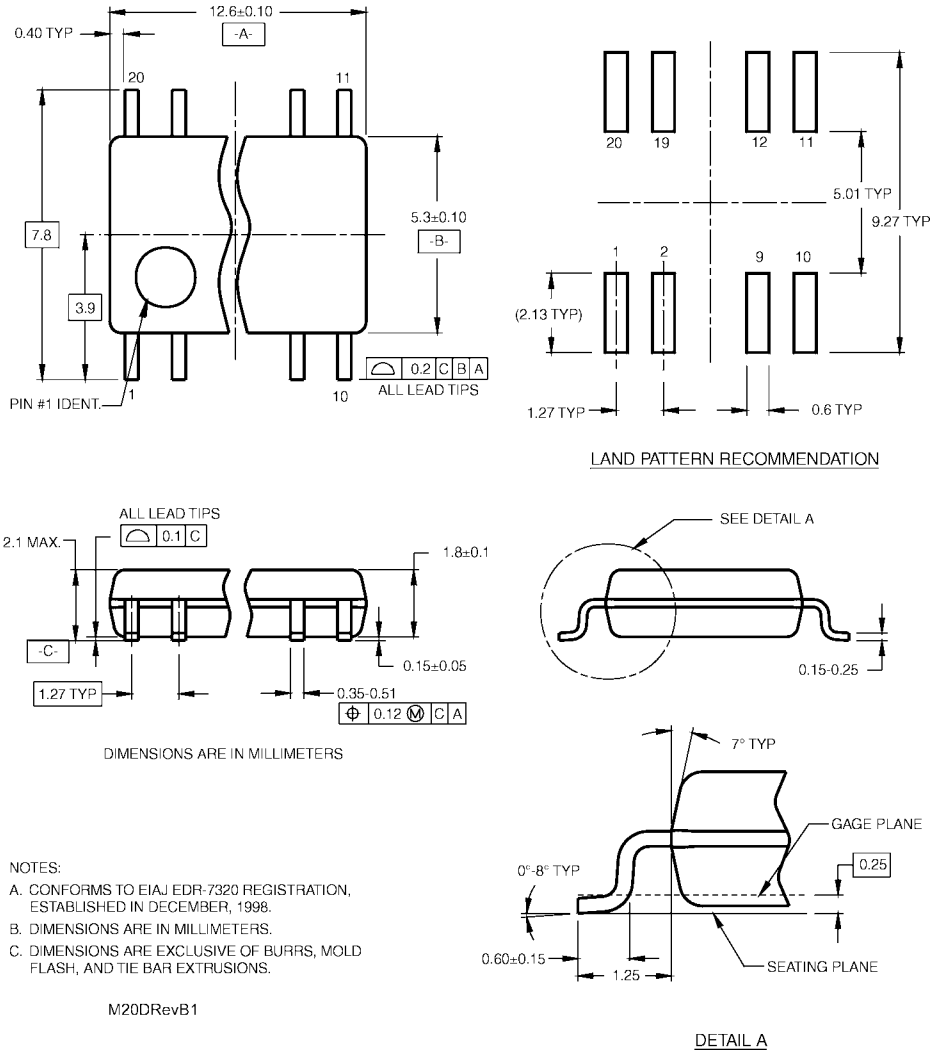
Note 10: C_{PD} is measured at 10 MHz.

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

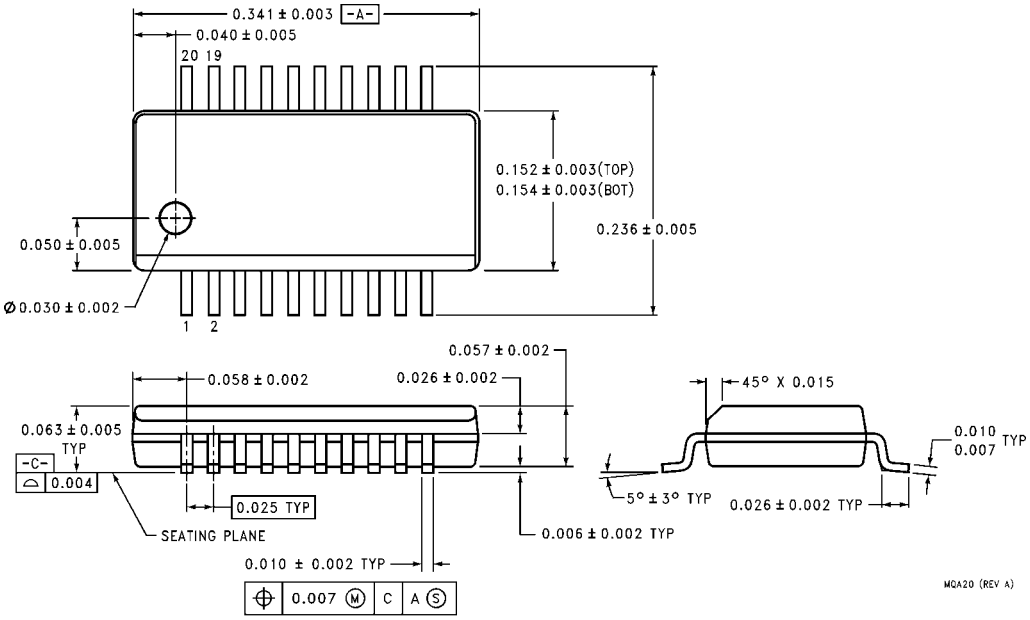
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide
Package Number MQA20