FAIRCHILD

SEMICONDUCTOR

74F899 9-Bit Latchable Transceiver with Parity Generator/Checker

General Description

The 74F899 is a 9-bit to 9-bit parity transceiver with transparent latches. The device can operate as a feed-through transceiver or it can generate/check parity from the 8-bit data busses in either direction. It has a guaranteed current sinking capability of 24 mA at the A-bus and 64 mA at the B-bus.

The 74F899 features independent latch enables for the A-to-B direction and the B-to-A direction, a select pin for ODD/EVEN parity, and separate error signal output pins for checking parity.

February 1989 Revised August 1999

Features

- Latchable transceiver with output sink of 24 mA at the A-bus and 64 mA at the B-bus
- Option to select generate parity and check or "feed-through" data/parity in directions A-to-B or B-to-A
- Independent latch enables for A-to-B and B-to-A directions
- Select pin for ODD/EVEN parity
- ERRA and ERRB output pins for parity checking
- Ability to simultaneously generate and check parity
- May be used in systems applications in place of the 74F543 and 74F280
- May be used in system applications in place of the 74F657 and 74F373 (no need to change T/R to check parity)

Ordering Code:

Order Number	Package Number	Package Description
74F899SC	M28B	28-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F899QC	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams



74F899

Input Loading/Fan-Out

		HIGH/LOW				
Pin Names	Description	U.L.	Input I _{IH} /I _{IL}			
		HIGH/LOW	Output I _{OH} /I _{OL}			
A ₀ -A ₇	Data Inputs/	1.0/1.0	20 µA/–0.6 mA			
	Data Outputs	150/40	–3 mA/24 mA			
B ₀ –B ₇	Data Inputs/	1.0/1.0	20 μA/–0.6 mA			
	Data Outputs	600/106.6	–12 mA/64 mA			
APAR	A Bus Parity	1.0/1.0	20 µA/–0.6 mA			
	Input/Output	150/40	–3 mA/24 mA			
BPAR	B Bus Parity	1.0/1.0	20 µA/–0.6 mA			
	Input/Output	600/106.6	–12 mA/64 mA			
ODD/EVEN	Parity Select Input	1.0/1.0	20 µA/–0.6 mA			
GBA, GAB	Output Enable Inputs	1.0/1.0	20 µA/–0.6 mA			
SEL	Mode Select Input	1.0/1.0	20 µA/–0.6 mA			
LEA, LEB	Latch Enable Inputs	1.0/1.0	20 μA/–0.6 mA			
ERRA, ERRB	Error Signal Outputs	50/33.3	–1 mA/20 mA			

Pin Descriptions

Pin Names	Description
A ₀ -A ₇	A Bus Data Inputs/Data Outputs
B ₀ -B ₇	B Bus Data Inputs/Data Outputs
APAR, BPAR	A and B Bus Parity Inputs
ODD/EVEN	ODD/EVEN Parity Select, Active LOW for EVEN Parity
GBA, GAB	Output Enables for A or B Bus, Active LOW
SEL	Select Pin for Feed-Through or Generate Mode, LOW for Generate Mode
LEA, LEB	Latch Enables for A and B Latches, HIGH for Transparent Mode
ERRA, ERRB	Error Signals for Checking Generated Parity with Parity In, LOW if Error Occurs

Functional Description

The 74F899 has three principal modes of operation which are outlined below. These modes apply to both the A-to-B and B-to-A directions.

- Bus A (B) communicates to Bus B (A), parity is generated and passed on to the B (A) Bus as BPAR (APAR). If LEB (LEA) is HIGH and the Mode Select (SEL) is LOW, the parity generated from B[0:7] (A[0:7]) can be checked and monitored by ERRB (ERRA).
- Bus A (B) communicates to Bus B (A) in a feed-through mode if <u>SEL</u> is HIGH. Parity is still generated and checked as ERRA and ERRB in the feed-through mode (can be used as an interrupt to signal a data/parity bit error to the CPU).
- Independent Latch Enables (LEA and LEB) allow other permutations of generating/checking (see Function Table).

Inputs			0					
GAB	GBA	SEL	LEA	LEB	Operation			
н	н	Х	Х	Х	Busses A and B are 3-STATE.			
Н	L	L	L	н	Generates parity from B[0:7] based on O/E (Note 1). Generated parity \rightarrow APAR. Generated parity checked against BPAR and output as ERRB.			
Н	L	L	Н	Н	Generates parity from B[0:7] based on O/ \overline{E} . <u>Gener</u> ated parity \rightarrow APAR. Generated parity checked against BPAR and output as <u>ERR</u> B. Generated parity also fed back through the A latch for generate/check as <u>ERRA</u> .			
Н	L	L	х	L	Generates parity from B latch data based on O/ \overline{E} . Generated parity \rightarrow APAR. Generated parity checked against latched BPAR and output as ERRB.			
Н	L	Н	Х	Н	BPAR/B[0:7] \rightarrow APAR/A0:7] Feed-through mode. Generated parity checked against BPAR and output as ERRB.			
Н	L	Н	Н	Н	$BPAR/B[0:7] \to APAR/A[0:7]$			
					Feed-through mode. Generated parity checked against BPAR and output as <u>ERRB</u> . Generated parity also fed back through the A latch for generate/check as <u>ERRA</u> .			
L	н	L	Н	L	Generates parity for A[0:7] based on O/ \overline{E} . Generated parity \rightarrow BPAR. Generated parity checked against APAR and output as ERRA.			
L	Н	L	Н	Н	Generates parity from A[0:7] based on O/\overline{E} . Generated parity \rightarrow BPAR. Generated parity checked against APAR and output as <u>ERR</u> A. Generated parity also fed back through the B latch for generate/check as ERRB.			
L	н	L	L	х	Generates parity from A latch data based on O/E. Generated parity \rightarrow BPAR. Generated parity checked against latched APAR and output as ERRA.			
L	Н	н	н	L	$APAR/A[0:7] \rightarrow BPAR/B[0:7]$			
					Feed-through mode. Generated parity checked against APAR and output as ERRA.			
L	н	н	н	н	$APAR/A[0:7] \rightarrow BPAR/B[0:7]$			
					Feed-through mode. Generated parity checked against APAR and output as <u>ERRA</u> . Generated parity also fed back through the B latch for generate/check as ERRB.			

H = HIGH Voltage Level Note 1: O/E = ODD/EVEN





74F899

74F899

Absolute Maximum Ratings(Note 2)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 3)	-0.5V to +7.0V
Input Current (Note 3)	-30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with $V_{CC} = 0V$)	
Standard Output	-0.5V to V _{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	Twice the Rated I _{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature Supply Voltage 0°C to +70°C +4.5V to +5.5V

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Parameter Min Typ Max Units			Units	V _{cc}	Conditions			
VIH	Input HIGH Voltage		2.0			V		Recognized as a			
								HIGH Signal			
V _{IL}	Input LOW Voltage				0.8	V		Recognized as a			
								LOW Signal			
V _{CD}	Input Clamp Diode Voltage				-1.2	V	Min	I _{IN} = -18 mA			
V _{OH}	Output HIGH	10% V _{CC}	2.5					$I_{OH} = -1 \text{ mA}$			
	Voltage	10% V _{CC}	2.4					$I_{OH} = -3 \text{ mA}$			
		10% V _{CC}	2.0			V		$I_{OH} = -15 \text{ mA} (B_n, \text{BPAR})$			
		5% V _{CC}	2.7					$I_{OH} = -1 \text{ mA}$			
		5% V_{CC}	2.7					$I_{OH} = -3 \text{ mA}$			
V _{OL}	Output LOW	10% V _{CC}			0.5			I _{OL} = 20 mA			
	Voltage							(A _n , APAR, ERRA, ERRB)			
		5% V _{CC}			0.55	V		I _{OL} = 24 mA			
								(A _n , APAR, ERRA, ERRB)			
		10% V _{CC}			0.55			I _{OL} = 64 mA (B _n , BPAR)			
V _{TH}	Input Threshold Voltage			1.45		V		± 0.1 V, Sweep Edge Rate must be > 1V/50 ns			
V _{OLV}	Negative Ground Bo	-	1.0	1.0	V		Observed on "quiet" output during				
	Voltage			1.0				simultaneous switching of remaining outputs			
V _{OLP}	Positive Ground Bou		1.0		V		Observed on "quiet" output during				
	Voltage			1.0		v		simultaneous switching of remaining outputs			
IIL	Input Low Current				-0.6	mA	Max	V _{IN} = 0.5V			
IIH	Input HIGH				5.0		Мох	$V_{m} = 2.7V_{c}$			
	Current		0.0		μΛ	Max	VIN - 2.7 V				
I _{BVI}	Input HIGH Current			7.0		Max	V _{IN} = 7.0V				
	Breakdown Test				7.0	μΛ	Max	(ODD/EVEN, GBA, GAB, SEL, LEA, LEB)			
I _{BVIT}	Input HIGH Current		0.5	m۸	Ман	V _{IN} = 5.5V					
	Breakdown (I/O)			0.5	ШA	Wax	(A _n , B _n , A _{PAR} , B _{PAR})				
ICEX	Output HIGH			50	μА	Мах	Vour = Voo				
	Leakage Current				00	μη	Max	*001 - *00			
V _{ID}	Input Leakage	Input Leakage				V	0.0	I _{ID} = 1.9 μA			
	Test	4.75			v	0.0	All Other Pins Grounded				
I _{OD}	Output Leakage		3 75	μА	0.0	$V_{IOD} = 150 \text{ mV}$					
	Circuit Current				0.70	μη	0.0	All Other Pins Grounded			
IIL	Input Low Current				-0.6	mA	Max	V _{IN} = 0.5V			
I _{IH+}	Output Leakage Cur	rrent		70	uА	Max	$V_{I/O} = 2.7V$				
I _{OZH}	Current					p., .	max	(A _n , B _n , APAR, BPAR)			

DC Electrical Characteristics (Continued)

Symbol	Parameter	Min	Тур	Max	Units	v _{cc}	Conditions
I_{IL+}	Output Leakage			6E0		Мох	$V_{I/O} = 0.5V$
I _{OZL}	Current			-050	μΑ	IVIAX	(A _n , B _n , APAR, BPAR)
I _{OS}	Output Short-Circuit Current	-60		-150		Max	$V_{OUT} = 0V$
					mA		(A _n , APAR, ERRA, ERRB)
		-100		-225		Max	$V_{OUT} = 0V (B_n, BPAR)$
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	$V_{OUT} = 5.25V$
I _{CCH}	Power Supply Current		132	155	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current		178	210	mA	Max	$V_{O} = LOW, GAB = LOW,$
							$GBA = HIGH, V_{IL} = LOW$
I _{CCZ}	Power Supply Current		160	190	mA	Max	$V_0 = HIGH Z$

AC Electrical Characteristics

-			T _A = +25°C	;	$T_A = 0^{\circ}C$	to +70°C		
			V _{CC} = +5.0\	/	V _{cc} =	= + 5.0V		Figure
Symbol	Parameter		C _L = 50 pF		$C_L = 50 \text{ pF}$		Units	Number
		Min	Тур	Max	Min	Max	1	
t _{PLH}	Propagation Delay	4.0	7.5	13.0	4.0	14.0		Figure 4
t _{PHL}	A _n , APAR to B _n , BPAR	4.0	8.5	13.0	4.0	14.0	ns	Figure 1
t _{PLH}	Propagation Delay	7.5	12.0	17.0	7.5	18.0		Figure 2
t _{PHL}	A _n , B _n to BPAR, APAR	7.5	12.5	17.0	7.5	18.0	115	Figure 2
t _{PLH}	Propagation Delay	7.5	12.0	17.0	7.5	18.0		Figure 2
t _{PHL}	A _n , B _n to ERRA, ERRB	7.5	12.5	17.0	7.5	18.0	ns	Figure 3
t _{PLH}	Propagation Delay	4.5	7.5	11.0	4.5	12.0		
t _{PHL}	ODD/EVEN to ERRA, ERRB	4.5	8.0	11.0	4.5	12.0	ns	Figure 4
t _{PLH}	Propagation Delay	4.5	7.5	11.5	4.5	12.5		Figure 5
t _{PHL}	ODD/EVEN to APAR, BPAR	4.5	8.5	11.5	4.5	12.5	ns	
t _{PLH}	Propagation Delay	5.5	9.0	13.0	5.5	14.0		-
t _{PHL}	APAR, BPAR to ERRA, ERRB	5.5	9.5	13.0	5.5	14.0	ns	Figure 6
t _{PLH}	LEA/LEB to	9.5	13.0	17.5	7.5	18.0		_
t _{PHL}	ERRA /ERRB	9.7		17.5	7.5	18.0	ns	Figure 7
t _{PLH}	Propagation Delay	3.0	6.0	10.0	3.0	11.0		Figure 10
t _{PHL}	SEL to APAR, BPAR	3.0	7.0	10.0	3.0	11.0	ns	
t _{PLH}	Propagation Delay	3.5	7.0	10.0	3.5	11.0		-
t _{PHL}	LEB to A _n , APAR	3.5	8.0	10.0	3.5	11.0	ns	Figure 11
t _{PLH}	Propagation Delay	3.5	6.5	10.0	3.5	11.0		
t _{PHL}	LEA to B _n , BPAR	3.5	7.5	10.0	3.5	11.0	ns	Figure 11
t _{PZH}	Output Enable Time	1.0	4.5	10.0	1.0	11.0		
t _{PZL}	GBA or GAB to A _n ,	1.0	6.5	10.0	1.0	11.0	ns	Figure 8, Figure 9
	APAR or B _n , BPAR							r igure o
t _{PHZ}	Output Disable Time	1.0	4.0	7.0	1.0	8.0		
t _{PLZ}	GBA or GAB to A _n ,	1.0	4.0	7.0	1.0	8.0	ns	Figure 8,
	APAR or B _n , BPAR							riguie 5
t _S (H)	Setup Time, HIGH or LOW	5.0	1.6		5.0			Figure 12, Figure 13
t _S (L)	A _n , B _n to LEA, LEB	5.0	1.8		5.0		ns	
t _H (H)	Hold Time, HIGH or LOW	0	-1.7		0		ne	Figure 12, Figure 13
t _H (L)	A _n , B _n to LEA, LEB	0	-1.5		0		115	
t _W	Pulse Width for LEA, LEB	6.0	2.0		6.0		ns	Figure 14

74F899



6





8







