

March 1988 Revised October 2000

# 74F646 • 74F646B • 74F648 Octal Transceiver/Register with 3-STATE Outputs

### **General Description**

These devices consist of bus transceiver circuits with 3-STATE, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Control  $\overline{G}$  and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control  $\overline{G}$  is Active LOW. In the isolation mode (control  $\overline{G}$  HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

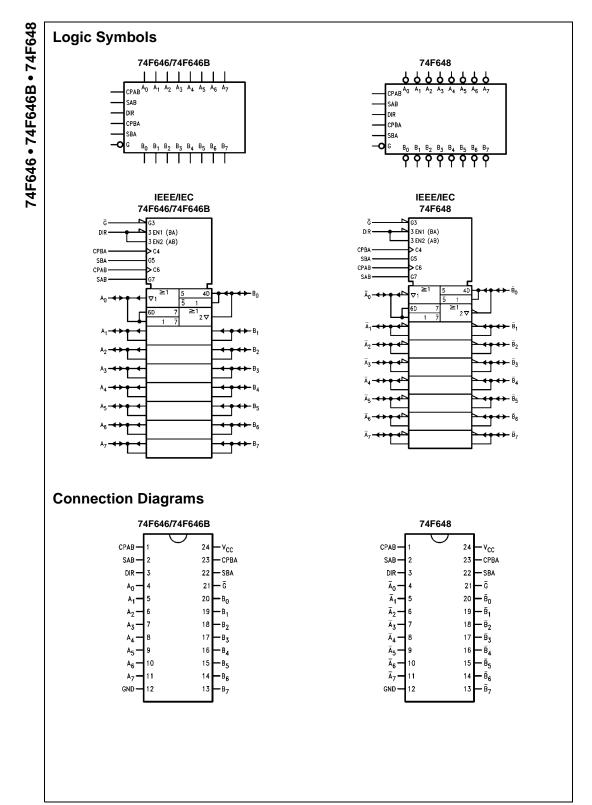
### **Features**

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- 74F648 has inverting data paths
- 74F646/74F646B have non-inverting data paths
- 74F646B is a faster version of the 74F646
- 3-STATE outputs
- 300 mil slim DIP

### **Ordering Code:**

Order Number	Package Number	Package Description
74F646SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F646MSA	MSA24	24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74F646SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
74F646BSC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F646BSPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
74F648SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F648SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.



# **Unit Loading/Fan Out**

Pin Names	Description	U.L.	Input I <sub>IH</sub> /I <sub>IL</sub>
Pin Names	Description	HIGH/LOW	Output I <sub>OH</sub> /I <sub>OL</sub>
A <sub>0</sub> -A <sub>7</sub>	Data Register A Inputs/	3.5/1.083	70 μΑ/–650 μΑ
	3-STATE Outputs	600/106.6 (80)	-12 mA/64 mA (48 mA)
B <sub>0</sub> -B <sub>7</sub>	Data Register B Inputs/	3.5/1.083	70 μΑ/–650 μΑ
	3-STATE Outputs	600/106.6 (80)	-12 mA/64 mA (48 mA)
CPAB, CPBA	Clock Pulse Inputs	1.0/1.0	20 μA/–0.6 mA
SAB, SBA	Select Inputs	1.0/1.0	20 μA/–0.6 mA
G	Output Enable Input	1.0/1.0	20 μA/–0.6 mA
DIR	Direction Control Input	1.0/1.0	20 μA/–0.6 mA

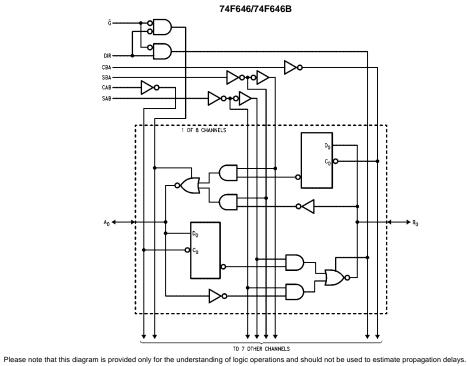
### **Function Table**

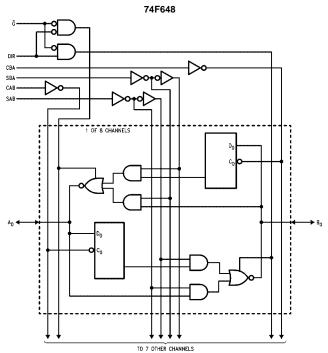
Inputs						Data I/O	(Note 1)	Francisco
G	DIR	СРАВ	СРВА	SAB	SBA	A <sub>0</sub> -A <sub>7</sub>	B <sub>0</sub> -B <sub>7</sub>	Function
Н	Χ	H or L	H or L	Х	Χ			Isolation
Н	Χ	~	X	Χ	X	Input	Input	Clock A <sub>n</sub> Data into A Register
Н	Χ	Χ	~	Χ	Χ			Clock B <sub>n</sub> Data into B Register
L	Н	Х	Х	L	Χ			A <sub>n</sub> to B <sub>n</sub> —Real Time (Transparent Mode)
L	Н	~	X	L	X	Input	Output	Clock A <sub>n</sub> Data into A Register
L	Н	H or L	X	Н	Χ			A Register to B <sub>n</sub> (Stored Mode)
L	Н	_	Χ	Н	Χ			Clock A <sub>n</sub> Data into A Register and Output to B <sub>n</sub>
L	L	Х	Х	Χ	L			B <sub>n</sub> to A <sub>n</sub> —Real Time (Transparent Mode)
L	L	X	~	Χ	L	Output	Input	Clock B <sub>n</sub> Data into B Register
L	L	X	H or L	Χ	Н			B Register to A <sub>n</sub> (Stored Mode)
L	L	X	~	Χ	Н			Clock B <sub>n</sub> Data into B Register and Output to A <sub>n</sub>

Note 1: The data output functions may be enabled or disabled by various signals at the  $\overline{G}$  and DIR Inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Irrelevant
\( \sigma = LOW-to-HIGH Transition \)

## **Logic Diagrams**





Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

### **Absolute Maximum Ratings**(Note 2)

 $\begin{array}{ll} \mbox{Storage Temperature} & -65\mbox{°C to } +150\mbox{°C} \\ \mbox{Ambient Temperature under Bias} & -55\mbox{°C to } +125\mbox{°C} \\ \end{array}$ 

Junction Temperature under Bias  $-55^{\circ}$ C to  $+150^{\circ}$ C  $V_{CC}$  Pin Potential to Ground Pin -0.5V to +7.0V

Input Voltage (Note 3) -0.5V to +7.0V
Input Current (Note 3) -30 mA to +5.0 mA

Voltage Applied to Output

in HIGH State (with V<sub>CC</sub> = 0V)

 $\begin{array}{ll} \text{Standard Output} & -0.5 \text{V to V}_{\text{CC}} \\ \text{3-STATE Output} & -0.5 \text{V to +5.5 V} \end{array}$ 

Current Applied to Output

in LOW State (Max) twice the rated  $I_{OL}$  (mA) ESD Last Passing Voltage (Min) 4000V

# Recommended Operating Conditions

Free Air Ambient Temperature  $0^{\circ}$ C to  $+70^{\circ}$ C Supply Voltage +4.5V to +5.5V

**Note 2:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

### **DC Electrical Characteristics**

Symbol	Parameter	Min	Тур	Max	Units	v <sub>cc</sub>	Conditions	
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal	
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal	
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA (Non I/O Pins)	
V <sub>OH</sub>	Output HIGH 10% V <sub>CC</sub> Voltage	2.0			٧	Min	$I_{OH} = -15 \text{ mA } (A_n, B_n)$	
V <sub>OL</sub>	Output LOW 10% V <sub>CC</sub>							
VOL	Voltage			0.55	V	Min	$I_{OL} = 64 \text{ mA } (A_n, B_n)$	
I <sub>IH</sub>	Input HIGH							
	Current			5.0	μΑ	Max	V <sub>IN</sub> = 2.7V (Non I/O Pins)	
I <sub>BVI</sub>	Input HIGH Current			7.0	μА	Max	V <sub>IN</sub> = 7.0V (Non I/O Pins)	
	Breakdown Test			7.0	μΛ	IVICA	V <sub>IN</sub> = 7.00 (10011/011113)	
I <sub>BVIT</sub>	Input HIGH Current			0.5	mA	Max	$V_{IN} = 5.5V (A_n, B_n)$	
	Breakdown (I/O)			0.5	IIIA	IVIAX	$V_{\rm IN} = 3.3V (A_{\rm IN}, D_{\rm IN})$	
I <sub>CEX</sub>	Output HIGH			50	μА	Max	$V_{OUT} = V_{CC}$	
	Leakage Current			30	μΛ	IVICA	v001 – vCC	
V <sub>ID</sub>	Input Leakage	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA	
	Test	4.70				0.0	All Other Pins Grounded	
I <sub>OD</sub>	Output Leakage			3.75	μА	0.0	V <sub>IOD</sub> = 150 mV	
	Circuit Current			3.73	μΛ	0.0	All Other Pins Grounded	
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V (Non I/O Pins)	
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70	μΑ	Max	$V_{OUT} = 2.7V (A_n, B_n)$	
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			-650	μΑ	Max	$V_{OUT} = 0.5V (A_n, B_n)$	
Ios	Output Short-Circuit Current	-100		-225	mA	Max	V <sub>OUT</sub> = 0V	
I <sub>ZZ</sub>	Bus Drainage Test			500	μΑ	0.0V	V <sub>OUT</sub> = 5.25V	
I <sub>CCH</sub>	Power Supply Current			135	mA	Max	V <sub>O</sub> = HIGH	
I <sub>CCL</sub>	Power Supply Current			150	mA	Max	$V_O = LOW$	
I <sub>CCZ</sub>	Power Supply Current			150	mA	Max	$V_O = HIGH Z$	

### **AC Electrical Characteristics** 74F646/74F648

		$T_A =$	+25°C	$T_A = -55^{\circ}C$	C to +125°C	$T_A = 0$ °C to +70°C		Units
Symbol	Parameter	V <sub>CC</sub> =	+ <b>5.0V</b>	V <sub>CC</sub> =	+5.0V	V <sub>CC</sub> =		
Symbol	Falantee	C <sub>L</sub> =	50 pF	$C_L =$	50 pF	$C_L = 50 \text{ pF}$		
		Min	Max	Min	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency	90		75		90		MHz
t <sub>PLH</sub>	Propagation Delay	2.0	7.0	2.0	8.5	2.0	8.0	ns
t <sub>PHL</sub>	Clock to Bus	2.0	8.0	2.0	9.5	2.0	9.0	115
t <sub>PLH</sub>	Propagation Delay	1.0	7.0	1.0	8.0	1.0	7.5	no
t <sub>PHL</sub>	Bus to Bus (74F646)	1.0	6.5	1.0	8.0	1.0	7.0	ns
t <sub>PLH</sub>	Propagation Delay	2.0	8.5	1.0	10.0	2.0	9.0	no
t <sub>PHL</sub>	Bus to Bus (74F648)	1.0	7.5	1.0	9.0	1.0	8.0	ns
t <sub>PLH</sub>	Propagation Delay	2.0	8.5	2.0	11.0	2.0	9.5	ns
t <sub>PHL</sub>	SBA or SAB to A or B	2.0	8.0	2.0	10.0	2.0	9.0	115
t <sub>PZH</sub>	Enable Time	2.0	8.5	2.0	10.0	2.0	9.0	ns
t <sub>PZL</sub>	OE to A or B	2.0	12.0	2.0	13.5	2.0	12.5	115
t <sub>PHZ</sub>	Disable Time	1.0	7.5	1.0	9.0	1.0	8.5	ns
t <sub>PLZ</sub>	OE to A or B	2.0	9.0	2.0	11.0	2.0	9.5	115
t <sub>PZH</sub>	Enable Time	2.0	14.0	2.0	16.0	2.0	15.0	
t <sub>PZL</sub>	DIR to A or B	2.0	13.0	2.0	15.0	2.0	14.0	ns
t <sub>PHZ</sub>	Disable Time	1.0	9.0	1.0	10.0	1.0	9.5	ns
t <sub>PLZ</sub>	DIR to A or B	2.0	11.0	2.0	12.0	2.0	11.5	115

## AC Operating Requirements 74F646/74F648

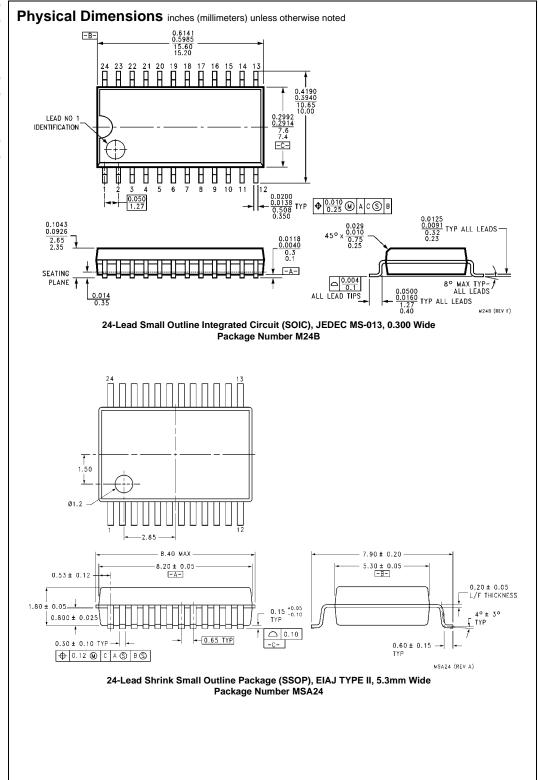
Symbol Parameter		$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$			to +125°C +5.0V	$T_A = 0$ °C to +70°C $V_{CC} = +5.0V$		Units
		Min	Max	Min	Max	Min	Max	
t <sub>S</sub> (H)	Setup Time, HIGH or LOW	5.0		5.0		5.0		
t <sub>S</sub> (L)	Bus to Clock	5.0		5.0		5.0		ns
t <sub>H</sub> (H)	Hold Time, HIGH or LOW	2.0		2.5		2.0		no
t <sub>H</sub> (L)	Bus to Clock	2.0		2.5		2.0		ns
t <sub>W</sub> (H)	Clock Pulse Width	5.0		5.0		5.0		
$t_W(L)$	HIGH or LOW	5.0		5.0		5.0		ns

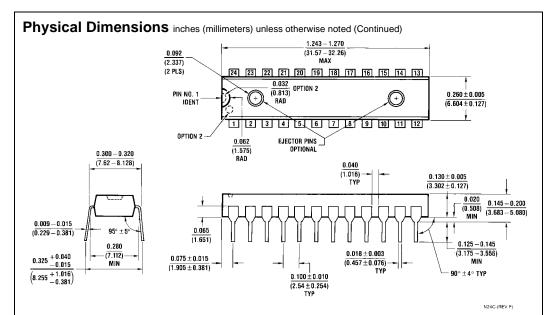
### **AC Electrical Characteristics 74F646B**

		I <sub>A</sub> = +25°C		; to +125°C	$I_A = 0$ °C			
Parameter	V <sub>CC</sub> =	+ <b>5.0V</b>	V <sub>CC</sub> =	+5.0V	V <sub>CC</sub> =	Units		
	C <sub>L</sub> =	50 pF	$C_L =$	50 pF	$C_L = 50 pF$			
	Min	Max	Min	Max	Min	Max		
Maximum Clock Frequency	165				150		MHz	
Propagation Delay	2.5	7.0			2.5	8.0	ns	
Clock to Bus	3.0	7.5			3.0	8.0		
Propagation Delay	2.0	6.0			2.0	7.0	ns	
Bus to Bus	2.0	6.0			2.0	7.0	115	
Propagation Delay	2.5	7.5			2.5	8.5	ns	
SBA or SAB to A or B	2.5	7.5			2.5	8.5		
Enable Time	2.5	6.5			2.5	8.0		
OE to A or B	2.5	9.0			2.5	10.0	ns	
Disable Time	1.5	6.5			1.5	7.5		
OE to A or B	2.0	7.0			2.0	8.5	ns	
Enable Time	2.0	7.0			2.0	8.5	no	
DIR to A or B	3.0	9.5			3.0	10.0	ns	
Disable Time	1.5	7.5			1.5	8.5	no	
DIR to A or B	2.5	8.5			2.5	9.5	ns	
	Maximum Clock Frequency Propagation Delay Clock to Bus Propagation Delay Bus to Bus Propagation Delay SBA or SAB to A or B Enable Time OE to A or B Disable Time OE to A or B Enable Time OE to A or B Enable Time OE to A or B Disable Time DIR to A or B Disable Time	Parameter           C <sub>L</sub> =           Min           Maximum Clock Frequency         165           Propagation Delay         2.5           Clock to Bus         3.0           Propagation Delay         2.0           Bus to Bus         2.5           Propagation Delay         2.5           SBA or SAB to A or B         2.5           Enable Time         2.5           Disable Time         1.5           OE to A or B         2.0           Enable Time         2.0           DIR to A or B         3.0           Disable Time         1.5	C <sub>L</sub> = 50 pF           Min         Max           Maximum Clock Frequency         165           Propagation Delay         2.5         7.0           Clock to Bus         3.0         7.5           Propagation Delay         2.0         6.0           Bus to Bus         2.0         6.0           Propagation Delay         2.5         7.5           SBA or SAB to A or B         2.5         7.5           Enable Time         2.5         6.5           OE to A or B         2.5         9.0           Disable Time         1.5         6.5           OE to A or B         2.0         7.0           Enable Time         2.0         7.0           DIR to A or B         3.0         9.5           Disable Time         1.5         7.5	Parameter         C <sub>L</sub> = 50 pF         C <sub>L</sub> =           Min         Max         Min           Maximum Clock Frequency         165           Propagation Delay         2.5         7.0           Clock to Bus         3.0         7.5           Propagation Delay         2.0         6.0           Bus to Bus         2.0         6.0           Propagation Delay         2.5         7.5           SBA or SAB to A or B         2.5         7.5           Enable Time         2.5         6.5           OE to A or B         2.5         9.0           Disable Time         1.5         6.5           OE to A or B         2.0         7.0           Enable Time         2.0         7.0           DIR to A or B         3.0         9.5           Disable Time         1.5         7.5	Parameter         C <sub>L</sub> = 50 pF         C <sub>L</sub> = 50 pF           Min         Max         Min         Max           Maximum Clock Frequency         165         Propagation Delay           Propagation Delay         2.5         7.0           Bus to Bus         2.0         6.0           Propagation Delay         2.5         7.5           SBA or SAB to A or B         2.5         7.5           Enable Time         2.5         6.5           OE to A or B         2.5         9.0           Disable Time         1.5         6.5           OE to A or B         2.0         7.0           Enable Time         2.0         7.0           DIR to A or B         3.0         9.5           Disable Time         1.5         7.5	Parameter         C <sub>L</sub> = 50 pF         C <sub>L</sub> = 50 pF		

# AC Operating Requirements 74F646B

Symbol Parameter		$T_A = +25$ °C $V_{CC} = +5.0$ V		l ''	to +125°C +5.0V	$T_A = 0$ °C to +70°C $V_{CC} = +5.0V$		Units
		Min	Max	Min	Max	Min	Max	
t <sub>S</sub> (H)	Setup Time, HIGH or LOW	5.0				4.0		
t <sub>S</sub> (L)	Bus to Clock	5.0				4.0		ns
t <sub>H</sub> (H)	Hold Time, HIGH or LOW	1.5				1.5		no
t <sub>H</sub> (L)	Bus to Clock	1.5				1.5		ns
t <sub>W</sub> (H)	Clock Pulse Width	5.0				5.0		ns
t <sub>W</sub> (L)	HIGH or LOW	5.0				5.0		115





24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N24C

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