

74F640 • 74F645

Octal Bus Transceiver with 3-STATE Outputs

General Description

These devices are octal bus transceivers designed for asynchronous two-way data flow between the A and B busses. Both busses are capable of sinking 64 mA, have 3-STATE outputs, and a common output enable pin. The direction of data flow is determined by the transmit/receive ($\overline{T/R}$) input. The 74F645 is a high speed/low power version of the 74F245. The 74F640 is an inverting option of the 74F645.

Features

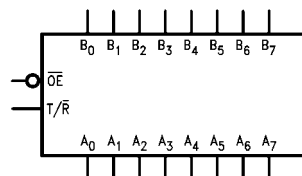
- Designed for asynchronous two-way data flow between busses
- Outputs sink 64 mA
- Transmit/receive ($\overline{T/R}$) input controls the direction of data flow
- 74F645 is a lower power, faster version of the 74F245
- 74F640 is an inverting option of the 74F645

Ordering Code:

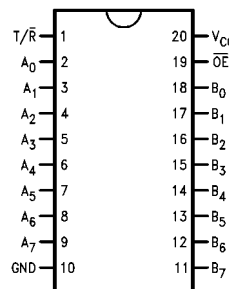
| Order Number | Package Number | Package Description |
|--------------|----------------|---------------------------------------------------------------------------|
| 74F640SC | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide |
| 74F640PC | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |
| 74F645PC | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



74F640 • 74F645 Octal Bus Transceiver with 3-STATE Outputs

Unit Loading/Fan Out

| Pin Names | Description | U.L. HIGH/LOW | Input I_{IH}/I_{IL} Output I_{OH}/I_{OL} |
|------------------|-------------------------------------|------------------------|-------------------------------------------------|
| \overline{OE} | Output Enable Input (Active LOW) | 1.0/1.0 | 20 μ A/–0.6 mA |
| T/\overline{R} | Transmit/Receive Input | 1.0/1.0 | 20 μ A/–0.6 mA |
| A_0 – A_7 | Side A Inputs or 3-STATE Outputs | 3.5/0.667 600/106.6 | 70 μ A/–0.4 mA –12 mA/64 mA |
| B_0 – B_7 | Side B Inputs or 3-STATE Outputs | 3.5/0.667 600/106.6 | 70 μ A/–0.4 mA –12 mA/64 mA |

Functional Description

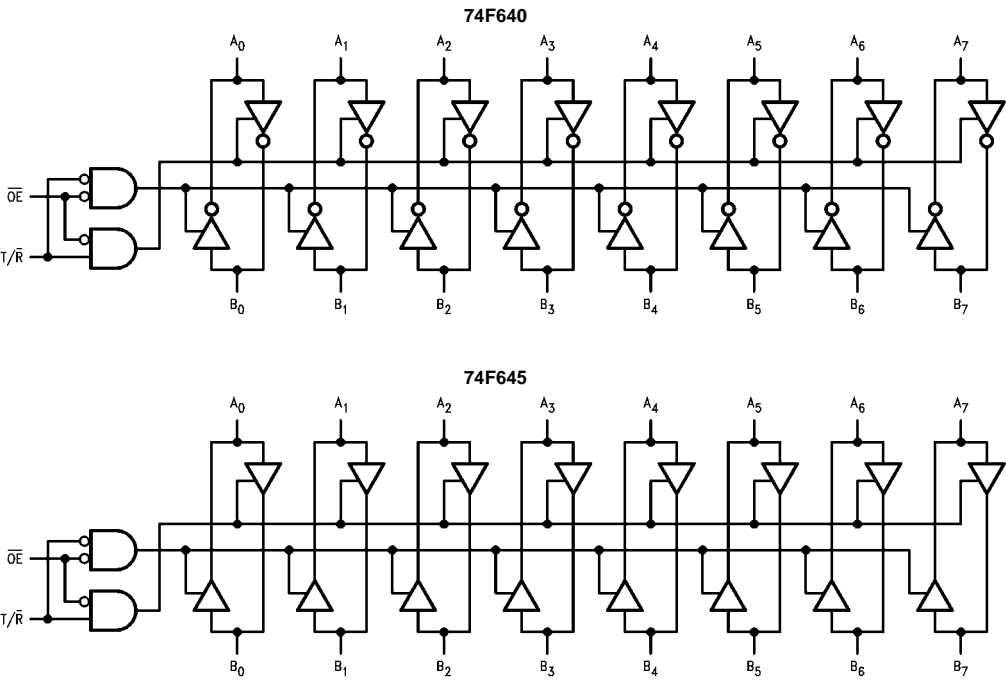
The output enable (\overline{OE}) is active LOW. If the device is disabled (\overline{OE} HIGH), the outputs are in the high impedance state. The transmit/receive input (T/\overline{R}) controls whether data is transmitted from the A bus to the B bus or from the B bus to the A bus. When T/\overline{R} is LOW, B data is sent to the A bus. If T/\overline{R} is HIGH, A data is sent to the B bus.

Function Table

| Inputs | | Outputs | |
|-----------------|------------------|----------------------------------|---------------------|
| \overline{OE} | T/\overline{R} | 74F640 | 74F645 |
| L | L | Bus \overline{B} data to Bus A | Bus B data to Bus A |
| L | H | Bus \overline{A} data to Bus B | Bus A data to Bus B |
| H | X | Z | Z |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance State

Logic Diagram



Absolute Maximum Ratings(Note 1)

| | |
|------------------------------------------------------------------------|--------------------------------------|
| Storage Temperature | –65°C to +150°C |
| Ambient Temperature under Bias | –55°C to +125°C |
| Junction Temperature under Bias | –55°C to +150°C |
| V _{CC} Pin Potential to Ground Pin | –0.5V to +7.0V |
| Input Voltage (Note 2) | –0.5V to +7.0V |
| Input Current (Note 2) | –30 mA to +5.0 mA |
| Voltage Applied to Output in HIGH State (with V _{CC} = 0V) | |
| Standard Output | –0.5V to V _{CC} |
| 3-STATE Output | –0.5V to +5.5V |
| Current Applied to Output in LOW State (Max) | twice the rated I _{OL} (mA) |
| ESD Last Passing Voltage (Min) | 4000V |

Recommended Operating Conditions

| | |
|------------------------------|----------------|
| Free Air Ambient Temperature | 0°C to +70°C |
| Supply Voltage | +4.5V to +5.5V |

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

| Symbol | Parameter | Min | Typ | Max | Units | V _{CC} | Conditions |
|------------------------------------|--------------------------------------------|------|-----|------|-------|-----------------|-------------------------------------------------------------|
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | | Recognized as a HIGH Signal |
| V _{IL} | Input LOW Voltage | | | 0.8 | V | | Recognized as a LOW Signal |
| V _{CD} | Input Clamp Diode Voltage | | | –1.2 | V | Min | I _{IN} = –18 mA (Non I/O Pins) |
| V _{OH} | Output HIGH Voltage 10% V _{CC} | 2.0 | | | V | Min | I _{OH} = –15 mA (A _n , B _n) |
| V _{OL} | Output LOW Voltage 10% V _{CC} | | | 0.55 | V | Min | I _{OL} = 64 mA (A _n , B _n) |
| I _{IH} | Input HIGH Current | | | 5.0 | μA | Max | V _{IN} = 2.7V (Non I/O Pins) |
| I _{BVI} | Input HIGH Current Breakdown Test | | | 7.0 | μA | Max | V _{IN} = 7.0V (Non I/O Pins) |
| I _{BVIT} | Input HIGH Current Breakdown (I/O) | | | 0.5 | mA | Max | V _{IN} = 5.5V (A _n , B _n) |
| I _{CEX} | Output HIGH Leakage Current | | | 50 | μA | Max | V _{OUT} = V _{CC} |
| V _{ID} | Input Leakage Test | 4.75 | | | V | 0.0 | I _{ID} = 1.9 μA All Other Pins Grounded |
| I _{OD} | Output Leakage Circuit Current | | | 3.75 | μA | 0.0 | V _{IOD} = 150 mV All Other Pins Grounded |
| I _{IL} | Input LOW Current | | | –0.6 | mA | Max | V _{IN} = 0.5V (Non I/O Pins) |
| I _{IH} + I _{OZH} | Output Leakage Current | | | 70 | μA | Max | V _{OUT} = 2.7V (A _n , B _n) |
| I _{IL} + I _{OZL} | Output Leakage Current | | | –650 | μA | Max | V _{OUT} = 0.5V (A _n , B _n) |
| I _{OS} | Output Short-Circuit Current | –100 | | –225 | mA | Max | V _{OUT} = 0V |
| I _{ZZ} | Bus Drainage Test | | | 500 | μA | 0.0V | V _{OUT} = 5.25 |
| I _{CCH} | Power Supply Current (74F640) | | | 80 | mA | Max | V _O = HIGH, V _{IN} = 0.2V |
| I _{CCL} | Power Supply Current (74F640) | | | 80 | mA | Max | V _O = LOW |
| I _{CCZ} | Power Supply Current (74F640) | | | 96 | mA | Max | V _O = HIGH Z |
| I _{CCH} | Power Supply Current (74F645) | | | 65 | mA | Max | V _O = HIGH |
| I _{CCL} | Power Supply Current (74F645) | | | 80 | mA | Max | V _O = LOW, V _{IN} = 0.2V |
| I _{CCZ} | Power Supply Current (74F645) | | | 90 | mA | Max | V _O = HIGH Z |

AC Electrical Characteristics 74F640

| Symbol | Parameter | $T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$ | | | $T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$ | | Units |
|-----------|------------------------------------------|--------------------------------------------------------------------------------|-----|-----|------------------------------------------------------------------------------------------------------|-----|-------|
| | | Min | Typ | Max | Min | Max | |
| t_{PLH} | Propagation Delay | 2.5 | | 7.5 | 2.0 | 8.0 | ns |
| t_{PHL} | A Input to B Output | 2.0 | | 7.0 | 2.0 | 7.0 | |
| t_{PLH} | Propagation Delay | 2.5 | | 7.5 | 2.0 | 8.0 | ns |
| t_{PHL} | B Input to A Output | 2.0 | | 7.0 | 2.0 | 7.0 | |
| t_{PZH} | Enable Time | 2.5 | | 7.5 | 2.0 | 9.0 | ns |
| t_{PZL} | $\overline{\text{OE}}$ Input to A Output | 2.5 | | 8.0 | 2.0 | 8.5 | |
| t_{PHZ} | Disable Time | 1.5 | | 7.0 | 1.0 | 7.5 | ns |
| t_{PLZ} | $\overline{\text{OE}}$ Input to A Output | 1.5 | | 6.0 | 1.5 | 6.0 | |
| t_{PZH} | Enable Time | 2.5 | | 7.5 | 2.0 | 9.0 | ns |
| t_{PZL} | $\overline{\text{OE}}$ Input to B Output | 2.5 | | 8.0 | 2.0 | 8.5 | |
| t_{PHZ} | Disable Time | 1.5 | | 7.0 | 1.0 | 7.5 | ns |
| t_{PLZ} | $\overline{\text{OE}}$ Input to B Output | 1.5 | | 6.0 | 1.5 | 6.0 | |

AC Electrical Characteristics 74F645

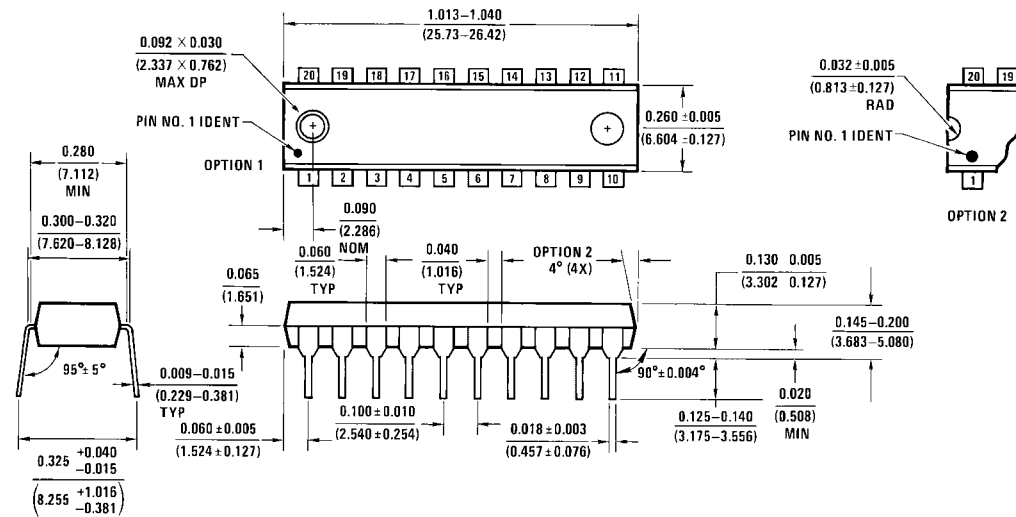
| Symbol | Parameter | $T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$ | | | $T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$ | | Units |
|-----------|------------------------------------------|--------------------------------------------------------------------------------|-----|-----|------------------------------------------------------------------------------------------------------|-----|-------|
| | | Min | Typ | Max | Min | Max | |
| t_{PLH} | Propagation Delay | 1.5 | | 6.0 | 1.5 | 7.0 | ns |
| t_{PHL} | A Input to B Output | 2.0 | | 7.0 | 2.0 | 7.5 | |
| t_{PLH} | Propagation Delay | 1.5 | | 6.0 | 1.5 | 7.0 | ns |
| t_{PHL} | B Input to A Output | 2.0 | | 7.0 | 2.0 | 7.5 | |
| t_{PZH} | Enable Time | 2.5 | | 8.0 | 2.0 | 9.0 | ns |
| t_{PZL} | $\overline{\text{OE}}$ Input to A Output | 2.5 | | 8.5 | 2.0 | 8.5 | |
| t_{PHZ} | Disable Time | 1.5 | | 7.0 | 1.0 | 8.0 | ns |
| t_{PLZ} | $\overline{\text{OE}}$ Input to A Output | 1.0 | | 5.5 | 1.0 | 5.5 | |
| t_{PZH} | Enable Time | 2.5 | | 7.5 | 2.0 | 9.5 | ns |
| t_{PZL} | $\overline{\text{OE}}$ Input to B Output | 2.5 | | 8.5 | 2.5 | 9.0 | |
| t_{PHZ} | Disable Time | 1.5 | | 6.5 | 1.0 | 7.5 | ns |
| t_{PLZ} | $\overline{\text{OE}}$ Input to B Output | 1.0 | | 5.5 | 1.0 | 5.5 | |

Physical Dimensions inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com