

April 1988 Revised October 2000

74F533

Octal Transparent Latch with 3-STATE Outputs

General Description

The 74F533 consists of eight latches with 3-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{\text{OE}}$) is LOW. When $\overline{\text{OE}}$ is HIGH the bus output is in the high impedance state. The 74F533 is the same as the 74F373, except that the outputs are inverted.

Features

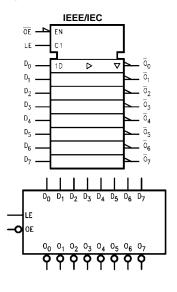
- Eight latches in a single package
- 3-STATE outputs for bus interfacing
- Inverted version of the 74F373

Ordering Code:

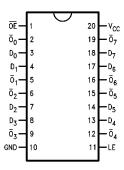
Order Number	Package Number	Package Description
74F533SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F533SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F533PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L.	Input I _{IH} /I _{IL}		
	Description	HIGH/LOW	Output I _{OH} /I _{OL}		
D ₀ -D ₇	Data Inputs	1.0/1.0	20 μA/-0.6 mA		
LE	Latch Enable Input (Active HIGH)	1.0/1.0	20 μA/-0.6 mA		
ŌĒ	Output Enable Input (Active LOW)	1.0/1.0	20 μA/–0.6 mA		
$\overline{O}_0 - \overline{O}_7$	Complementary 3-STATE Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)		

Function Table

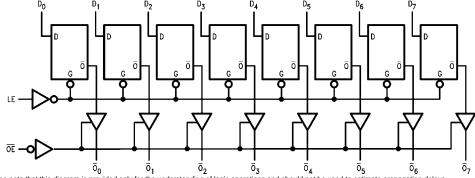
	Output		
LE	OE	D	ō
Н	L	Н	L
Н	L	L	Н
L	L	X	\overline{O}_0
Х	Н	X	Z

H = HIGH Voltage Level L = LOW Voltage Level

Functional Description

The 74F533 contains eight D-type latches with 3-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE buffers are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the buffers are in the bi-state mode. When $\overline{\text{OE}}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Recommended Operating Conditions

 $\begin{array}{ll} \mbox{Storage Temperature} & -65^{\circ}\mbox{C to } +150^{\circ}\mbox{C} \\ \mbox{Ambient Temperature under Bias} & -55^{\circ}\mbox{C to } +125^{\circ}\mbox{C} \\ \end{array}$

Junction Temperature under Bias —55°C to +150°C

V_{CC} Pin Potential to

 $\begin{tabular}{ll} Ground Pin & -0.5V to +7.0V \\ Input Voltage (Note 2) & -0.5V to +7.0V \\ Input Current (Note 2) & -30 mA to +5.0 mA \\ \end{tabular}$

Voltage Applied to Output in HIGH State (with V_{CC} = 0V)

 $\begin{array}{lll} \text{Standard Output} & -0.5 \text{V to V}_{\text{CC}} \\ \text{3-STATE Output} & -0.5 \text{V to +5.5V} \end{array}$

Current Applied to Output

in LOW State (Max) twice the rated I_{OL} (mA) ESD Last Passing Voltage (Min) 4000V

Free Air Ambient Temperature 0°C to +70°C Supply Voltage +4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

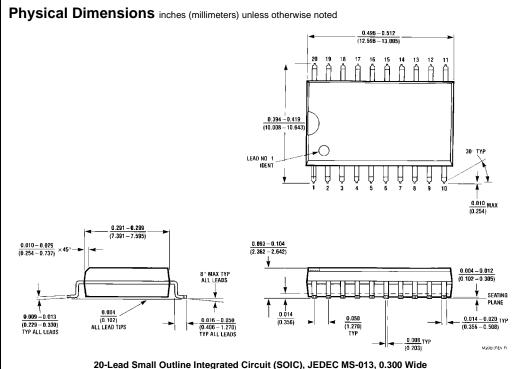
Symbol	Paramet	er	Min	Тур	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage				-1.2	V	Min	$I_{IN} = -18 \text{ mA}$
V _{OH}	Output HIGH 10% V _{CC}		2.5					I _{OH} = -1 mA
	Voltage	10% V _{CC}	2.4			V		$I_{OH} = -3 \text{ mA}$
		5% V _{CC}	2.7			V	Min	$I_{OH} = -1 \text{ mA}$
		5% V _{CC}	2.7					$I_{OH} = -3 \text{ mA}$
V _{OL}	Output LOW Voltage	10% V _{CC}			0.5	V	Min	I _{OL} = 24 mA
I _{IH}	Input HIGH Current				5.0	μΑ	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current				7.0			V 7.0V
	Breakdown Test				7.0	μΑ	Max	V _{IN} = 7.0V
I _{BVIT}	Input HIGH Current	GH Current			V 55V			
	Breakdown (I/O)				0.5	mA	Max	$V_{IN} = 5.5V$
I _{CEX}	Output HIGH							., .,
	Leakage Current				50	μΑ	Max	$V_{OUT} = V_{CC}$
V _{ID}	Input Leakage		4.75			.,		I _{ID} = 1.9 μA
	Test		4.75			V	0.0	All Other Pins Grounded
I _{OD}	Output Leakage				0.75		0.0	V _{IOD} = 150 mV
	Circuit Current			3.75	μА	0.0	All Other Pins Grounded	
I _{IL}	Input LOW Current				-0.6	mA	Max	V _{IN} = 0.5V
I _{OZH}	Output Leakage Currer	t			50	μΑ	Max	V _{OUT} = 2.7V
I _{OZL}	Output Leakage Currer	it			-50	μΑ	Max	V _{OUT} = 0.5V
I _{OS}	Output Short-Circuit Cu	rrent	-60		-150	mA	Max	V _{OUT} = 0V
I _{ZZ}	Bus Drainage Test				500	μА	0.0V	V _{OUT} = 5.25V
I _{CCZ}	Power Supply Current			41	61	mA	Max	V _O = HIGH Z

AC Electrical Characteristics

Symbol	Parameter	$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$			$T_A = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$		$T_A = 0$ °C to +70°C $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$		Units
		Min	Тур	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	4.0	6.7	9.0	4.0	12.0	4.0	10.0	
t _{PHL}	D_n to \overline{O}_n	2.5	4.4	7.0	2.5	9.0	2.5	8.0	ns
t _{PLH}	Propagation Delay	5.0	7.1	11.0	5.0	14.0	5.0	13.0	ns
t _{PHL}	LE to \overline{O}_n	3.0	4.7	7.0	3.0	9.0	3.0	8.0	115
t _{PZH}	Output Enable Time	2.0	5.9	10.0	2.0	12.5	2.0	11.0	
t _{PZL}		2.0	5.6	7.5	2.0	10.5	2.0	8.5	ns
t _{PHZ}	Output Disable Time	1.5	3.4	6.5	1.5	8.5	1.5	7.0	ns
t _{PLZ}		1.5	2.7	5.5	1.5	7.5	1.5	6.5	115

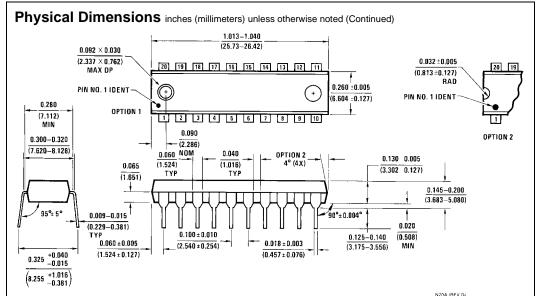
AC Operating Requirements

		$T_A = +25$ °C $V_{CC} = +5.0V$		$T_A = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = +5.0V$		$T_A = 0$ °C to +70°C $V_{CC} = +5.0V$		Units	
Symbol	Parameter								
		Min	Max	Min	Max	Min	Max		
t _S (H)	Setup Time, HIGH or LOW	2.0		2.0		2.0		ns	
t _S (L)	D _n to LE	2.0		2.0		2.0		115	
t _H (H)	Hold Time, HIGH or LOW	3.0		3.0		3.0		200	
t _H (L)	D _n to LE	3.0		3.0		3.0		ns	
t _W (H)	LE Pulse Width, HIGH	6.0		6.0		6.0		ns	



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 2.6±0.10 0.40 TYP -A-5.01 TYP 5.3±0.10 9.27 TYP 7.8 -B-3.9 0.2 C B A ALL LEAD TIPS 10 PIN #1 IDENT.-0.6 TYP 1.27 TYP -LAND PATTERN RECOMMENDATION ALL LEAD TIPS SEE DETAIL A 0.1 C 2.1 MAX. 1.8±0.1 L 0.15±0.05 0.15-0.25 -1.27 TYP 0.35-0.51 **♦** 0.12 **⋈** C A DIMENSIONS ARE IN MILLIMETERS GAGE PLANE 0.25 NOTES: A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998. B. DIMENSIONS ARE IN MILLIMETERS. C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS. 0.60±0.15-SEATING PLANE 1.25 -M20DRevB1 DETAIL A 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M20D



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N20A

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