

# 74F190

## Up/Down Decade Counter with Preset and Ripple Clock

### General Description

The 74F190 is a reversible BCD (8421) decade counter featuring synchronous counting and asynchronous presetting. The preset feature allows the 74F190 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

### Features

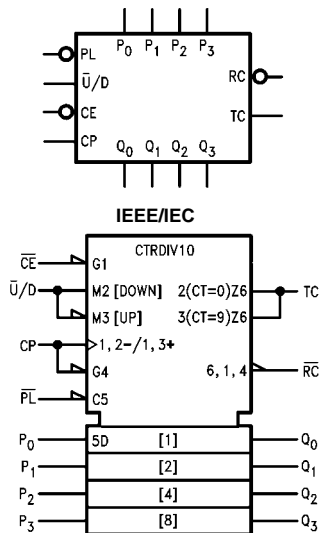
- High-speed—125 MHz typical count frequency
- Synchronous counting
- Asynchronous parallel load
- Cascadable

### Ordering Code:

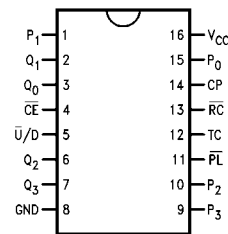
Order Number	Package Number	Package Description
74F190SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74F190PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbols



### Connection Diagram



74F190 Up/Down Decade Counter with Preset and Ripple Clock

## Unit Loading/Fan Out

Pin Names	Description	U.L.	
		HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\overline{CE}$	Count Enable Input (Active LOW)	1.0/3.0	20 $\mu$ A/-1.8 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/-0.6 mA
P <sub>0</sub> -P <sub>3</sub>	Parallel Data Inputs	1.0/1.0	20 $\mu$ A/-0.6 mA
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	1.0/1.0	20 $\mu$ A/-0.6 mA
$\overline{U/D}$	Up/Down Count Control Input	1.0/1.0	20 $\mu$ A/-0.6 mA
Q <sub>0</sub> -Q <sub>3</sub>	Flip-Flop Outputs	50/33.3	-1 mA/20 mA
$\overline{RC}$	Ripple Clock Output (Active LOW)	50/33.3	-1 mA/20 mA
TC	Terminal Count Output (Active HIGH)	50/33.3	-1 mA/20 mA

## Functional Description

The 74F190 is a synchronous up/down BCD decade counter containing four edge-triggered flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations. It has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load ( $\overline{PL}$ ) input is LOW, information present on the Parallel Data inputs (P<sub>0</sub>-P<sub>3</sub>) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table. A HIGH signal on the  $\overline{CE}$  input inhibits counting. When  $\overline{CE}$  is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the  $\overline{U/D}$  input signal, as indicated in the Mode Select Table.  $\overline{CE}$  and  $\overline{U/D}$  can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches 9 in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until  $\overline{U/D}$  is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes. The TC signal is also used internally to enable the Ripple Clock ( $\overline{RC}$ ) output. The  $\overline{RC}$  output is normally HIGH. When  $\overline{CE}$  is LOW and TC is HIGH, the  $\overline{RC}$  output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multi-

stage counters. For a discussion and illustrations of the various methods of implementing multistage counters, please see the 74F191 data sheet.

## $\overline{RC}$ Truth Table

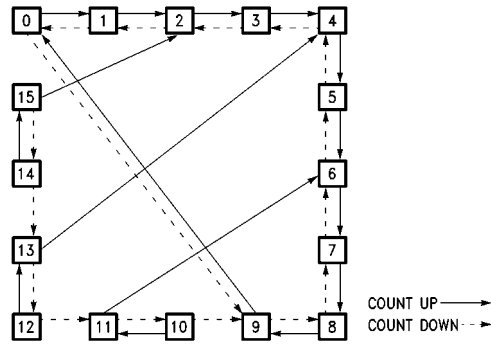
Inputs			Output
$\overline{CE}$	TC*	CP	$\overline{RC}$
L	H	$\overline{\text{Pulse}}$	$\overline{\text{Pulse}}$
H	X	X	H
X	L	X	H

## Mode Select Table

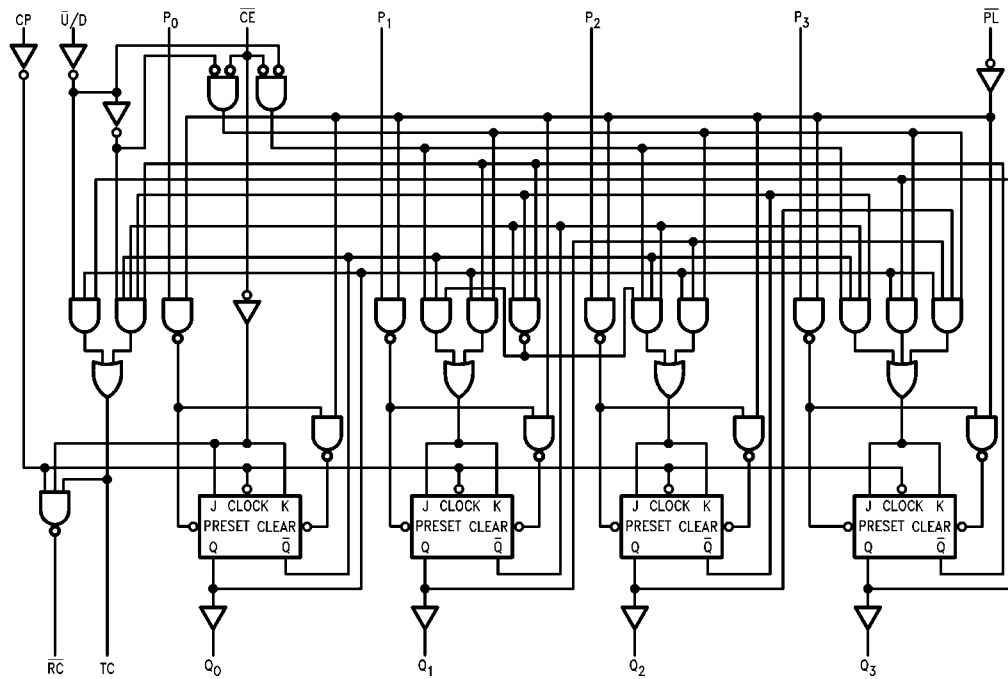
Inputs				Mode
$\overline{PL}$	$\overline{CE}$	$\overline{U/D}$	CP	
H	L	L	$\nearrow$	Count Up
H	L	H	$\nearrow$	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

\*TC is generated internally  
H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
 $\nearrow$  = LOW-to-HIGH Clock Transition  
 $\overline{\text{Pulse}}$  = LOW Pulse

**State Diagram**



**Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

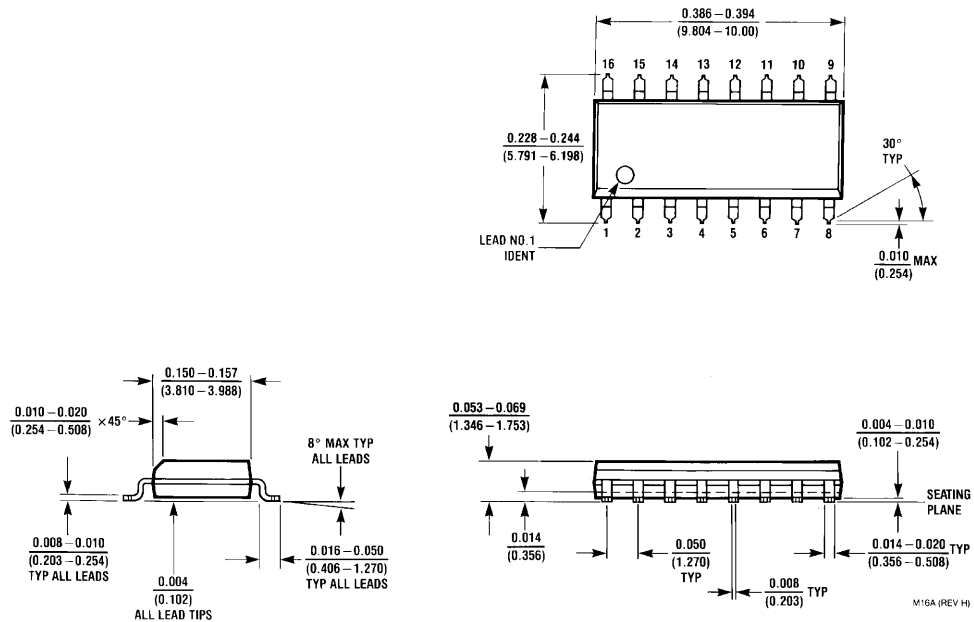
Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA
		5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage			0.5	V	Min	I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V, except $\overline{CE}$ V <sub>IN</sub> = 0.5V, $\overline{CE}$
				-1.8			
I <sub>OS</sub>	Output Short-Circuit Current	-60		-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCL</sub>	Power Supply Current		38	55	mA	Max	V <sub>O</sub> = LOW

AC Electrical Characteristics									
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		Units
		Min	Typ	Max	Min	Max	Min	Max	
$f_{\text{MAX}}$	Maximum Clock Frequency	100	125		75		90		MHz
$t_{\text{PLH}}$	Propagation Delay	3.0	5.5	7.5	3.0	9.5	3.0	8.5	ns
$t_{\text{PHL}}$	CP to $Q_n$	5.0	8.5	11.0	5.0	13.5	5.0	12.0	
$t_{\text{PLH}}$	Propagation Delay	6.0	10.0	13.0	6.0	16.5	6.0	14.0	ns
$t_{\text{PHL}}$	CP to TC	5.0	8.5	11.0	5.0	13.5	5.0	12.0	
$t_{\text{PLH}}$	Propagation Delay	3.0	5.5	7.5	3.0	9.5	3.0	8.5	ns
$t_{\text{PHL}}$	CP to $\overline{\text{RC}}$	3.0	5.0	7.0	3.0	9.0	3.0	8.0	
$t_{\text{PLH}}$	Propagation Delay	3.0	5.0	7.0	3.0	9.0	3.0	8.0	ns
$t_{\text{PHL}}$	$\overline{\text{CE}}$ to $\overline{\text{RC}}$	3.0	5.5	7.0	3.0	9.0	3.0	8.0	
$t_{\text{PLH}}$	Propagation Delay	7.0	11.0	18.0	7.0	22.0	7.0	20.0	ns
$t_{\text{PHL}}$	$\overline{\text{U}}/\text{D}$ to $\overline{\text{RC}}$	5.5	9.0	12.0	5.5	14.0	5.5	13.0	
$t_{\text{PLH}}$	Propagation Delay	4.0	7.0	10.0	4.0	13.5	4.0	11.0	ns
$t_{\text{PHL}}$	$\overline{\text{U}}/\text{D}$ to $\overline{\text{TC}}$	4.0	6.5	10.0	4.0	12.5	4.0	11.0	
$t_{\text{PLH}}$	Propagation Delay	3.0	4.5	7.0	3.0	9.0	3.0	8.0	ns
$t_{\text{PHL}}$	$P_n$ to $Q_n$	6.0	10.0	13.0	6.0	16.0	6.0	14.0	
$t_{\text{PLH}}$	Propagation Delay	5.0	8.5	11.0	5.0	13.0	5.0	12.0	ns
$t_{\text{PHL}}$	$\overline{\text{PL}}$ to $Q_n$	5.5	9.0	12.0	5.5	14.5	5.5	13.0	

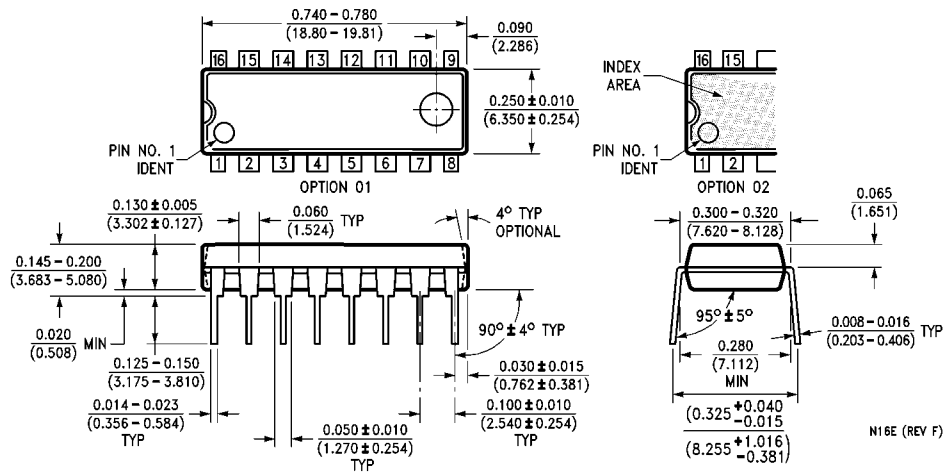
AC Operating Requirements								
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		Units
		Min	Max	Min	Max	Min	Max	
$t_{\text{S}}(\text{H})$	Setup Time, HIGH or LOW	4.5		6.0		5.0		ns
$t_{\text{S}}(\text{L})$	$P_n$ to $\overline{\text{PL}}$	4.5		6.0		5.0		
$t_{\text{H}}(\text{H})$	Hold Time, HIGH or LOW	2.0		2.0		2.0		ns
$t_{\text{H}}(\text{L})$	$P_n$ to $\overline{\text{PL}}$	2.0		2.0		2.0		
$t_{\text{S}}(\text{L})$	Setup Time, LOW	10.0		10.5		10.0		ns
$t_{\text{H}}(\text{L})$	Hold Time, LOW	0		0		0		
$t_{\text{S}}(\text{H})$	Setup Time, HIGH or LOW	12.0		12.0		12.0		ns
$t_{\text{S}}(\text{L})$	$\overline{\text{U}}/\text{D}$ to CP	12.0		12.0		12.0		
$t_{\text{H}}(\text{H})$	Hold Time, HIGH or LOW	0		0		0		ns
$t_{\text{H}}(\text{L})$	$\overline{\text{U}}/\text{D}$ to CP	0		0		0		
$t_{\text{W}}(\text{L})$	$\overline{\text{PL}}$ Pulse Width, LOW	6.0		8.5		6.0		ns
$t_{\text{W}}(\text{L})$	CP Pulse Width, LOW	5.0		7.0		5.0		ns
$t_{\text{REC}}$	Recovery Time $\overline{\text{PL}}$ to CP	6.0		7.5		6.0		ns

**Physical Dimensions** inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow  
Package Number M16A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N16E**

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