

74F189

64-Bit Random Access Memory with 3-STATE Outputs

General Description

The F189 is a high-speed 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are 3-STATE and are in the high impedance state whenever the Chip Select (\overline{CS}) input is HIGH. The outputs are active only in the Read mode and the output data is the complement of the stored data.

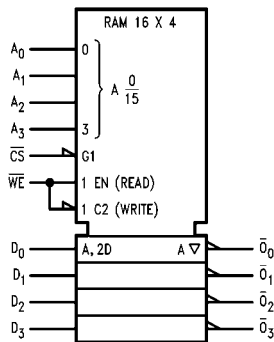
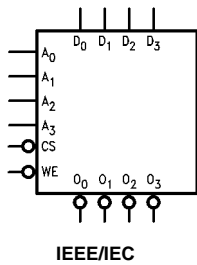
Features

- 3-STATE outputs for data bus applications
- Buffered inputs minimize loading
- Address decoding on-chip
- Diode clamped inputs minimize ringing

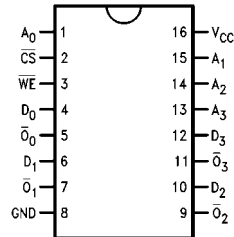
Ordering Code:

Order Number	Package Number	Package Description
74F189PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Logic Symbols



Connection Diagram



74F189 64-Bit Random Access Memory with 3-STATE Outputs

Unit Loading/Fan Out

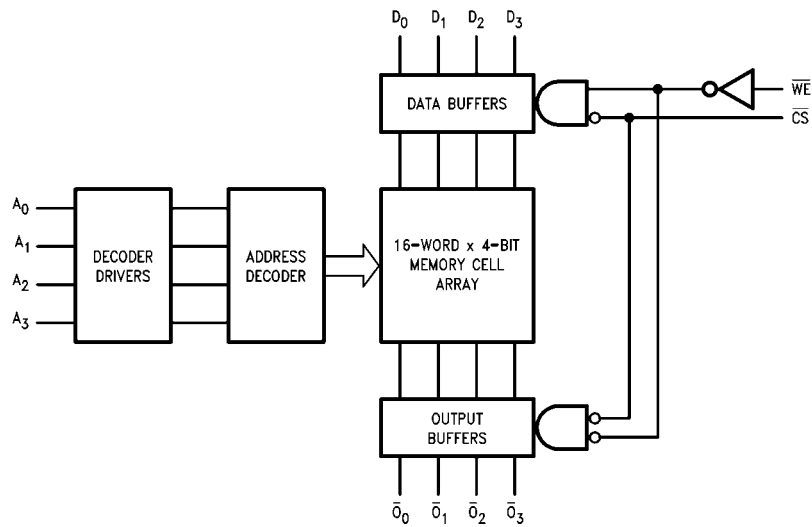
Pin Names	Description	U.L. HIGH/LOW	Input I_H/I_L Output I_{OH}/I_{OL}
A_0 – A_3	Address Inputs	1.0/1.0	20 μ A/–0.6 mA
\overline{CS}	Chip Select Input (Active LOW)	1.0/1.0	20 μ A/–1.2 mA
\overline{WE}	Write Enable Input (Active LOW)	1.0/1.0	20 μ A/–0.6 mA
D_0 – D_3	Data Inputs	1.0/1.0	20 μ A/–0.6 mA
\overline{O}_0 – \overline{O}_3	Inverted Data Outputs	150/40 (33.3)	–3.0 mA/24 mA (20 mA)

Function Table

Inputs		Operation	Condition of Outputs
\overline{CS}	\overline{WE}		
L	L	Write	High Impedance
L	H	Read	Complement of Stored Data
H	X	Inhibit	High Impedance

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Block Diagram



Absolute Maximum Ratings(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

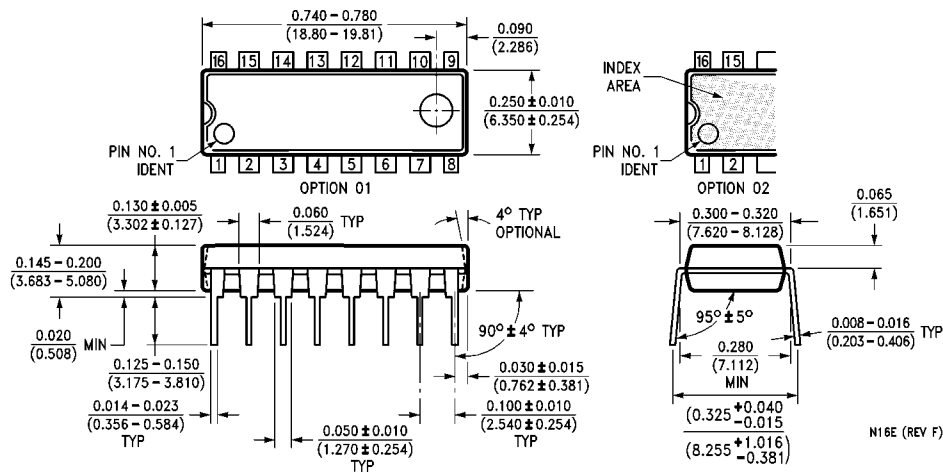
DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	10% V _{CC}	2.5		V	Min	I _{OH} = -1 mA
		10% V _{CC}	2.4	I _{OH} = -3 mA			
		5% V _{CC}	2.7	I _{OH} = -1 mA			
		5% V _{CC}	2.7	I _{OH} = -3 mA			
V _{OL}	Output LOW Voltage			0.5	V	Min	I _{OL} = 24 mA
I _{IH}	Input HIGH Current			5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V
I _{CEx}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current			3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6 -1.2	mA	Max	V _{IN} = 0.5V (except \overline{CS}) V _{IN} = 0.5V (\overline{CS})
I _{OZH}	Output Leakage Current			50	μA	Max	V _{OUT} = 2.7V
I _{OZL}	Output Leakage Current			-50	μA	Max	V _{OUT} = 0.5V
I _{OS}	Output Short-Circuit Current	-60		-150	mA	Max	V _{OUT} = 0V
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	V _{OUT} = 5.25V
I _{CCZ}	Power Supply Current		37	55	mA	Max	V _O = HIGH Z

AC Electrical Characteristics									
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Access Time, HIGH or LOW	10.0	18.5	26.0	9.0	32.0	10.0	27.0	ns
t_{PHL}	A_n to \overline{O}_n	8.0	13.5	19.0	8.0	23.0	8.0	20.0	
t_{PZH}	Access Time, HIGH or LOW	3.5	6.0	8.5	3.5	10.5	3.5	9.5	ns
t_{PZL}	\overline{CS} to \overline{O}_n	5.0	9.0	13.0	5.0	15.0	5.0	14.0	
t_{PHZ}	Disable Time, HIGH or LOW	2.0	4.0	6.0	2.0	8.0	2.0	7.0	ns
t_{PLZ}	\overline{CS} to \overline{O}_n	3.0	5.5	8.0	2.5	10.0	3.0	9.0	
t_{PZH}	Write Recovery Time,	6.5	15.0	28.0	6.5	37.5	6.5	29.0	ns
t_{PZL}	HIGH or LOW \overline{WE} to \overline{O}_n	6.5	11.0	15.5	6.5	17.5	6.5	16.5	
t_{PHZ}	Disable Time, HIGH or LOW	4.0	7.0	10.0	3.5	12.0	4.0	11.0	ns
t_{PLZ}	\overline{WE} to \overline{O}_n	5.0	9.0	13.0	5.0	15.0	5.0	14.0	

AC Operating Requirements									
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		Units	
		Min	Max	Min	Max	Min	Max		
$t_S(H)$	Setup Time, HIGH or LOW	0		0		0		ns	
$t_S(L)$	A_n to \overline{WE}	0		0		0			
$t_H(H)$	Hold Time, HIGH or LOW	2.0		2.0		2.0		ns	
$t_H(L)$	A_n to \overline{WE}	2.0		2.0		2.0			
$t_S(H)$	Setup Time, HIGH or LOW	10.0		11.0		10.0		ns	
$t_S(L)$	D_n to \overline{WE}	10.0		11.0		10.0			
$t_H(H)$	Hold Time, HIGH or LOW	0		2.0		0		ns	
$t_H(L)$	D_n to \overline{WE}	0		2.0		0			
$t_S(L)$	Setup Time, LOW	0		0		0		ns	
$t_H(L)$	Hold Time, LOW	6.0		7.5		6.0			
$t_W(L)$	\overline{WE} Pulse Width, LOW	6.0		15.0		6.0		ns	

Physical Dimensions inches (millimeters) unless otherwise noted



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E**

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