

April 1988 Revised September 2000

74F113

Dual JK Negative Edge-Triggered Flip-Flop

General Description

The 74F113 offers individual J, K, Set and Clock inputs. When the clock goes HIGH the inputs are enabled and data may be entered. The logic level of the J and K inputs may be changed when the clock pulse is HIGH and the flipflop will perform according to the Truth Table as long as minimum setup and hold times are observed. Input data is

transferred to the outputs on the falling edge of the clock pulse.

Asynchronous input:

LOW input to \overline{S}_D sets Q to HIGH level

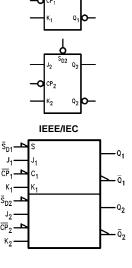
Set is independent of clock

Ordering Code:

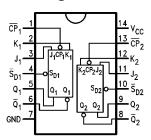
Order Number	Package Number	Package Description
74F113SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
74F113SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F113PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

Dia Nama	Donaintion.	U.L.	Input I _{IH} /I _{IL}	
Pin Names	Description	HIGH/LOW	Output I _{OH} /I _{OL}	
J ₁ , J ₂ , K ₁ , K ₂	Data Inputs	1.0/1.0	20 μA/-0.6 mA	
$\overline{CP}_1, \overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)	1.0/4.0	20 μA/–2.4 mA	
\overline{S}_{D1} , \overline{S}_{D2}	Direct Set Inputs (Active LOW)	1.0/5.0	20 μA/–3.0 mA	
$Q_1, Q_2, \overline{Q}_1, \overline{Q}_2$	Outputs	50/33.3	−1 mA/20 mA	

Truth Table

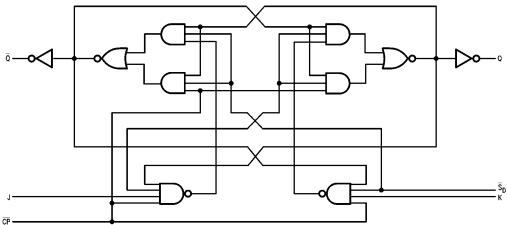
	Inpu	Outputs			
\overline{s}_{D}	CP	J	K	Q	Q
L	Х	Χ	Х	Н	L
Н	\sim	h	h	\overline{Q}_0	Q_0
Н	\sim	1	h	L	Н
Н	\sim	h	- 1	Н	L
Н	\sim	1	- 1	Q_0	\overline{Q}_0

H (h) = HIGH Voltage Level
L (l) = LOW Voltage level
]\[= HIGH-to-LOW Clock Transition
X = Immaterial
Q_0(\overline{\overline{O}}_0) = Before HIGH-to-LOW Transition of Clock

Lower case letters indicate the state of the referenced input or output prior to the HIGH-to-LOW clock transition.

Logic Diagram

(One Half Shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

-65°C to +150°C Storage Temperature Ambient Temperature under Bias -55°C to +125°C

Junction Temperature under Bias -55°C to +150°C V_{CC} Pin Potential to Ground Pin -0.5V to +7.0VInput Voltage (Note 2) -0.5V to +7.0VInput Current (Note 2) -30 mA to +5.0 mA

Voltage Applied to Output

in HIGH State (with $V_{CC} = 0V$)

Standard Output -0.5V to V_{CC}

3-STATE Output -0.5V to +5.5V

Current Applied to Output

in LOW State (Max) twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature 0°C to +70°C Supply Voltage +4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

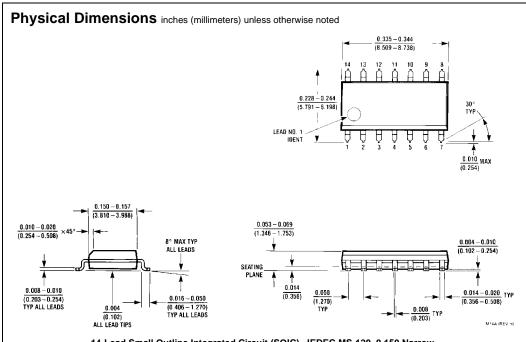
Symbol	l Parameter		Parameter		Min	Тур	Max	Units	V _{CC}	Conditions	
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal			
V _{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal			
V _{CD}	Input Clamp Diode Voltage				-1.2	V	Min	I _{IN} = -18 mA			
V _{OH}	Output HIGH	10% V _{CC}	2.5			V	Min	I _{OH} = -1 mA			
	Voltage	$5\% V_{CC}$	2.7			V	IVIIII	$I_{OH} = -1 \text{ mA}$			
V _{OL}	Output LOW	10% V _{CC}			0.5	V	Min	I _{OL} = 20 mA			
	Voltage										
I _{IH}	Input HIGH				5.0	μА	Max	V _{IN} = 2.7V			
	Current				5.0	μА	IVIAX				
I _{BVI}	Input HIGH Current				7.0	μА	Max	V _{IN} = 7.0V			
	Breakdown Test				7.0	μΛ	IVIAA	VIN - 7.0V			
I _{CEX}	Output HIGH				50	μА	Max	V -V			
	Leakage Current				30	μΛ	IVIAA	$V_{OUT} = V_{CC}$			
V _{ID}	Input Leakage		4.75			V	V 0.0	$I_{ID} = 1.9 \mu A$			
	Test		4.73			V		All Other Pins Grounded			
I _{OD}	Output Leakage				3.75	μА	0.0	V _{IOD} = 150 mV			
	Circuit Current							All Other Pins Grounded			
I _{IL}	Input LOW Current				-0.6			$V_{IN} = 0.5V (J_n, K_n)$			
					-2.4	mA	Max	$V_{IN} = 0.5V (\overline{CP}_n)$			
					-3.0			$V_{IN} = 0.5V (\overline{S}_{Dn})$			
l _{OZH}	Output Leakage Current				50	μΑ	Max	V _{OUT} = 2.7V			
l _{OZL}	Output Leakage Current				-50	μΑ	Max	V _{OUT} = 0.5V			
los	Output Short-Circuit Current		-60		-150	mA	Max	V _{OUT} = 0V			
Icc	Power Supply Current			12	19	mA	Max				

AC Electrical Characteristics

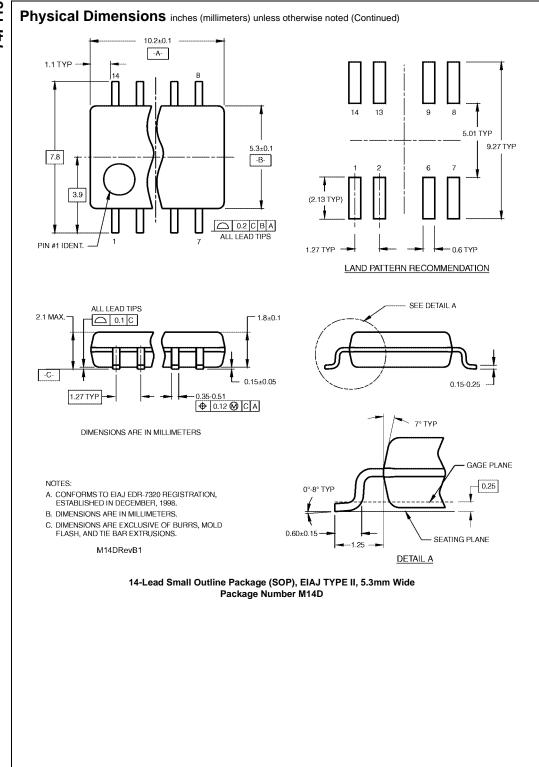
Symbol	Parameter	$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$			$T_A = 0$ °C to +70°C $V_{CC} = +5.0V$ $C_L = 50$ pF		Units	
		Min	Тур	Max	Min	Max		
f _{MAX}	Maximum Clock Frequency	85	105		80		MHz	
t _{PLH}	Propagation Delay	2.0	4.0	6.0	2.0	7.0	no	
t _{PHL}	\overline{CP}_{n} to Q_{n} or \overline{Q}_{n}	2.0	4.0	6.0	2.0	7.0	ns	
t _{PLH}	Propagation Delay	2.0	4.5	6.5	2.0	7.5	20	
t _{PHL}	\overline{S}_{Dn} to Q_n or \overline{Q}_n	2.0	4.5	6.5	2.0	7.5	ns	

AC Operating Requirements

Symbol	Parameter	$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$		$T_A = 0$ °C to +70°C $V_{CC} = +5.0V$		Units	
		Min	Max	Min	Max		
t _S (H)	Setup Time, HIGH or LOW	4.0		5.0			
t _S (L)	J_n or K_n to \overline{CP}_n	3.0		3.5		ns	
t _H (H)	Hold Time, HIGH or LOW	0		0			
t _H (L)	J_n or K_n to \overline{CP}_n	0		0			
t _W (H)	CP _n Pulse Width	4.5		5.0		ns	
t _W (L)	HIGH or LOW	4.5		5.0		115	
t _W (L)	S _{Dn} Pulse Width, LOW	4.5		5.0		ns	
t _{REC}	\overline{S}_{Dn} to \overline{CP}_n Recovery Time	4.0		5.0		ns	



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow Package Number M14A



Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.770(18.80 - 19.56)0.090 (2.286) 14 13 12 11 10 9 8 14 13 12 0.250 ± 0.010 PIN NO. 1 IDENT PIN NO. 1 IDENT 1 2 3 4 5 6 7 1 2 3 $\frac{0.092}{(2.337)}$ DIA 0.030 MAX (0.762) DEPTH OPTION 1 OPTION 02 $\frac{0.135 \pm 0.005}{(3.429 \pm 0.127)}$ 0.300 - 0.320 $\overline{(7.620 - 8.128)}$ 0.065 $\frac{0.145 - 0.200}{(3.683 - 5.080)}$ 0.060 4° TYP Optional (1.524) (1.651) $\frac{0.008 - 0.016}{(0.203 - 0.406)}$ TYP 0.020 (0.508) 0.125 - 0.150 0.075 ± 0.015 $\overline{(3.175 - 3.810)}$ 0.280 (1.905 ± 0.381) (7.112) MIN 0.014 - 0.0230.100 ± 0.010 (2.540 ± 0.254) TYP (0.356 - 0.584) $\frac{0.050\pm0.010}{(1.270-0.254)}$ TYP 0.325 ^{+0.040} -0.015

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A

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- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

 $8.255 + 1.016 \\ -0.381$

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N14A (REV F)