FAIRCHILD

SEMICONDUCTOR ™

74F112
Dual JK Negative Edge-Triggered Flip-Flop

General Description

The 74F112 contains two independent, high-speed JK flip-flops with Direct Set and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to the transition time. The J and K inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. A LOW signal on $\overline{S}_D$ or $\overline{C}_D$ prevents clocking and forces Q or $\overline{Q}$ HIGH, respectively.

Simultaneous LOW signals on $\overline{S}_D$ and $\overline{C}_D$ force both Q and $\overline{Q}$ HIGH.

Asynchronous Inputs:

LOW input to $\overline{S}_D$ sets Q to HIGH level

LOW input to $\overline{C}_D$ sets Q to LOW level

Clear and Set are independent of clock

Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

Ordering Code:

Order Number	Package Number	Package Description
74F112SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74F112SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F112PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols

IEEE/IEC

Connection Diagram
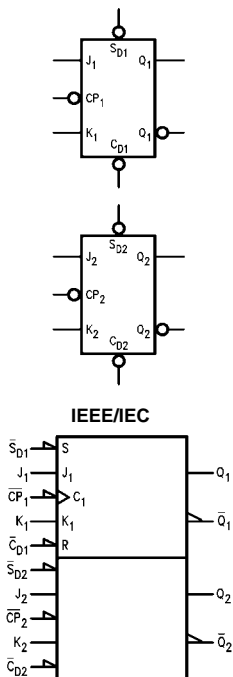
DS009472   www.fairchildsemi.com
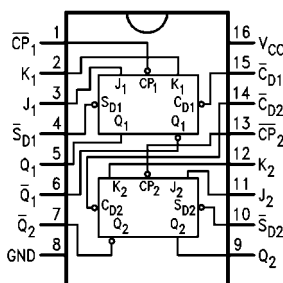
Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
J_1, J_2, K_1, K_2	Data Inputs	1.0/1.0	20 μA/−0.6 mA
$\overline{CP}_1$, $\overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)	1.0/4.0	20 μA/−2.4 mA
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	1.0/5.0	20 μA/−3.0 mA
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	1.0/5.0	20 μA/−3.0 mA
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	50/33.3	−1 mA/20 mA

Truth Table

Inputs					Outputs	
$\overline{S}_D$	$\overline{C}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	$\diagdown$	h	h	$\overline{Q}_0$	Q_0
H	H	$\diagdown$	l	h	L	H
H	H	$\diagdown$	h	l	H	L
H	H	$\diagdown$	l	l	Q_0	$\overline{Q}_0$

H (h) = HIGH Voltage Level
L (l) = LOW Voltage Level
X = Immaterial
$\diagdown$ = HIGH-to-LOW Clock Transition
$Q_0(\overline{Q}_0)$ = Before HIGH-to-LOW Transition of Clock
Lower case letters indicate the state of the referenced input or output one setup time prior to the HIGH-to-LOW clock transition.

Logic Diagram

(One Half Shown)
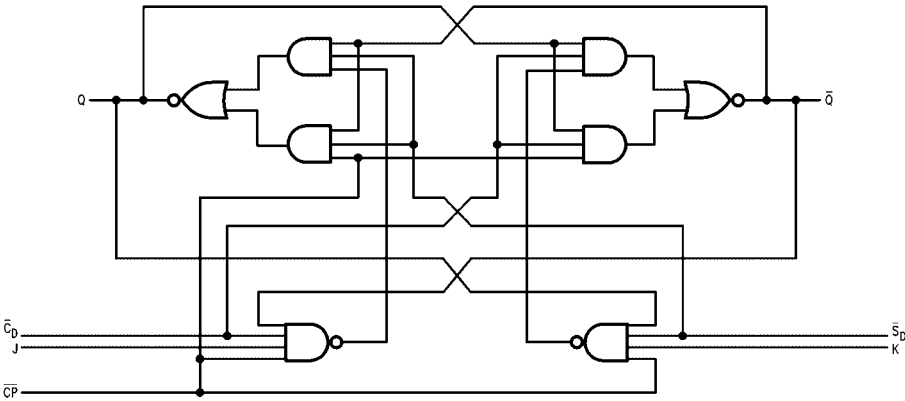
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH	10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
	Voltage	5% V_{CC}	2.7					I_{OH} = −1 mA
V_{OL}	Output LOW	10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
	Voltage							
I_{IH}	Input HIGH				5.0	µA	Max	V_{IN} = 2.7V
	Current							
I_{BVI}	Input HIGH Current				7.0	µA	Max	V_{IN} = 7.0V
	Breakdown Test							
I_{CEX}	Output HIGH				50	µA	Max	V_{OUT} = V_{CC}
	Leakage Current							
V_{ID}	Input Leakage		4.75			V	0.0	I_{ID} = 1.9 µA
	Test							All other pins grounded
I_{OD}	Output Leakage				3.75	µA	0.0	V_{IOD} = 150 mV
	Circuit Current							All other pins grounded
I_{IL}	Input LOW Current				−0.6			V_{IN} = 0.5V (J_n, K_n)
					−2.4	mA	Max	V_{IN} = 0.5V ($\overline{CP}_n$)
					−3.0			V_{IN} = 0.5V ($\overline{C}_{Dn}$, $\overline{S}_{Dn}$)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CCH}	Power Supply Current			12	19	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			12	19	mA	Max	V_O = LOW

AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	85	105		80		MHz
t_{PLH}	Propagation Delay	2.0	5.0	6.5	2.0	7.5	ns
t_{PHL}	$\overline{CP}_n$ to Q_n or $\overline{Q}_n$	2.0	5.0	6.5	2.0	7.5	
t_{PLH}	Propagation Delay	2.0	4.5	6.5	2.0	7.5	ns
t_{PHL}	$\overline{C}_{Dn}$, $\overline{S}_{Dn}$ to $\overline{Q}_n$, $\overline{Q}_n$	2.0	4.5	6.5	2.0	7.5	

AC Operating Requirements

Symbol	Parameter	$T_A = +25°C$ $V_{CC} = +5.0V$		$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V$		Units
		Min	Max	Min	Max	
$t_S(H)$	Setup Time, HIGH or LOW	4.0		5.0		ns
$t_S(L)$	J_n or K_n to $\overline{CP}_n$	3.0		3.5		
$t_H(H)$	Hold Time, HIGH or LOW	0		0		
$t_H(L)$	J_n or K_n to $\overline{CP}_n$	0		0		
$t_W(H)$	$\overline{CP}$ Pulse Width	4.5		5.0		ns
$t_W(L)$	HIGH or LOW	4.5		5.0		
$t_W(L)$	Pulse Width, LOW $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$	4.5		5.0		ns
t_{REC}	Recovery Time $\overline{S}_{Dn}$, $\overline{C}_{Dn}$ to $\overline{CP}$	4.0		5.0		ns

Physical Dimensions inches (millimeters) unless otherwise noted

0.386 − 0.394
(9.804 − 10.00)

16 15 14 13 12 11 10 9

0.228 − 0.244
(5.791 − 6.198)

30°
TYP

LEAD NO.1
IDENT

1 2 3 4 5 6 7 8

0.010 MAX
(0.254)

0.150 − 0.157
(3.810 − 3.988)

0.010 − 0.020
(0.254 − 0.508) ×45°

8° MAX TYP
ALL LEADS

0.008 − 0.010
(0.203 − 0.254)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.053 − 0.069
(1.346 − 1.753)

0.004 − 0.010
(0.102 − 0.254)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008
(0.203) TYP
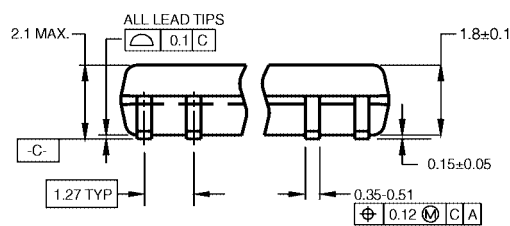
0.014 − 0.020
(0.356 − 0.508) TYP

M16A (REV H)

16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A

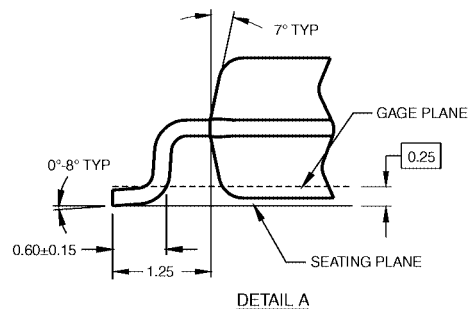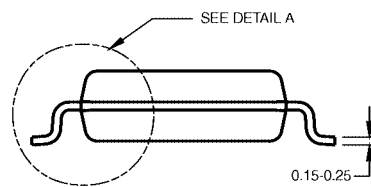# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

10.2±0.1
-A-

0.47 TYP

16   9

7.8

3.9

5.3±0.1
-B-

1   8

PIN #1 IDENT.

△ 0.2 C B A
ALL LEAD TIPS

16   15   10   9

5.01 TYP

9.27 TYP

(2.13 TYP)

1   2   7   8

1.27 TYP   0.6 TYP
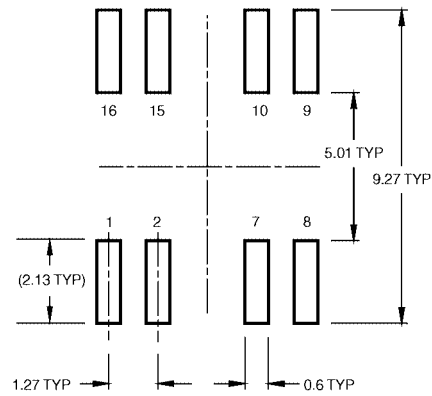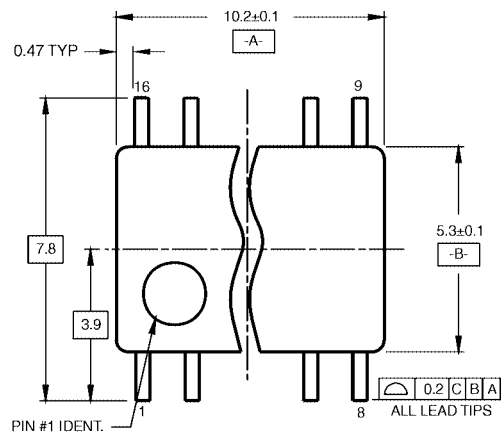
LAND PATTERN RECOMMENDATION

ALL LEAD TIPS
2.1 MAX.   △ 0.1 C

1.8±0.1

-C-

1.27 TYP

0.35-0.51
⊕ 0.12 Ⓜ C A

0.15±0.05

DIMENSIONS ARE IN MILLIMETERS

NOTES:
A. CONFORMS TO EIAJ EDR-7320 REGISTRATION,
   ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
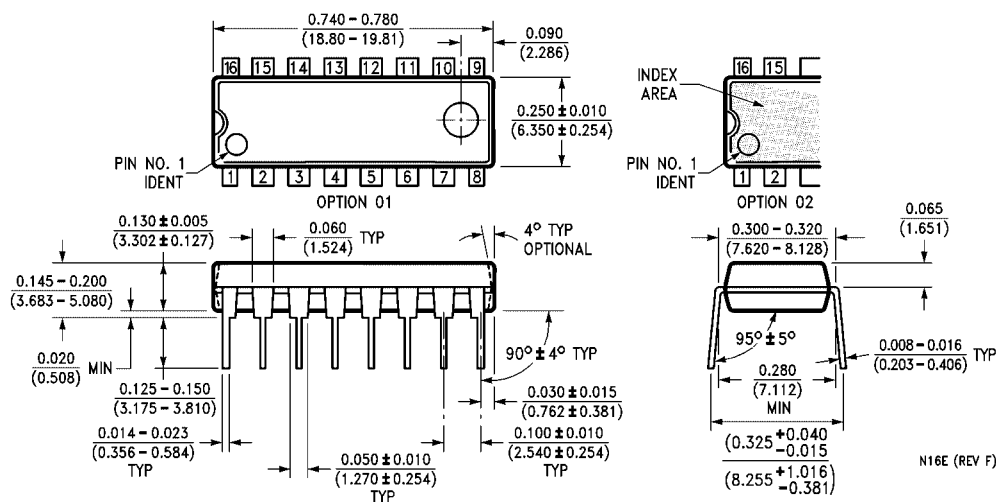C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD
   FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1

SEE DETAIL A

0.15-0.25

7° TYP

GAGE PLANE

0°-8° TYP

0.25

0.60±0.15

1.25

SEATING PLANE

DETAIL A

16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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