

# 74F10

## Triple 3-Input NAND Gate

### General Description

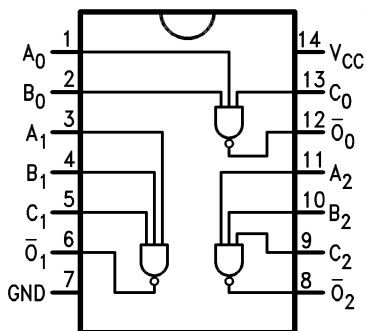
This device contains three independent gates, each of which performs the logic NAND function.

### Ordering Information

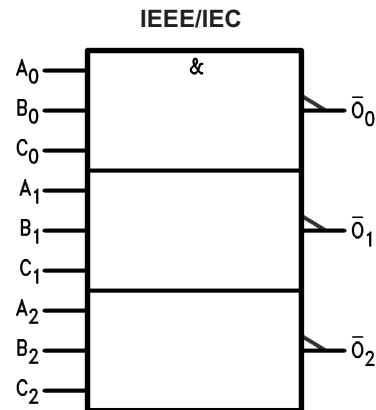
Order Number	Package Number	Package Description
74F10SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74F10SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering number.

### Connection Diagram



### Logic Symbol



### Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ , Output $I_{OH}/I_{OL}$
$A_n, B_n, C_n$	Inputs	1.0 / 1.0	20 $\mu$ A / -0.6mA
$\bar{O}_n$	Outputs	50 / 33.3	-1mA / 20mA

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$T_{STG}$	Storage Temperature	-65°C to +150°C
$T_A$	Ambient Temperature Under Bias	-55°C to +125°C
$T_J$	Junction Temperature Under Bias	-55°C to +150°C
$V_{CC}$	$V_{CC}$ Pin Potential to Ground Pin	-0.5V to +7.0V
$V_{IN}$	Input Voltage <sup>(1)</sup>	-0.5V to +7.0V
$I_{IN}$	Input Current <sup>(1)</sup>	-30mA to +5.0mA
$V_O$	Voltage Applied to Output in HIGH State (with $V_{CC} = 0V$ )	
	Standard Output	-0.5V to $V_{CC}$
	3-STATE Output	-0.5V to 5.5V
	Current Applied to Output in LOW State (Max.)	twice the rated $I_{OL}$ (mA)

### Note:

1. Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
$T_A$	Free Air Ambient Temperature	0°C to +70°C
$V_{CC}$	Supply Voltage	+4.5V to +5.5V

## DC Electrical Characteristics

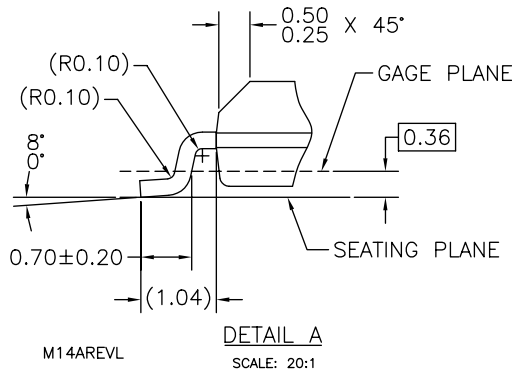
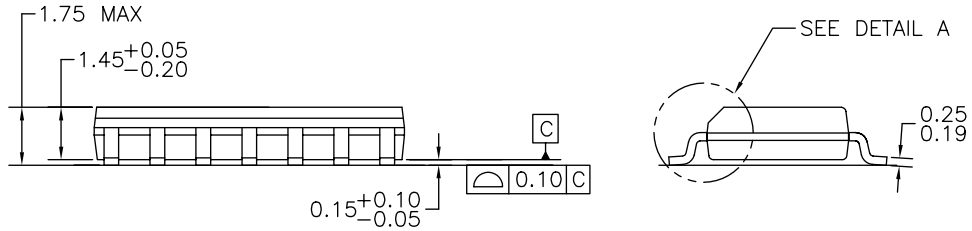
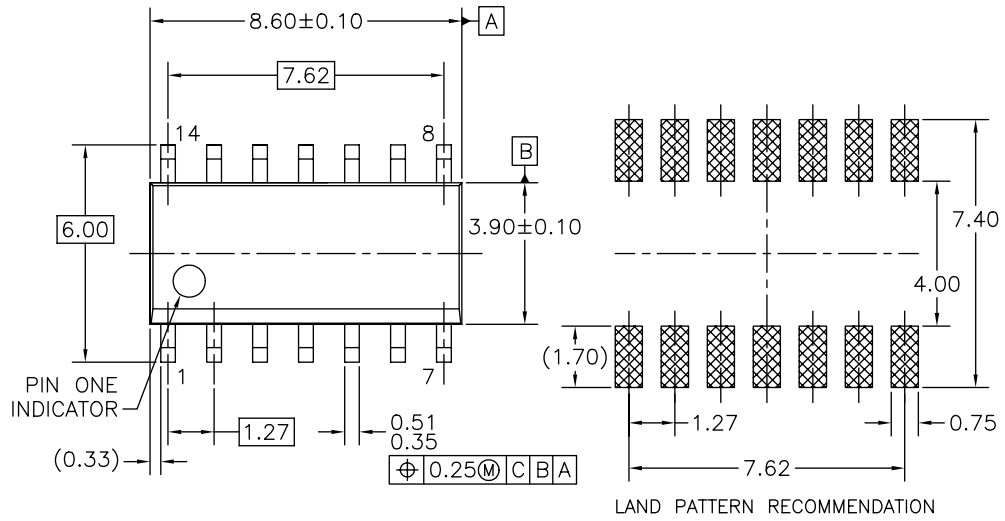
Symbol	Parameter	V <sub>CC</sub>	Conditions	Min.	Typ.	Max.	Units
V <sub>IH</sub>	Input HIGH Voltage		Recognized as a HIGH Signal	2.0			V
V <sub>IL</sub>	Input LOW Voltage		Recognized as a LOW Signal			0.8	V
V <sub>CD</sub>	Input Clamp Diode Voltage	Min.	I <sub>IN</sub> = -18mA			-1.2	V
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub>	I <sub>OH</sub> = -1mA	2.5			V
		5% V <sub>CC</sub>	I <sub>OH</sub> = -1mA	2.7			
V <sub>OL</sub>	Output LOW Voltage	10% V <sub>CC</sub>	I <sub>OL</sub> = 20mA			0.5	V
I <sub>IH</sub>	Input HIGH Current	Max.	V <sub>IN</sub> = 2.7V			5.0	μA
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	Max.	V <sub>IN</sub> = 7.0V			7.0	μA
I <sub>CEx</sub>	Output HIGH Leakage Current	Max.	V <sub>OUT</sub> = V <sub>CC</sub>			50	μA
V <sub>ID</sub>	Input Leakage Test	0.0	I <sub>ID</sub> = 1.9μA, All other pins grounded	4.75			V
I <sub>OD</sub>	Output Leakage Circuit Current	0.0	V <sub>IOD</sub> = 150mV, All other pins grounded			3.75	μA
I <sub>IL</sub>	Input LOW Current	Max.	V <sub>IN</sub> = 0.5V			-0.6	mA
I <sub>OS</sub>	Output Short-Circuit Current	Max.	V <sub>OUT</sub> = 0V	-60		-150	mA
I <sub>CCH</sub>	Power Supply Current	Max.	V <sub>O</sub> = HIGH		1.4	2.1	mA
I <sub>CCL</sub>	Power Supply Current	Max.	V <sub>O</sub> = LOW		5.1	7.7	mA

## AC Electrical Characteristics

Symbol	Parameter	T <sub>A</sub> = +25°C, V <sub>CC</sub> = +5.0V, C <sub>L</sub> = 50pF			T <sub>A</sub> = -55°C to +125°C, V <sub>CC</sub> = +5.0V, C <sub>L</sub> = 50 pF		T <sub>A</sub> = 0°C to +70°C, V <sub>CC</sub> = +5.0V, C <sub>L</sub> = 50pF		Units
		Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t <sub>PLH</sub>	Propagation Delay, A <sub>n</sub> , B <sub>n</sub> , C <sub>n</sub> to $\bar{O}_n$	2.4	3.7	5.0	2.0	7.0	2.4	6.0	ns
t <sub>PHL</sub>		1.5	3.2	4.3	1.5	6.5	1.5	5.3	

**Physical Dimensions**

Dimensions are in millimeters unless otherwise noted.



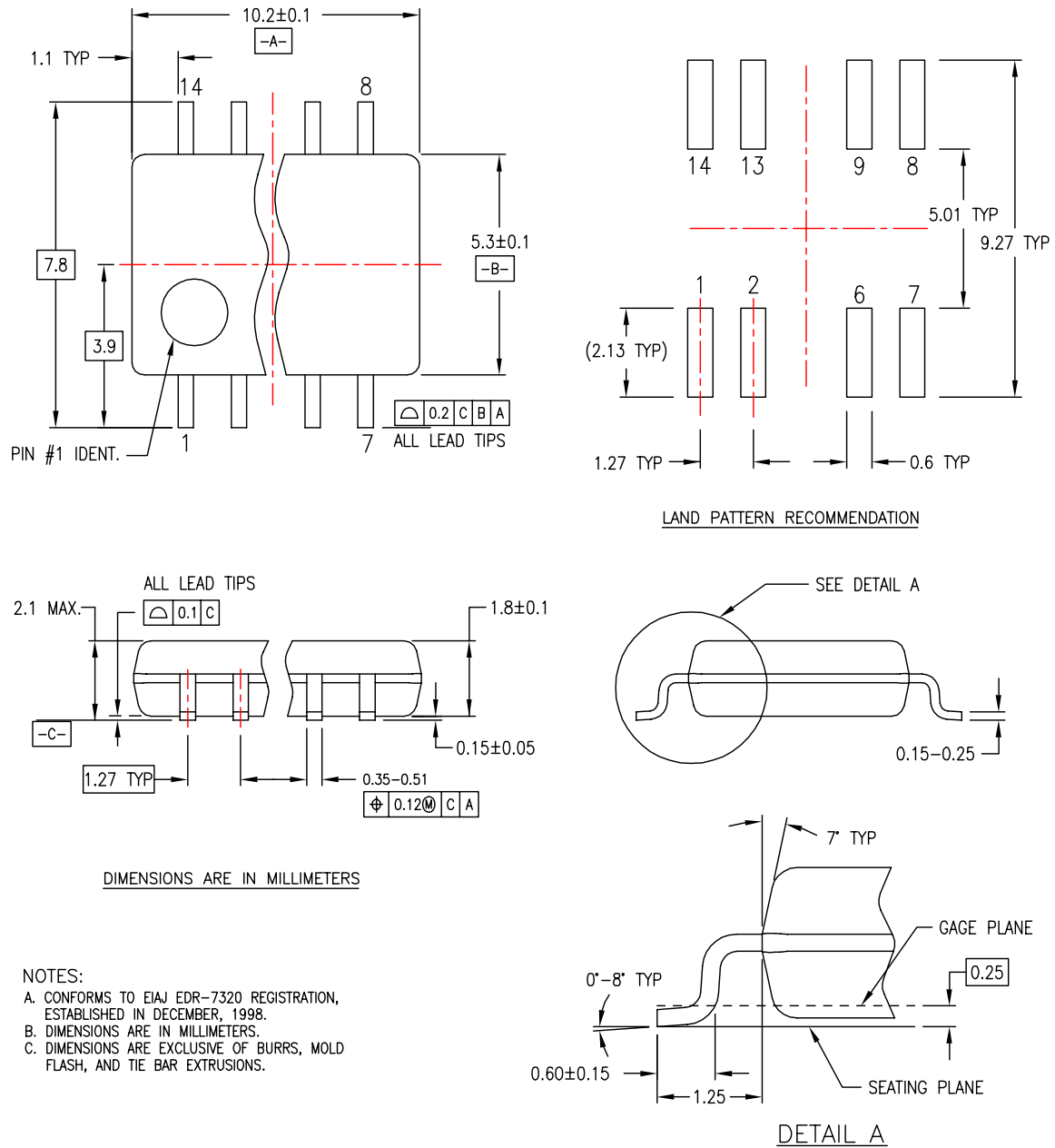
NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C, DATED MAY 1990.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.

**Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M14A**

**Physical Dimensions** (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.


M14DREVC

**Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M14D**



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