FAIRCHILD SEMICONDUCTOR™

September 2001
Revised October 2001

74ALVCR162601
Low Voltage 18-Bit Universal Bus Transceivers with 3.6V Tolerant Inputs and Outputs and 26Ω Series Resistors in the Outputs

General Description

The 74ALVCR162601, 18-bit universal bus transceiver, combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH-to-LOW logic level. If LEAB is LOW, the A bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CLKAB. Output-enable $\overline{OEAB}$ is active-LOW. When $\overline{OEAB}$ is HIGH, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA and $\overline{CLKENBA}$.

The 74ALVCR162601 is designed for low voltage (1.65V to 3.6V) V_{CC} applications with I/O compatibility up to 3.6V. The 74ALVCR162601 is also designed with 26Ω series resistors on both the A and B Port outputs. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

Features

- 1.65–3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- 26Ω series resistors on both the A and B Port outputs.
- t_{PD} (A to B, B to A)
  - 4.3 ns max for 3.0V to 3.6V V_{CC}
  - 5.1 ns max for 2.3V to 2.7V V_{CC}
  - 9.2 ns max for 1.65V to 1.95V V_{CC}
- Power-down HIGH impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- Uses patented noise/EMI reduction circuitry
- Latchup conforms to JEDEC JED78
- ESD performance:
  - Human body model > 2000V
  - Machine model >200V

Note 1: To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

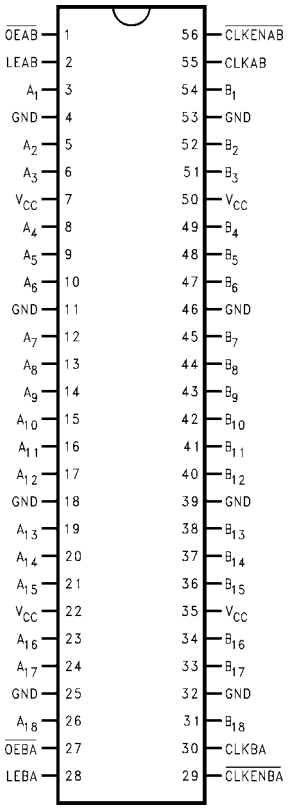
Ordering Code:

Order Number	Package Number	Package Description
74ALVCR162601T	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

© 2001 Fairchild Semiconductor Corporation

Connection Diagram



Pin Descriptions

Pin Names	Description
$\overline{OEAB}$, $\overline{OEBA}$	Output Enable Inputs (Active LOW)
LEAB, LEBA	Latch Enable Inputs
CLKAB, CLKBA	Clock Inputs
$\overline{CLKENAB}$, $\overline{CLKENBA}$	Clock Enable Inputs
A_1–A_{18}	Side A Inputs or 3-STATE Outputs
B_1–B_{18}	Side B Inputs or 3-STATE Outputs

Function Table (Note 2)

Inputs					Outputs
$\overline{CLKENAB}$	$\overline{OEAB}$	LEAB	CLKAB	A_n	B_n
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_0 (Note 3)
H	L	L	X	X	B_0 (Note 3)
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B_0 (Note 3)
L	L	L	H	X	B_0 (Note 4)

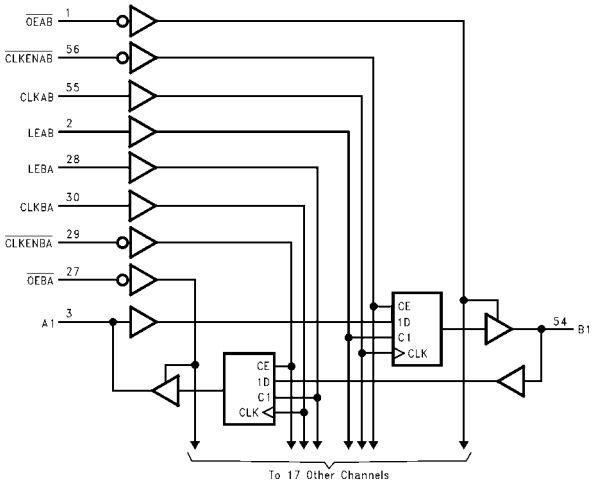
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial (HIGH or LOW, inputs may not float)
Z = HIGH Impedance

Note 2: A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CLKENBA}$.

Note 3: Output level before the indicated steady-state input conditions were established

Note 4: Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.

Logic Diagram



Absolute Maximum Ratings(Note 5)

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage (V_I)	−0.5V to 4.6V
Output Voltage (V_O) (Note 6)	−0.5V to V_{CC} +0.5V
DC Input Diode Current (I_{IK})	
V_I < 0V	−50 mA
DC Output Diode Current (I_{OK})	
V_O < 0V	−50 mA
DC Output Source/Sink Current	
(I_{OH}/I_{OL})	±50 mA
DC V_{CC} or GND Current per	
Supply Pin (I_{CC} or GND)	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C

Recommended Operating Conditions (Note 7)

Power Supply	
Operating	1.65V to 3.6V
Input Voltage	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10 ns/V

Note 5: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 6: I_O Absolute Maximum Rating must be observed.

Note 7: Floating or unused control inputs must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		1.65 - 1.95	0.65 x V_{CC}		V
			2.3 - 2.7	1.7		
			2.7 - 3.6	2.0		
V_{IL}	LOW Level Input Voltage		1.65 - 1.95		0.35 x V_{CC}	V
			2.3 - 2.7		0.7	
			2.7 - 3.6		0.8	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 µA	1.65 - 3.6	V_{CC} - 0.2		V
		I_{OH} = −2 mA	1.65	1.2		
		I_{OH} = −4 mA	2.3	1.9		
		I_{OH} = −6 mA	2.3	1.7		
			3.0	2.4		
		I_{OH} = −8 mA	2.7	2		
		I_{OH} = −12 mA	3.0	2		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA	1.65 - 3.6		0.2	V
		I_{OL} = 2 mA	1.65		0.45	
		I_{OL} = 4 mA	2.3		0.4	
		I_{OL} = 6 mA	2.3		0.55	
			3.0		0.55	
		I_{OL} = 8 mA	2.7		0.6	
		I_{OL} = 12 mA	3.0		0.8	
I_{OH}	High Level Output Current		1.65		−2	mA
			2.3		−6	
			2.7		−8	
			3.0		−12	
I_{OL}	Low Level Output Current		1.65		2	mA
			2.3		6	
			2.7		8	
			3.0		12	
I_I	Input Leakage Current	0 ≤ V_I ≤ 3.6V	1.65 - 3.6		±5.0	µA
I_{OZ}	3-STATE Output Leakage	0 ≤ V_O ≤ 3.6V, V_I = V_{IH} or V_{IL}	1.65 - 3.6		±10	µA
I_{OFF}	Power Off Leakage Current	0V ≤ (V_I, V_O) ≤ 3.6V	0		10	mA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND, I_O = 0	3.6		40	µA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} − 0.6V	2.7 - 3.6		750	µA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $R_L = 500\Omega$								Units
		$C_L = 50$ pF				$C_L = 30$ pF				
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		$V_{CC} = 2.5 \pm 0.2V$		$V_{CC} = 1.8V \pm 0.15V$		
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	250		200		200		125		MHz
t_{PHL}, t_{PLH}	Propagation Delay A to B or B to A	1.1	4.3	1.3	5.1	0.8	4.6	1.5	9.2	ns
t_{PHL}, t_{PLH}	Propagation Delay Clock to A or B	1.1	4.9	1.3	6.0	0.8	5.5	1.5	9.8	ns
t_{PHL}, t_{PLH}	Propagation Delay LEBA or LEAB to A or B	1.1	4.9	1.3	6.3	0.8	5.8	1.5	9.8	ns
t_{PZL}, t_{PZH}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A or B	1.1	4.8	1.3	6.4	0.8	5.9	1.5	9.8	ns
t_{PLZ}, t_{PHZ}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A or B	1.1	4.8	1.3	5.4	0.8	4.9	1.5	8.8	ns
t_S	Setup Time	1.5		1.5		1.5		2.5		ns
t_H	Hold Time	1.0		1.0		1.0		1.0		ns
t_W	Pulse Width	1.5		1.5		1.5		4.0		ns

Capacitance

Symbol	Parameter		Conditions	$T_A = +25°C$		Units
				V_{CC}	Typical	
C_{IN}	Input Capacitance		$V_I = 0V$ or V_{CC}	3.3	6	pF
C_{OUT}	Output Capacitance		$V_I = 0V$ or V_{CC}	3.3	7	pF
C_{PD}	Power Dissipation Capacitance	Outputs Enabled	f = 10 MHz, $C_L = 0$ pF	3.3	20	pF
				2.5	20	

AC Loading and Waveforms

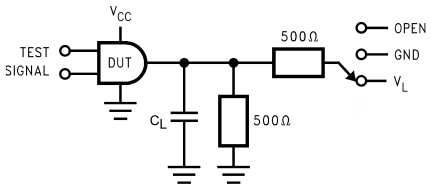


FIGURE 1. AC Test Circuit

Table 1: Values for Figure 1

TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_L
t_{PZH}, t_{PHZ}	GND

Table 2: Variable Matrix
(Input Charactertistics: f = 1MHz; t_r=t_f=2ns; Z_0= 50Ω)

Symbol	V_{CC}			
	3.3V ± 0.3V	**2.7V**	**2.5V ± 0.2V**	**1.8V ± 0.15V**
V_{mi}	1.5V	1.5V	V_{CC}/2	V_{CC}/2
V_{mo}	1.5V	1.5V	V_{CC}/2	V_{CC}/2
V_X	V_{OL} + 0.3V	V_{OL} + 0.3V	V_{OL} + 0.15V	V_{OL} + 0.15V
V_Y	V_{OH} − 0.3V	V_{OH} − 0.3V	V_{OH} − 0.15V	V_{OH} − 0.15V
V_L	6V	6V	V_{CC}*2	V_{CC}*2

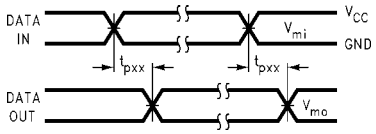


FIGURE 2. Waveform for Inverting and Non-inverting Functions

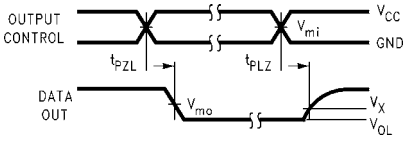


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

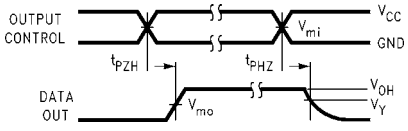


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

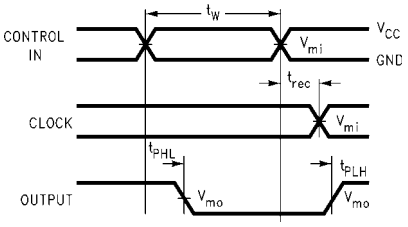


FIGURE 5. Propagation Delay, Pulse Width and t_{rec} Waveforms

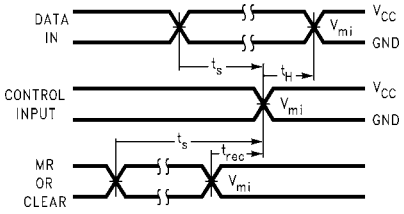
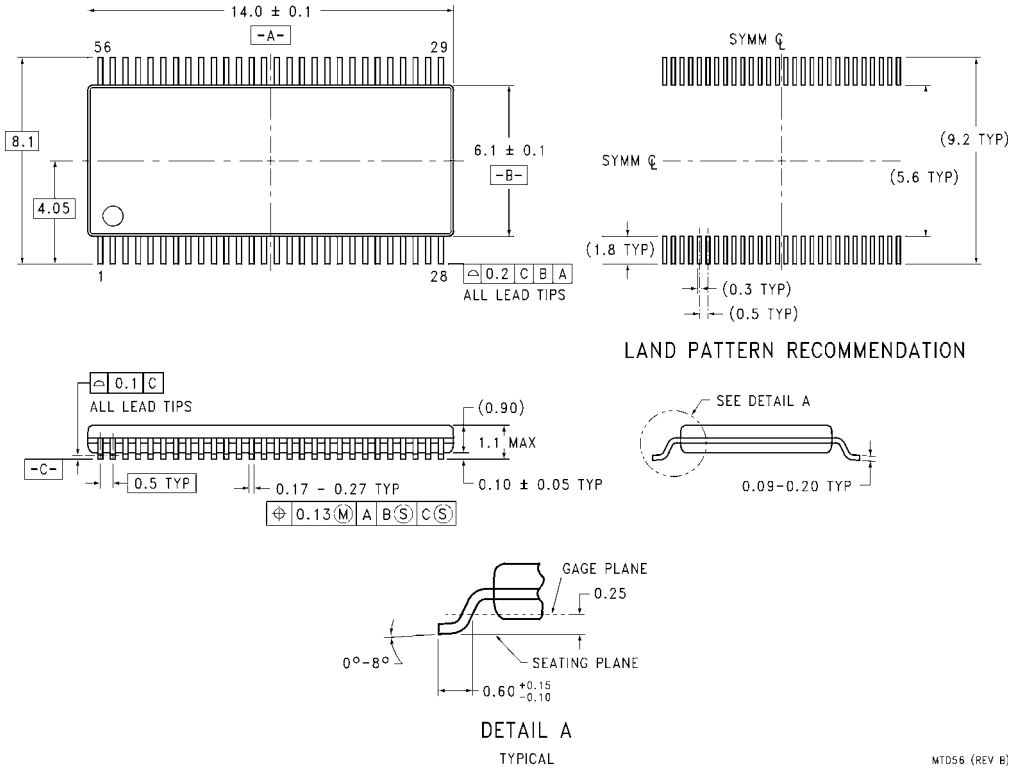


FIGURE 6. Setup Time, Hold Time and Recovery Time for Low Voltage Logic

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com