FAIRCHILD SEMICONDUCTOR®

January 2008

74ALVC245
Low Voltage Bidirectional Transceiver with 3.6V Tolerant Inputs and Outputs

Features

- 1.65V to 3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- Power-off high impedance inputs and outputs
- Supports Live Insertion and Withdrawal(1)
- t_{PD}:
  - 3.4ns max. for 3.0V to 3.6V V_{CC}
  - 3.9ns max. for 2.3V to 2.7V V_{CC}
  - 6ns max. for 1.65V to 1.95V V_{CC}
- Uses patented Quiet Series™ noise/EMI reduction circuitry
- Latchup conforms to JEDEC JED78
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V

Note:

1. To ensure the high impedance state during power up and power down, $\overline{OE}_n$ should be tied to V_{CC} through a pull up resistor. The minimum value of the resistor is determined by the current sourcing capability of the driver.

General Description

The ALVC245 contains eight non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The T/$\overline{R}$ input determines the direction of data flow. The $\overline{OE}$ input disables both the A and B ports by placing them in a high impedance state.

The 74ALVC245 is designed for low voltage (1.65V to 3.6V) V_{CC} applications with I/O compatibility up to 3.6V.

The 74ALVC245 is fabricated with an advanced CMOS technology to achieve high-speed operation while maintaining low CMOS power dissipation.

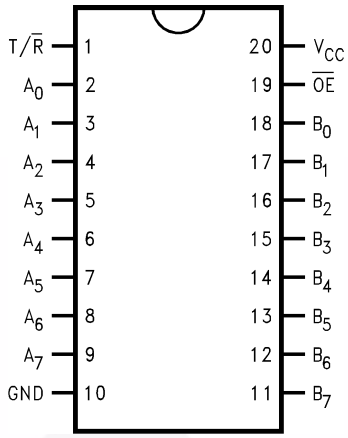
Ordering Information

Order Number	Package Number	Package Description
74ALVC245WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ALVC245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

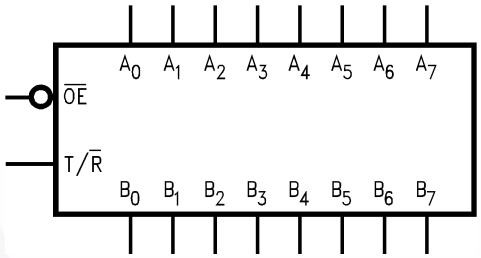
Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



Logic Symbol



Pin Description

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or 3-STATE Outputs
B_0–B_7	Side B Inputs or 3-STATE Outputs

Truth Table

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH Z State on A_0–A_7, B_0–B_7(2)

H = HIGH Voltage Level

L = LOW Voltage Level

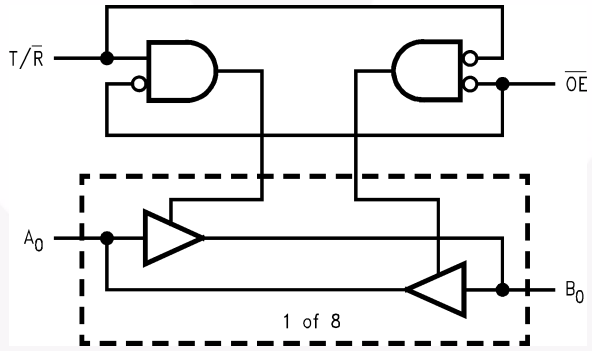
X = Immaterial

Z = High Impedance

Note:

2. Unused bus terminals during HIGH Z State must be held HIGH or LOW.

Logic Diagram



Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +4.6V
V_I	DC Input Voltage	–0.5V to 4.6V
V_O	Output Voltage[3]	–0.5V to V_{CC} +0.5V
I_{IK}	DC Input Diode Current, $V_I < 0V$	–50mA
I_{OK}	DC Output Diode Current, $V_O < 0V$	–50mA
I_{OH}/I_{OL}	DC Output Source/Sink Current	±50mA
I_{CC} or GND	DC V_{CC} or GND Current per Supply Pin	±100mA
T_{STG}	Storage Temperature Range	–65°C to +150°C

Note:

3. I_O Absolute Maximum Rating must be observed, limited to 4.6V.

Recommended Operating Conditions[4]

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	1.65V to 3.6V
V_I	Input Voltage	0V to V_{CC}
V_O	Output Voltage	0V to V_{CC}
T_A	Free Air Operating Temperature	–40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate: V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10ns/V

Note:

4. Floating or unused control inputs must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	Min.	Max.	Units
V_{IH}	HIGH Level Input Voltage	1.65–1.95		0.65 x V_{CC}		V
		2.3–2.7		1.7		
		2.7–3.6		2.0		
V_{IL}	LOW Level Input Voltage	1.65–1.95			0.35 x V_{CC}	V
		2.3–2.7			0.7	
		2.7–3.6			0.8	
V_{OH}	HIGH Level Output Voltage	1.65–3.6	I_{OH} = –100µA	V_{CC} – 0.2		V
		1.65	I_{OH} = –4mA	1.2		
		2.3	I_{OH} = –6mA	2.0		
		2.3	I_{OH} = –12mA	1.7		
		2.7		2.2		
		3.0		2.4		
		3.0	I_{OH} = –24mA	2		
V_{OL}	LOW Level Output Voltage	1.65–3.6	I_{OL} = 100µA		0.2	V
		1.65	I_{OL} = 4mA		0.45	
		2.3	I_{OL} = mA		0.4	
		2.3	I_{OL} = 12mA		0.7	
		2.7			0.4	
		3.0	I_{OL} = 24mA		0.55	
I_I	Input Leakage Current	3.6	$0 \le V_I \le 3.6V$		±5.0	µA
I_{OZ}	3-STATE Output Leakage	3.6	$0 \le V_O \le 3.6V$		±10	µA
I_{CC}	Quiescent Supply Current	3.6	$V_I = V_{CC}$ or GND, $I_O = 0$		10	µA
ΔI_{CC}	Increase in I_{CC} per Input	3–3.6	$V_{IH} = V_{CC} - 0.6V$		750	µA

AC Electrical Characteristics

		$T_A = -40°C$ to $+85°C$, $R_L = 500\Omega$								
		$C_L = 50pF$				$C_L = 30pF$				
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 1.8V \pm 0.15V$		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{PHL}, t_{PLH}	Propagation Delay	1.3	3.4		3.9	1.0	3.5	1.5	6.0	ns
t_{PZL}, t_{PZH}	Output Enable Time	1.6	5.5		6.3	2.0	6.0	2.7	8.6	ns
t_{PLZ}, t_{PHZ}	Output Disable Time	1.7	5.5		5.3	0.8	4.8	1.5	8.0	ns

Capacitance

Symbol	Parameter		Conditions	$T_A = +25°C$		Units
				V_{CC}	Typical	
C_{IN}	Input Capacitance	Control	V_I = 0V or V_{CC}	3.3	3	pF
$C_{I/O}$	Input/ Output Capacitance	A or B Ports	V_I = 0V or V_{CC}	3.3	6	
C_{PD}	Power Dissipation Capacitance	Outputs Enabled	f = 10MHz, C_L = 0pF	3.3	30	pF
				2.5	27	
				1.8	25	
		Outputs Disabled	f = 10MHz, C_L = 0pF	3.3	0	
				2.5	0	
				1.8	0	

AC Loading and Waveforms

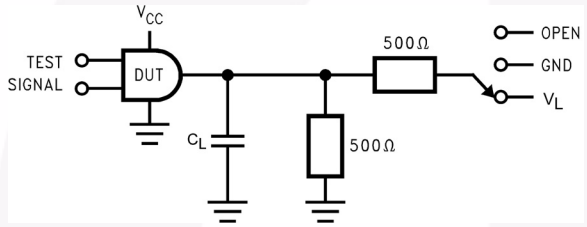


Figure 1. AC Test Circuit

Table 1. Values for Figure 1

Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_L
t_{PZH}, t_{PHZ}	GND

Table 2. Variable Matrix
(Input Characteristics: f = 1MHz; $t_r = t_f$ = 2ns; Z_0 = 50Ω)

Symbol	V_{CC}			
	3.3V ± 0.3V	2.7V	2.5V ± 0.2V	1.8V ± 0.15V
V_{mi}	1.5V	1.5V	V_{CC} / 2	V_{CC} / 2
V_{mo}	1.5V	1.5V	V_{CC} / 2	V_{CC} / 2
V_X	V_{OL} + 0.3V	V_{OL} + 0.3V	V_{OL} + 0.15V	V_{OL} + 0.15V
V_Y	V_{OH} – 0.3V	V_{OH} – 0.3V	V_{OH} – 0.15V	V_{OH} – 0.15V
V_L	6V	6V	V_{CC} x 2	V_{CC} x 2

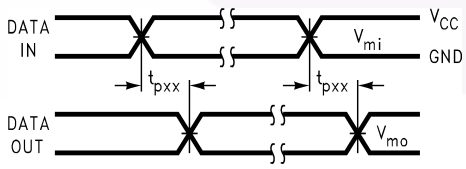


Figure 2. Waveform for Inverting and Non-Inverting Functions

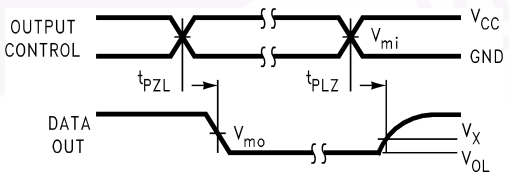


Figure 3. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Physical Dimensions

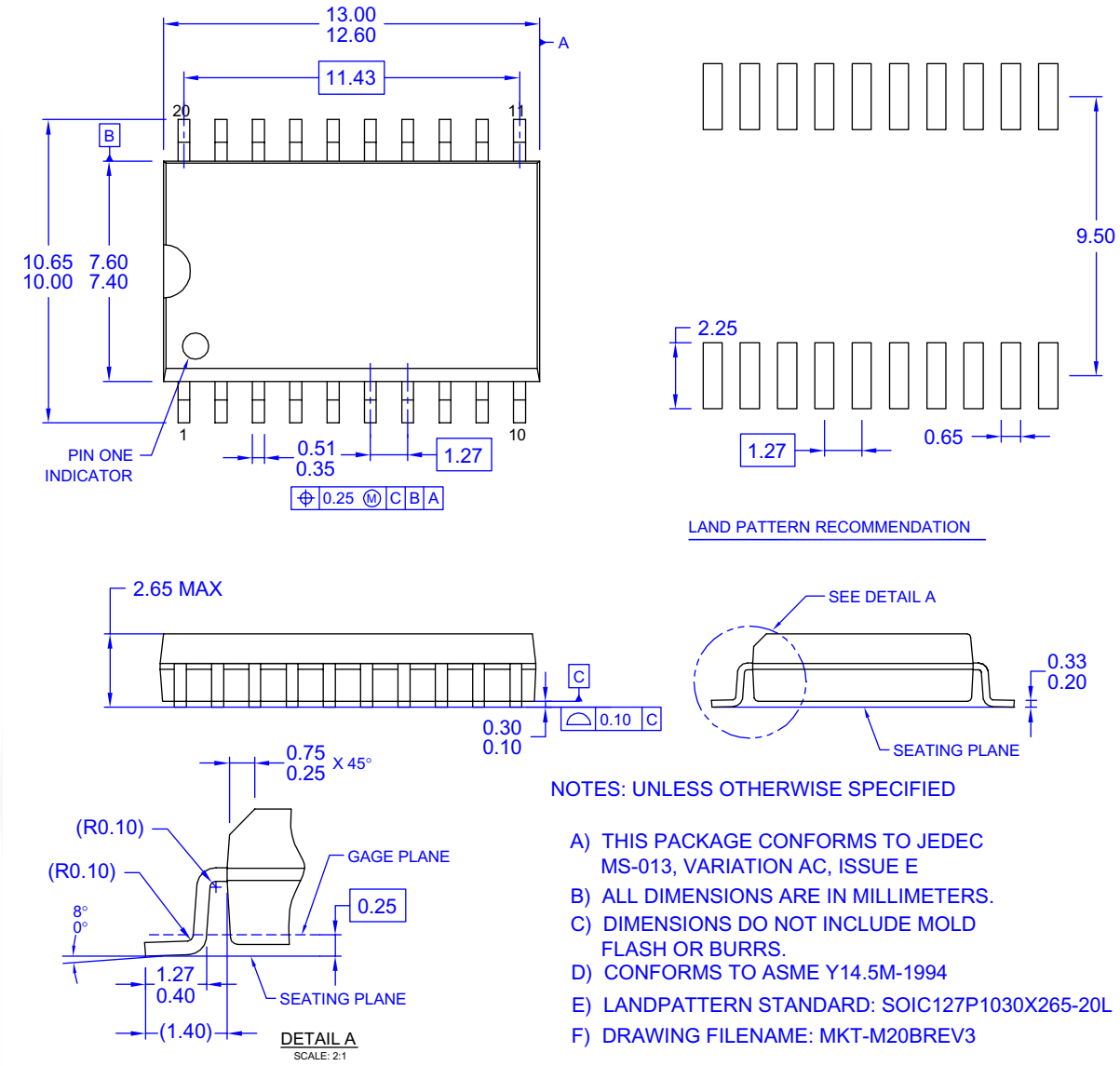


Figure 4. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

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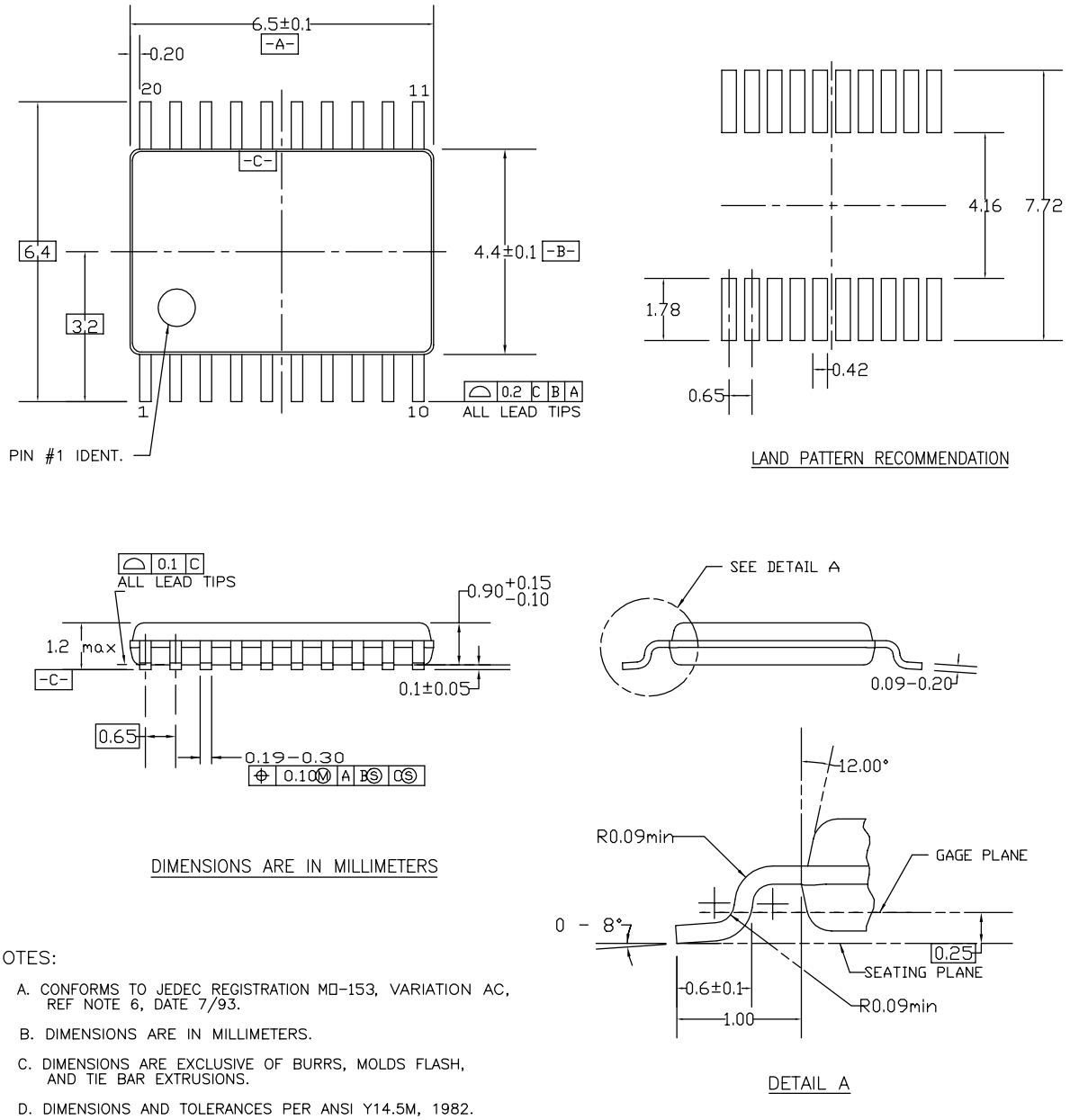
Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

Figure 5. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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Rev. I32