

October 2001 Revised November 2001

74ALVC162245

Low Voltage 16-Bit Bidirectional Transceiver with 3.6V Tolerant Inputs and Outputs and 26 Ω Series Resistors in A Port Outputs

General Description

The ALVC162245 contains sixteen non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. Each byte has separate 3-STATE control inputs which can be shorted together for full 16-bit operation. The T/\overline{R} inputs determine the direction of data flow through the device. The \overline{OE} inputs disable both the A and B Ports by placing them in a high impedance state.

The 74ALVC162245 is designed for low voltage (1.65V to 3.6V) V_{CC} applications with I/O compatibility up to 3.6V.

The 74ALVC162245 is also designed with 26Ω series resistance in the A Port outputs. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

The 74ALVC162245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- 1.65V-3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- \blacksquare 26 Ω series resistors in A Port outputs
- t_{PC}

3.9 ns max for 3.0V to 3.6V $\rm V_{CC}$ 4.8 ns max for 2.3V to 2.7V $\rm V_{CC}$ 8.6 ns max for 1.65V to 1.95V $\rm V_{CC}$

- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- Uses patented noise/EMI reduction circuitry
- Latchup conforms to JEDEC JED78
- ESD performance:

Human body model > 2000V Machine model >200V

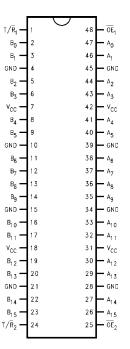
Note 1: To ensure the high-impedance state during power up or power down, $\overline{\text{DE}}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver

Ordering Code:

Order Number	Package Number	Package Description
74ALVC162245T	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Logic Symbol



Pin Descriptions

Pin Names	Description
OE _n	Output Enable Input (Active LOW)
T/\overline{R}_n	Transmit/Receive Input
A ₀ -A ₁₅	Side A Inputs or 3-STATE Outputs
B ₀ -B ₁₅	Side B Inputs or 3-STATE Outputs

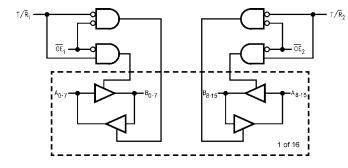
Truth Tables

Inj	outs	Q.,,t.,,,,t.,			
OE ₁ T/R ₁		Outputs			
L	L	Bus B ₀ –B ₇ Data to Bus A ₀ –A ₇			
L	Н	Bus A ₀ -A ₇ Data to Bus B ₀ -B ₇			
Н	X	HIGH Z State on A ₀ -A ₇ , B ₀ -B ₇			

Inp	outs	Outrote			
OE ₂ T/R ₂		Outputs			
L	L	Bus B ₈ –B ₁₅ Data to Bus A ₈ –A ₁₅			
L	Н	Bus A ₈ –A ₁₅ Data to Bus B ₈ –B ₁₅			
Н	Х	HIGH Z State on A ₈ -A ₁₅ , B ₈ -B ₁₅			

- H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial (HIGH or LOW, inputs and I/O's may not float)
- Z = High Impedance

Logic Diagram



Absolute Maximum Ratings(Note 2)

 $\begin{array}{lll} \mbox{Supply Voltage (V_{CC})} & -0.5 \mbox{V to } +4.6 \mbox{V} \\ \mbox{DC Input Voltage (V_I)} & -0.5 \mbox{V to } 4.6 \mbox{V} \end{array}$

Output Voltage (V $_{\rm O}$) (Note 3) $-0.5 \mbox{V}$ to V $_{\rm CC}$ +0.5V

DC Input Diode Current (I_{IK})

 $V_1 < 0V$ -50 mA

DC Output Diode Current (I_{OK})

 $V_O < 0V$ –50 mA

DC Output Source/Sink Current
(I_{OH}/I_{OL})

DC V_{CC} or GND Current per

Supply Pin (I_{CC} or GND) ±100 mA

Storage Temperature Range (T_{STG}) -65°C to +150°C

Recommended Operating Conditions (Note 4)

Power Supply

±50 mA

Operating 1.65V to 3.6V Input Voltage 0V to V_{CC}

Minimum Input Edge Rate (Δt/ΔV)

 $V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$ 10 ns/V

Note 2: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: I_O Absolute Maximum Rating must be observed.

Note 4: Floating or unused control inputs must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	Min	Max	Units
V _{IH}	HIGH Level Input Voltage		1.65 - 1.95	0.65 x V _{CC}		
			2.3 - 2.7	1.7		V
			2.7 - 3.6	2.0		
V _{IL}	LOW Level Input Voltage		1.65 - 1.95		0.35 x V _{CC}	
			2.3 - 2.7		0.7	V
			2.7 - 3.6		0.8	
V _{ОН}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	1.65 - 3.6	V _{CC} - 0.2		
	A Outputs	$I_{OH} = -2 \text{ mA}$	1.65	1.2		
		$I_{OH} = -4 \text{ mA}$	2.3	1.9		
		$I_{OH} = -6 \text{ mA}$	2.3	1.7		
			3.0	2.4		
		$I_{OH} = -8 \text{ mA}$	2.7	2		
		$I_{OH} = -12 \text{ mA}$	3.0	2		V
	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	1.65 - 3.6	V _{CC} - 0.2		V
	B Outputs	$I_{OH} = -4 \text{ mA}$	1.65	1.2		
		$I_{OH} = -6 \text{ mA}$	2.3	2.0		
		$I_{OH} = -12 \text{ mA}$	2.3	1.7		
			2.7	2.2		
			3.0	2.4		
		$I_{OH} = -24 \text{ mA}$	3.0	2		
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μA	1.65 - 3.6		0.2	
	A Outputs	I _{OL} = 2 mA	1.65		0.45	
		I _{OL} = 4 mA	2.3		0.4	
		I _{OL} = 6 mA	2.3		0.55	
			3.0		0.55	
		I _{OL} = 8 mA	2.7		0.6	
		I _{OL} = 12 mA	3.0		0.8	V
	LOW Level Output Voltage	I _{OL} = 100 μA	1.65 - 3.6		0.2	
	B Outputs	I _{OL} = 4 mA	1.65		0.45	
		I _{OL} = 6 mA	2.3		0.4	
		I _{OL} = 12 mA	2.3		0.7	
			2.7		0.4	
		I _{OL} = 24 mA	3.0		0.55	
l _I	Input Leakage Current	$0 \le V_I \le 3.6V$	1.65 - 3.6		±5.0	μА
l _{oz}	3-STATE Output Leakage	$0 \le V_O \le 3.6V$, $V_I = V_{IH}$ or V_{IL}	1.65 - 3.6		±10	μА

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V _{CC} (V)	Min	Max	Units
l _{OFF}	Power Off Leakage Current	$0V \le (V_I, V_O) \le 3.6V$	0		10	mA
I _{cc}	Quiescent Supply Current	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6		40	μА
ΔI_{CC}	Increase in I _{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.7 - 3.6		750	μА

AC Electrical Characteristics

			$\text{T}_{\text{A}} = -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}, \text{R}_{\text{L}} = 500\Omega$							
0	Parameter		C _L = 50 pF			C _L = 30 pF				
Symbol		V _{CC} = 3.3	3V ± 0.3V	V _{CC} =	2.7V	V _{CC} = 2.	.5 ± 0.2V	V _{CC} = 1.8	V ± 0.15V	Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t _{PHL} , t _{PLH}	Propagation Delay A to B	1.3	3.0	1.5	3.5	1	3.0	1.5	6.0	
	Propagation Delay B to A	1.3	3.9	1.5	4.8	1	4.3	1.5	8.6	ns
t _{PZL} , t _{PZH}	Output Enable Time A to B	1.3	4.3	1.5	5.4	1.0	4.9	1.5	9.3	
	Output Enable Time B to A	1.3	4.7	1.5	6.2	1.0	5.7	1.5	9.8	ns
t _{PLZ} , t _{PHZ}	Output Disable Time A to B	1.3	4.2	1.5	4.7	1.0	4.2	1.5	7.6	
	Output Disable Time B to A	1.3	4.6	1.5	5.3	1.0	4.8	1.5	8.6	ns

Capacitance

Symbol	Parameter		Conditions	T _A = -	Units	
Зупівої	raiametei		Conditions	V _{CC}	Typical	Ullits
C _{IN}	Input Capacitance		$V_I = 0V$ or V_{CC}	3.3	6	pF
C _{IO}	Input, Output Capacitance		$V_O = 0V$ or V_{CC}	3.3	7	pF
C _{PD}	Power Dissipation Capacitance	Outputs Enabled	f = 10 MHz, C _L = 50 pF	3.3	20	pF
i				2.5	20	ρı

AC Loading and Waveforms

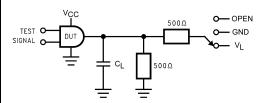


TABLE 1. Values for Figure 1

TEST	SWITCH
t _{PLH} , t _{PHL}	Open
t_{PZL} , t_{PLZ}	V_L
t _{PZH} , t _{PHZ}	GND

FIGURE 1. AC Test Circuit

TABLE 2. Variable Matrix (Input Characteristics: f = 1MHz; $t_r=t_f=2ns;\ Z_O=50\Omega)$

Symbol	V _{CC}							
Symbol	$\textbf{3.3V} \pm \textbf{0.3V}$	2.7V	$\textbf{2.5} \pm \textbf{0.2V}$	1.8V ± 0.15V				
V _{mi}	1.5V	1.5V	V _{CC} /2	V _{CC} /2				
V _{mo}	1.5V	1.5V	V _{CC} /2	V _{CC} /2				
V _X	V _{OL} + 0.3V	V _{OL} + 0.3V	V _{OL} + 0.15V	V _{OL} + 0.15V				
V _Y	V _{OH} – 0.3V	V _{OH} – 0.3V	V _{OH} – 0.15V	V _{OH} – 0.15V				
V _L	6V	6V	V _{CC} *2	V _{CC} *2				

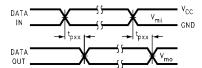


FIGURE 2. Waveform for Inverting and Non-inverting Functions

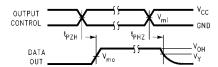


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

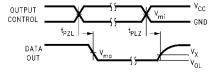


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Physical Dimensions inches (millimeters) unless otherwise noted 0.40 TYP 30 1 1 1 1 1 1 2 5 6.10±0.10 4.60 9.20 8.10 -B-0.2 C B A ALL LEAD TIPS PIN #1 IDENT 0.50 LAND PATTERN RECOMMENDATION 0.1 C SEE DETAIL A 0.90+0.15 ALL LEAD TIPS -C-0.09-0.20 0.10+0.05 ◆ 0.13 **(9)** A B(**9**) C(**9**) 12.00° TOP & BOTTOM DIMENSIONS ARE IN MILLIMETERS GAGE PLANE NOTES: 1.25 A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB REF NOTE 6, DATE 7/93. B. DIMENSIONS ARE IN MILLIMETERS. C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS. SEATING PLANE 0.60±0.10 D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982. MTD48RevB1 DETAIL A 48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Package Number MTD48

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