August 1999 Revised October 1999

74ACT16543 **16-Bit Registered Transceiver with 3-STATE Outputs**

General Description

FAIRCHILD

SEMICONDUCTOR

The ACT16543 contains sixteen non-inverting transceivers containing two sets of D-type registers for temporary storage of data flowing in either direction. Each byte has separate control inputs which can be shorted together for full 16-bit operation. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent input and output control in either direction of data flow

Features

- Independent registers for A and B buses
- Separate controls for data flow in each direction
- Back-to-back registers for storage
- Multiplexed real-time and stored data transfers ■ Separate control logic for each byte
- Outputs source/sink 24 mA

Connection Diagram

TTL-compatible inputs

Ordering Code:

Order Number	Package Number	Package Description		
74ACT16543SSC	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide		
74ACT16543MTD MTD56 56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide				
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.				

Logic Symbol



Pin Descriptions

Pin Names	Descriptions
OEAB	A-to-B Output Enable Input (Active LOW)
OEBAn	B-to-A Output Enable Input (Active LOW)
CEAB _n	A-to-B Enable Input (Active LOW)
CEBAn	B-to-A Enable Input (Active LOW)
LEAB _n	A-to-B Latch Enable Input (Active LOW)
LEBAn	B-to-A Latch Enable Input (Active LOW)
A ₀ -A ₁₅	A-to-B Data Inputs or
	B-to-A 3-STATE Outputs
B ₀ -B ₁₅	B-to-A Data Inputs or
	A-to-B 3-STATE Outputs

		, , , , , , , , , , , , , , , , , , , 		
EAB, -	1	\bigcirc	56	- OEBA
EAB, -	2		55	LEBA
EAB, -	3		54	CEBA
GND -	4		53	- GND
A0 -	5		52	— B _n
A1 -	6		51	— B ₁
v _{cc} —	7		50	- v _{cc}
A2 -	8		49	- B ₂
A3 -	9		48	— В3
Α4 -	10		47	— в4
GND —	11		46	- GND
A5 —	12		45	— B ₅
A ₆ —	13		44	— В _б
A7 —	14		43	— В ₇
A ₈ —	15		42	— В ₈
A9 —	16		41	— В ₉
A ₁₀ —	17		40	— B ₁₀
GND —	18		39	- GND
A ₁₁ —	19		38	— B ₁₁
A ₁₂ —	20		37	— B ₁₂
A ₁₃ —	21		36	— B ₁₃
v _{cc} —	22		35	- v _{cc}
A ₁₄ —	23		34	— B _{1.4}
A ₁₅ —	24		33	- B ₁₅
GND —	25		32	- GND
EAB ₂	26		31	- CEBA ₂
EAB ₂	27		30	- LEBA2
DEAB ₂ —	28		29	- OEBA ₂
				1

FACT™ is a trademark of Fairchild Semiconductor Corporation.

© 1999 Fairchild Semiconductor Corporation DS500301

Functional Description

The ACT16543 contains sixteen non-inverting transceivers with 3-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins may be shorted together to obtain full 16-bit operation. The following description applies to each byte. For data flow from A to B, for example, the A-to-B Enable (CEAB_n) input must be LOW in order to enter data from A₀–A₁₅ or take data from B₀–B₁₅, as indicated in the Data I/O Control Table. With CEAB_n LOW, a LOW signal on the A-to-B Latch Enable (CEAB_n) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the LEAB_n and OEAB_n both LOW, the 3-STATE B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the CEBA_n, LEBA_n and OEBA_n inputs.

Data I/O Control Table

	Inputs		Latch Status	Output	
CEAB _n	LEAB _n	$\overline{\text{OEAB}}_n$	(Byte n)	Buffers (Byte n)	
Н	Х	Х	Latched	High Z	
Х	н	Х	Latched	—	
L	L	Х	Transparent	—	
Х	Х	н	—	High Z	
L	Х	L	—	Driving	

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{\text{CEBA}_n}, \overline{\text{LEBA}_n}$ and $\overline{\text{OEBA}_n}$

Logic Diagrams Byte 1 Byte 2 (0:7) (8:15) DETAIL A × 7 DETAIL A x 7 OEBA OEBA CEAB OEAB -CEBA CEBA LEBA LEBA LEAB, LEAB₂

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Supply Voltage (V _{CC})	-0.5V to +7.0V
DC Input Diode Current (IIK)	
$V_{I} = -0.5V$	–20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Output Diode Current (I _{OK})	
$V_{O} = -0.5V$	–20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V _O)	–0.5V to $V_{CC}^{} + 0.5V$
DC Output Source/Sink Current (I _O)	±50 mA
DC V_{CC} or Ground Current	
per Output Pin	±50 mA
Storage Temperature	$-65^{\circ}C$ to $+150^{\circ}C$

Recommended Operating Conditions

Supply Voltage (V _{CC})	4.5V to 5.5V
Input Voltage (V _I)	0V to V_{CC}
Output Voltage (V _O)	0V to V_{CC}
Operating Temperature (T _A)	$-40^{\circ}C$ to $+85^{\circ}C$
Minimum Input Edge Rate ($\Delta V/\Delta t$)	125 mV/ns
V _{IN} from 0.8V to 2.0V	
V _{CC} @ 4.5V, 5.5V	

74ACT16543

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Paramotor	V _{CC}	V_{CC} $T_A = +25^{\circ}C$		$T_A = -40^{\circ}C \text{ to}+85^{\circ}C$	Unito	Conditions	
Cymbol I arameter		(V)	Typ Guaranteed Limits		Units	conditions		
VIH	Minimum HIGH	4.5	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$	
	Input Voltage	5.5	1.5	2.0	2.0	v	or $V_{CC} - 0.1V$	
VIL	Maximum LOW	4.5	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$	
	Input Voltage	5.5	1.5	0.8	0.8	v	or $V_{CC} - 0.1V$	
V _{OH}	Minimum HIGH	4.5	4.49	4.4	4.4	V	L _ 50 ··· A	
	Output Voltage	5.5	5.49	5.4	5.4	v	$I_{OUT} = -50 \mu A$	
							$V_{IN} = V_{IL} \text{ or } V_{IH}$	
		4.5		3.86	3.76	V	$I_{OH} = -24 \text{ mA}$	
		5.5		4.86	4.76		I _{OH} = -24 mA (Note 2)	
V _{OL}	Maximum LOW	4.5	0.001	0.1	0.1	V		
	Output Voltage	5.5	0.001	0.1	0.1	v	$I_{OUT} = 50 \ \mu A$	
							$V_{IN} = V_{IL} or V_{IH}$	
		4.5		0.36	0.44	V	I _{OL} = 24 mA	
		5.5		0.36	0.44		I _{OL} = 24 mA (Note 2)	
I _{OZT}	Maximum I/O	F F		±0 E	+5.0		$V_I = V_{IL}, V_{IH}$	
	Leakage Current	5.5		±0.5	±5.0	μΑ	$V_{O} = V_{CC}, GND$	
I _{IN}	Maximum Input	5.5		+0.1	+1.0		$V_I = V_{CC},$	
	Leakage Current	5.5		±0.1	±1.0	μΑ	GND	
I _{CCT}	Maximum I _{CC} /Input	5.5	0.6		1.5	mA	$V_I = V_{CC} - 2.1V$	
I _{CC}	Max Quiescent				90.0		$V_{IN} = V_{CC}$	
	Supply Current	5.5		8.0	80.0	μΑ	or GND	
I _{OLD}	Minimum Dynamic				75	mA	V _{OLD} = 1.65V Max	
I _{OHD}	Output Current (Note 3)	5.5			-75	mA	V _{OHD} = 3.85V Min	

Note 2: All outputs loaded; thresholds associated with output under test. Note 3: Maximum test duration 2.0 ms; one output loaded at a time.

www.fairchildsemi.com

74ACT16543

AC Electrical Characteristics

Symbol	Parameter	V _{cc} (V)	T _A = +25°C C _L = 50 pF			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$ $C_L = 50 \text{ pF}$		Units
		(Note 4)	Min	Тур	Max	Min	Max	
t _{PLH}	Propagation Delay		3.8	5.9	8.3	3.0	9.0	
t _{PHL}	Transparent Mode	5.0	3.5	5.5	7.9	2.6	8.5	ns
	A _n to B _n or B _n to A _n							
t _{PLH}	Propagation Delay		4.7	6.9	9.8	3.4	10.8	
t _{PHL}	LEBA _n , LEAB _n	5.0	3.9	6.3	9.0	3.1	9.8	ns
	to A _n , B _n							
t _{PZH}	Output Enable Time		4.2	6.3	9.2	3.0	9.9	
t _{PZL}	\overline{OEBA}_n or \overline{OEAB}_n to A_n or B_n	5.0	4.9	7.3	10.3	3.6	10.3	ns
	$\overline{\text{CEBA}}_n$ or $\overline{\text{CEAB}}_n$ to A_n or B_n							
t _{PHZ}	Output Disable Time		2.8	5.2	8.0	2.1	8.3	
t _{PLZ}	\overline{OEBA}_n or \overline{OEAB}_n to A_n or B_n	5.0	2.6	5.0	7.6	2.0	8.1	ns
	\overline{CEBA}_n or \overline{CEAB}_n to A_n or B_n							

Note 4: Voltage Range 5.0 is $5.0V \pm 0.5V$.

AC Operating Requirements

Symbol	Parameter	V _{CC} (V) (Note 5)	T _A = +25°C C _L = 50 pF Guarar	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$ $C_L = 50 \text{ pF}$	Units
t _S	Setup Time, HIGH or LOW A_n or B_n to \overline{LEBA}_n or \overline{LEAB}_n	5.0	3.0	3.0	ns
t _H	Hold Time, HIGH or LOW A_n or B_n to \overline{LEBA}_n or \overline{LEAB}_n	5.0	1.5	1.5	ns
t _W	Latch Enable, B to A Pulse Width, LOW	5.0	4.0	4.0	ns

Note 5: Voltage Range 5.0 is $5.0V\pm0.5V$

Capacitance

Symbol	Parameter	Тур	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C _{PD}	Power Dissipation.Capacitance	95.0	pF	$V_{CC} = 5.0V$





74ACT16543 16-Bit Registered Transceiver with 3-STATE Outputs

www.fairchildsemi.com