

## 74ACT16373 16-Bit Transparent Latch with 3-STATE Outputs

### General Description

The ACT16373 contains sixteen non-inverting latches with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is low, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the outputs are in high Z state.

### Features

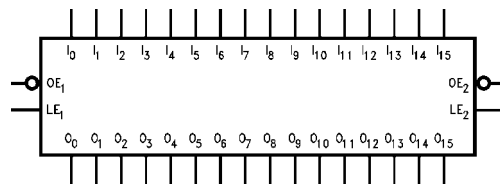
- Separate control logic for each byte
- 16-bit version of the ACT373
- Outputs source/sink 24 mA
- TTL-compatible inputs

### Ordering Code:

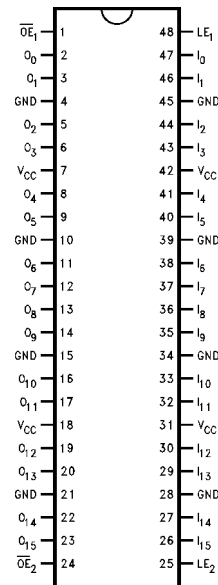
Order Number	Package Number	Package Description
74ACT16373SSC	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ACT16373MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

### Logic Symbol



### Connection Diagram



### Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
$LE_n$	Latch Enable Input
$I_0-I_{15}$	Inputs
$O_0-O_{15}$	Outputs

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### Functional Description

The ACT16373 contains sixteen D-type latches with 3-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable ( $LE_n$ ) input is HIGH, data on the  $D_n$  enters the latches. In this condition the latches are transparent, i.e., a latch output will change states each time its D input changes. When  $LE_n$  is LOW, the latches store information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of  $LE_n$ . The 3-STATE standard outputs are controlled by the Output Enable ( $\overline{OE}_n$ ) input. When  $\overline{OE}_n$  is LOW, the standard outputs are in the 2-state mode. When  $\overline{OE}_n$  is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

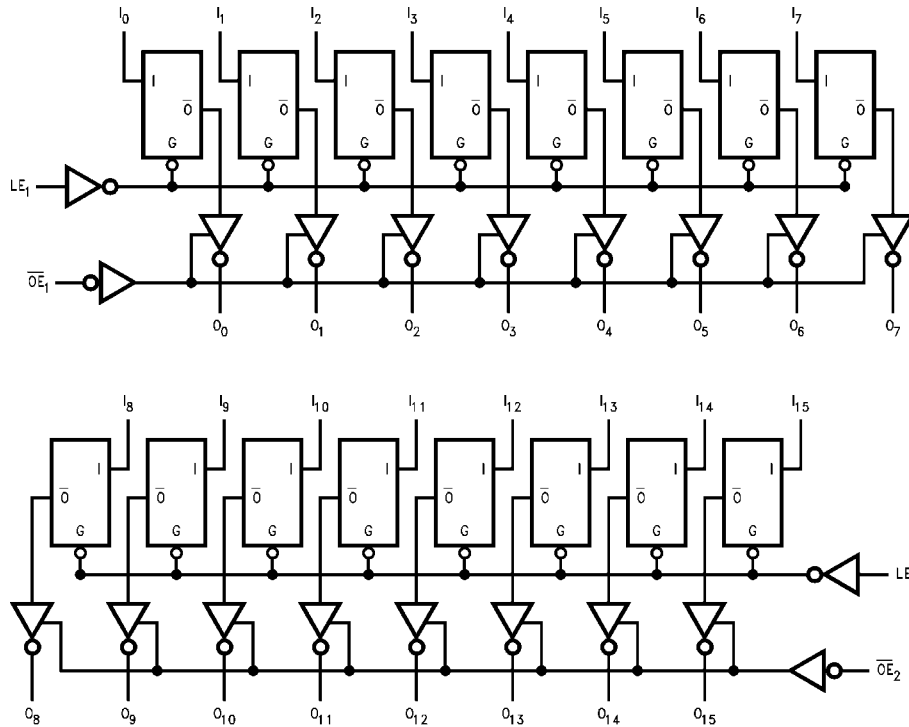
### Truth Tables

Inputs			Outputs
$LE_1$	$\overline{OE}_1$	$I_0-I_7$	$O_0-O_7$
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	(Previous)

Inputs			Outputs
$LE_2$	$\overline{OE}_2$	$I_8-I_{15}$	$O_8-O_{15}$
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	(Previous)

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance  
 Previous = previous output prior to HIGH-to-LOW transition of LE

### Logic Diagrams



**Absolute Maximum Ratings**(Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source/Sink Current ( $I_O$ )	+50 mA
DC $V_{CC}$ or Ground Current per Output Pin	+50 mA
Junction Temperature	+140°C
Storage Temperature	-65°C to +150°C

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	125 mV/ns
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Typ	Guaranteed Limits				
$V_{IH}$	Minimum HIGH Input Voltage	4.5	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		5.5	1.5	2.0	2.0			
$V_{IL}$	Maximum LOW Input Voltage	4.5	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		5.5	1.5	0.8	0.8			
$V_{OH}$	Minimum HIGH Output Voltage	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50 \mu A$	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA (Note 2)}$	
		5.5		4.86	4.76			
$V_{OL}$	Maximum LOW Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50 \mu A$	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA (Note 2)}$	
		5.5		0.36	0.44			
$I_{OZ}$	Maximum 3-STATE Leakage Current	5.5		$\pm 0.5$	$\pm 5.0$	$\mu A$	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, \text{GND}$	
$I_{IN}$	Maximum Input Leakage Current	5.5		$\pm 0.1$	$\pm 1.0$	$\mu A$	$V_I = V_{CC}, \text{GND}$	
$I_{CCT}$	Maximum $I_{CC}/\text{Input}$	5.5	0.6		1.5	mA	$V_I = V_{CC} - 2.1V$	
$I_{CC}$	Max Quiescent Supply Current	5.5		8.0	80.0	$\mu A$	$V_{IN} = V_{CC}$ or GND	
$I_{OLD}$	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V \text{ Max}$	
$I_{OHD}$	Output Current (Note 3)				-75	mA	$V_{OHD} = 3.85V \text{ Min}$	

**Note 2:** All outputs loaded; thresholds associated with output under test.

**Note 3:** Maximum test duration 2.0 ms; one output loaded at a time.

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V) (Note 4)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	5.0	3.1	5.3	7.9	3.1	8.4	ns
t <sub>PHL</sub>	D <sub>n</sub> to O <sub>n</sub>		2.6	4.6	7.3	2.6	7.8	
t <sub>PLH</sub>	Propagation Delay	5.0	3.1	5.4	7.9	3.2	8.4	ns
t <sub>PHL</sub>	LE to O <sub>n</sub>		2.8	4.9	7.3	2.8	7.8	
t <sub>PZH</sub>	Output Enable	5.0	2.5	4.7	7.4	2.5	7.9	ns
t <sub>PZL</sub>	Delay		2.7	4.8	7.5	2.7	8.0	
t <sub>PHZ</sub>	Output Disable	5.0	2.1	5.1	7.9	2.1	8.2	ns
t <sub>PLZ</sub>	Delay		2.0	4.5	7.4	2.0	7.9	

Note 4: Voltage Range 5.0 is 5.0V ± 0.5V.

## AC Operating Requirements

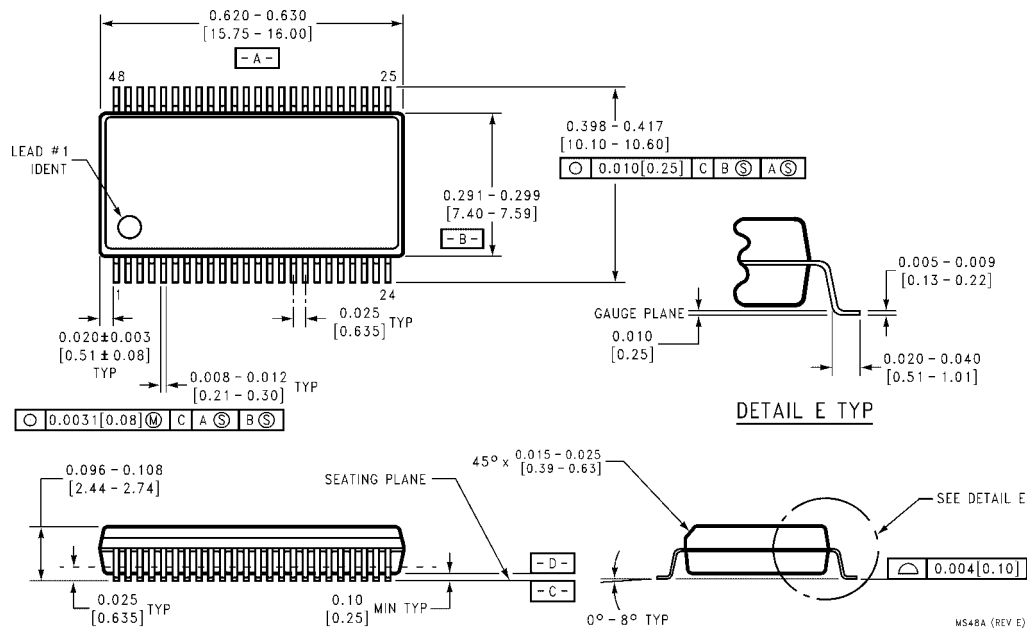
Symbol	Parameter	V <sub>CC</sub> (V) (Note 5)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF	T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF	Units
			Guaranteed Minimum		
t <sub>S</sub>	Setup Time, HIGH or LOW, Input to Clock	5.0	3.0	3.0	ns
t <sub>H</sub>	Hold time, HIGH or LOW, Input to Clock	5.0	1.5	1.5	ns
t <sub>W</sub>	CS Pulse Width, HIGH or LOW	5.0	4.0	4.0	ns

Note 5: Voltage Range 5.0 is 5.0V ± 0.5V

## Capacitance

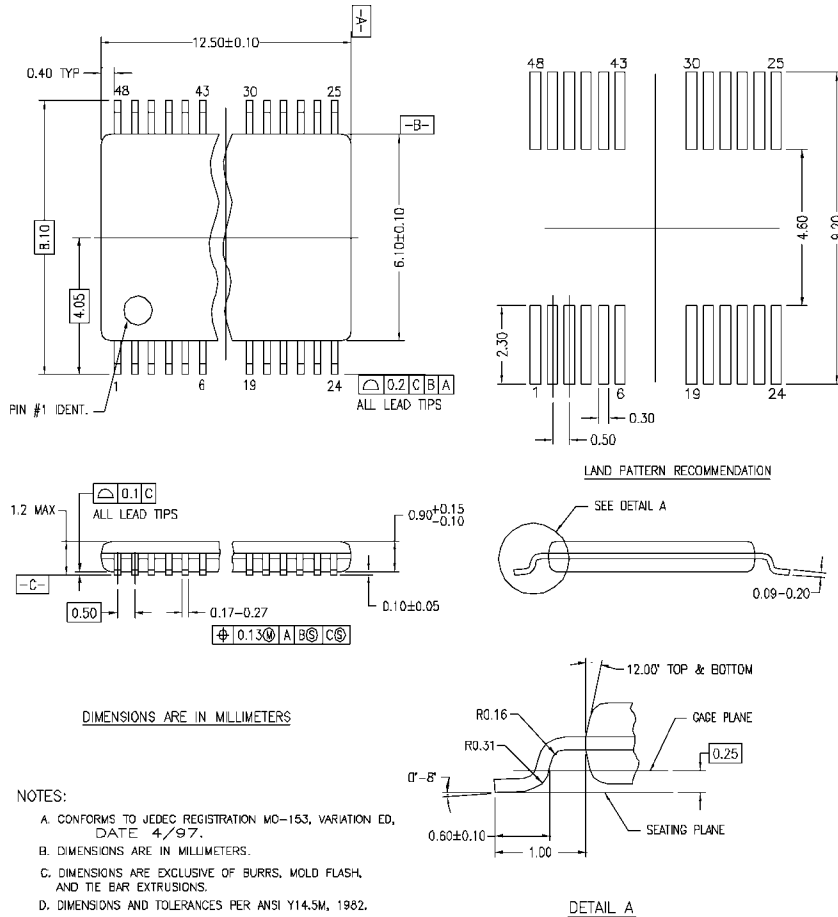
Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = 5.0V
C <sub>PD</sub>	Power Dissipation Capacitance	30	pF	V <sub>CC</sub> = 5.0V

**Physical Dimensions** inches (millimeters) unless otherwise noted



**48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide  
Package Number MS48A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION ED, DATE 4/97.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48REV C

**48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48**

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