

## Functional Description

The AC／ACT161 count in modulo－16 binary sequence． From state 15 （HHHH）they increment to state 0 （LLLL）． The clock inputs of all flip－flops are driven in parallel through a clock buffer．Thus all changes of the Q outputs （except due to Master Reset of the AC／ACT161）occur as a result of，and synchronous with，the LOW－to－HIGH transi－ tion of the CP input signal．The circuits have four funda－ mental modes of operation，in order of precedence： asynchronous reset，parallel load，count－up and hold．Five control inputs－Master Reset，Parallel Enable（ $\overline{\mathrm{PE}}$ ），Count Enable Parallel（CEP）and Count Enable Trickle（CET）－ determine the mode of operation，as shown in the Mode Select Table．A LOW signal on $\overline{\mathrm{MR}}$ overrides all other inputs and asynchronously forces all outputs LOW．A LOW signal on $\overline{\mathrm{PE}}$ overrides counting and allows information on the Parallel Data $\left(P_{n}\right)$ inputs to be loaded into the flip－flops on the next rising edge of CP．With $\overline{\mathrm{PE}}$ and $\overline{\mathrm{MR}}$ HIGH，CEP and CET permit counting when both are HIGH．Conversely， a LOW signal on either CEP or CET inhibits counting．
The AC／ACT161 use D－type edge－triggered flip－flops and changing the $\overline{P E}, \mathrm{CEP}$ ，and CET inputs when the CP is in either state does not cause errors，provided that the recom－ mended setup and hold times，with respect to the rising edge of CP，are observed．
The Terminal Count（TC）output is HIGH when CET is HIGH and counter is in state 15．To implement synchro－ nous multistage counters，the TC outputs can be used with the CEP and CET inputs in two different ways．
Figure 1 shows the connections for simple ripple carry，in which the clock period must be longer than the CP to TC delay of the first stage，plus the cumulative $\overline{\mathrm{CET}}$ to $\overline{\mathrm{TC}}$ delays of the intermediate stages，plus the $\overline{\mathrm{CET}}$ to CP setup time of the last stage．This total delay plus setup time sets the upper limit on clock frequency．For faster clock rates，the carry lookahead connections shown in Figure 2 are recommended．In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min in the Up mode，or min to max in the Down mode，to start its final cycle．Since this final cycle requires 16 clocks to com－ plete，there is plenty of time for the ripple to progress through the intermediate stages．The critical timing that lim－
its the clock period is the CP to $\overline{\mathrm{TC}}$ delay of the first stage plus the $\overline{\mathrm{CEP}}$ to CP setup time of the last stage．The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip－flops，registers or counters．
Logic Equations：Count Enable $=\mathrm{CEP} \cdot \mathrm{CET} \cdot \overline{\mathrm{PE}}$

$$
\mathrm{TC}=\mathrm{Q}_{0} \cdot \mathrm{Q}_{1} \cdot \mathrm{Q}_{2} \cdot \mathrm{Q}_{3} \cdot \mathrm{CET}
$$

## Mode Select Table

| $\overline{\text { PE }}$ | CET | CEP | Action on the Rising <br> Clock Edge（ - ） |
| :---: | :---: | :---: | :--- |
| X | X | X | Reset（Clear） |
| L | X | X | Load $\left(\mathrm{P}_{\mathrm{n}} \rightarrow \mathrm{Q}_{\mathrm{n}}\right)$ |
| H | H | H | Count（Increment） |
| H | L | X | No Change（Hold） |
| H | X | L | No Change（Hold） |

$\mathrm{H}=\mathrm{HIGH}$ Voltage Level
L＝LOW Voltage Level
X＝Immaterial

## State Diagram




FIGURE 1．Multistage Counter with Ripple Carry


FIGURE 2．Multistage Counter with Lookahead Carry



## DC Electrical Characteristics for ACT

| Symbol | Parameter | $\mathrm{V}_{\text {cc }}$ | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | Units | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | (V) | Typ | Guaranteed Limits |  |  |  |
| $\overline{\mathrm{V}_{\mathrm{IH}}}$ | Minimum HIGH Level Input Voltage | $\begin{aligned} & 4.5 \\ & 5.5 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & \hline 2.0 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 2.0 \end{aligned}$ | V | $\begin{aligned} & \mathrm{V}_{\text {OUT }}=0.1 \mathrm{~V} \\ & \text { or } \mathrm{V}_{\mathrm{CC}}-0.1 \mathrm{~V} \end{aligned}$ |
| $\overline{\mathrm{V}} \mathrm{IL}$ | Maximum LOW Level Input Voltage | $\begin{aligned} & 4.5 \\ & 5.5 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & \hline 0.8 \\ & 0.8 \end{aligned}$ | $\begin{aligned} & \hline 0.8 \\ & 0.8 \end{aligned}$ | V | $\begin{aligned} & \mathrm{V}_{\text {OUT }}=0.1 \mathrm{~V} \\ & \text { or } \mathrm{V}_{\mathrm{CC}}-0.1 \mathrm{~V} \end{aligned}$ |
| $\overline{\mathrm{V} \text { OH }}$ | Minimum HIGH Level Output Voltage | $\begin{aligned} & 4.5 \\ & 5.5 \end{aligned}$ | $\begin{aligned} & 4.49 \\ & 5.49 \end{aligned}$ | $\begin{aligned} & 4.4 \\ & 5.4 \end{aligned}$ | $\begin{aligned} & 4.4 \\ & 5.4 \end{aligned}$ | V | $\mathrm{l}_{\text {OUT }}=-50 \mu \mathrm{~A}$ |
|  |  | $\begin{aligned} & 4.5 \\ & 5.5 \end{aligned}$ |  | $\begin{aligned} & 3.86 \\ & 4.86 \end{aligned}$ | $\begin{aligned} & 3.76 \\ & 4.76 \end{aligned}$ | V | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IL}} \text { or } \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{I}_{\mathrm{OH}}=-24 \mathrm{~mA} \\ & \mathrm{I}_{\mathrm{OH}}=-24 \mathrm{~mA}(\text { Note } 5) \end{aligned}$ |
| $\mathrm{V}_{\text {OL }}$ | Maximum LOW Level Output Voltage | $\begin{aligned} & 4.5 \\ & 5.5 \end{aligned}$ | $\begin{aligned} & \hline 0.001 \\ & 0.001 \end{aligned}$ | $\begin{aligned} & \hline 0.1 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & \hline 0.1 \\ & 0.1 \end{aligned}$ | V | $\mathrm{I}_{\text {OUT }}=50 \mu \mathrm{~A}$ |
|  |  | $\begin{aligned} & 4.5 \\ & 5.5 \end{aligned}$ |  | $\begin{aligned} & 0.36 \\ & 0.36 \end{aligned}$ | $\begin{aligned} & 0.44 \\ & 0.44 \end{aligned}$ | V | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IL}} \text { or } \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{IOL}_{2}=24 \mathrm{~mA} \\ & \mathrm{I}_{\mathrm{OL}}=24 \mathrm{~mA}(\text { Note } 5) \end{aligned}$ |
| $\overline{I_{\text {I }}}$ | Maximum Input Leakage Current | 5.5 |  | $\pm 0.1$ | $\pm 1.0$ | $\mu \mathrm{A}$ | $\mathrm{V}_{\mathrm{l}}=\mathrm{V}_{\mathrm{CC}}, \mathrm{GND}$ |
| ${ }_{\text {ICCT }}$ | Maximum $\mathrm{I}_{\mathrm{CC}} /$ Input | 5.5 | 0.6 |  | 1.5 | mA | $\mathrm{V}_{1}=\mathrm{V}_{\text {CC }}-2.1 \mathrm{~V}$ |
| TOLD | Minimum Dynamic | 5.5 |  |  | 75 | mA | $\mathrm{V}_{\text {OLD }}=1.65 \mathrm{~V}$ Max |
| IOHD | Output Current (Note 6) | 5.5 |  |  | -75 | mA | $\mathrm{V}_{\text {OHD }}=3.85 \mathrm{~V}$ Min |
| $\mathrm{I}_{\text {CC }}$ | Maximum Quiescent Supply Current | 5.5 |  | 4.0 | 40.0 | $\mu \mathrm{A}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{CC}} \\ & \text { or GND } \end{aligned}$ |

Note 5: All outputs loaded; thresholds on input associated with output under test.
Note 6: Maximum test duration 2.0 ms , one output loaded at a time.

## AC Electrical Characteristics for AC

| Symbol | Parameter | $\mathrm{V}_{\mathrm{cc}}$ <br> (V) <br> (Note 7) | $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \end{aligned}$ |  |  | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \end{gathered}$ |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max | Min | Max |  |
| $\mathrm{f}_{\text {MAX }}$ | Maximum Count Frequency | $\begin{aligned} & 3.3 \\ & 5.0 \end{aligned}$ | $\begin{gathered} \hline 70 \\ 110 \end{gathered}$ | $\begin{aligned} & 111 \\ & 167 \end{aligned}$ |  | $\begin{aligned} & \hline 60 \\ & 95 \end{aligned}$ |  | MHz |
| $\overline{t_{\text {PLH }}}$ | Propagation Delay CP to $\mathrm{Q}_{\mathrm{n}}$ ( $\overline{\mathrm{PE}}$ Input HIGH or LOW) | $\begin{aligned} & 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & \hline 2.0 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & 7.0 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 12 \\ & 9.0 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 1.0 \end{aligned}$ | $\begin{gathered} 13.5 \\ 9.5 \end{gathered}$ | ns |
| $\overline{t_{\text {PHL }}}$ | Propagation Delay CP to $Q_{n}$ ( $\overline{\mathrm{PE}}$ Input HIGH or LOW) | $\begin{aligned} & 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & 7.0 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & \hline 12 \\ & 9.5 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & \hline 13 \\ & 10 \end{aligned}$ | ns |
| $\overline{t_{\text {PLH }}}$ | Propagation Delay CP to TC | $\begin{aligned} & 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & \hline 3.0 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & 9 \\ & 6 \end{aligned}$ | $\begin{gathered} \hline 15 \\ 10.5 \end{gathered}$ | $\begin{aligned} & 2.5 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & \hline 16.5 \\ & 11.5 \end{aligned}$ | ns |
| ${ }_{\text {t }}$ | Propagation Delay CP to TC | $\begin{aligned} & \hline 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & \hline 3.5 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & \hline 8.5 \\ & 6.5 \end{aligned}$ | $\begin{aligned} & \hline 14 \\ & 11 \end{aligned}$ | $\begin{aligned} & 2.5 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & \hline 15.5 \\ & 11.5 \end{aligned}$ | ns |
| $\overline{t_{\text {PLH }}}$ | Propagation Delay CET to TC | $\begin{aligned} & 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & 5.5 \\ & 3.5 \end{aligned}$ | $\begin{aligned} & 9.5 \\ & 6.5 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & 11 \\ & 7.5 \end{aligned}$ | ns |
| $\overline{t_{\text {PHL }}}$ | Propagation Delay CET to TC | $\begin{aligned} & 3.3 \\ & 5.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & 2.5 \\ & 2.0 \end{aligned}$ | $\begin{gathered} \hline 6.5 \\ 5 \end{gathered}$ | $\begin{gathered} \hline 11 \\ 8.5 \\ \hline \end{gathered}$ | $\begin{aligned} & 2.0 \\ & 1.5 \end{aligned}$ | $\begin{gathered} \hline 12.5 \\ 9.5 \end{gathered}$ | ns |
| $\overline{t_{\text {PHL }}}$ | $\begin{aligned} & \text { Propagation Delay } \\ & \overline{\mathrm{MR}} \text { to } Q_{n} \end{aligned}$ | $\begin{aligned} & 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & \hline 6.5 \\ & 5.5 \end{aligned}$ | $\begin{aligned} & \hline 12 \\ & 9.5 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 1.5 \end{aligned}$ | $\begin{gathered} 13.5 \\ 10 \end{gathered}$ | ns |
| ${ }_{\text {tPHL }}$ | $\begin{aligned} & \text { Propagation Delay } \\ & \overline{\mathrm{MR}} \text { to } \mathrm{TC} \end{aligned}$ | $\begin{aligned} & \hline 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & \hline 3.5 \\ & 2.5 \end{aligned}$ | $\begin{aligned} & 10 \\ & 8.5 \end{aligned}$ | $\begin{aligned} & \hline 15 \\ & 13 \end{aligned}$ | $\begin{aligned} & 3.0 \\ & 2.5 \end{aligned}$ | $\begin{aligned} & \hline 17.5 \\ & 13.5 \end{aligned}$ | ns |
| Note 7: Voltage Range 3.3 is $3.3 \mathrm{~V} \pm 0.3 \mathrm{~V}$ Voltage Range 5.0 is $5.0 \mathrm{~V} \pm 0.5 \mathrm{~V}$ |  |  |  |  |  |  |  |  |



| AC Operating Requirements for ACT |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Symbol | Parameter | $\mathrm{V}_{\mathrm{CC}}$$\mathrm{(V)}$(Note 10) | $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \end{aligned}$ |  | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \end{gathered}$ | Units |
|  |  |  | Typ |  | nteed Minimum |  |
| $\mathrm{t}_{\mathrm{s}}$ | Setup Time, HIGH or LOW $P_{n}$ to CP | 5.0 | 4.0 | 9.5 | 11.5 | ns |
| $\mathrm{t}_{\mathrm{H}}$ | Hold Time, HIGH or LOW $P_{n}$ to CP | 5.0 | -5.0 | 0 | 0 | ns |
| $\mathrm{t}_{\mathrm{s}}$ | $\begin{aligned} & \text { Setup Time, HIGH or LOW } \\ & \overline{\mathrm{PE}} \text { to CP } \end{aligned}$ | 5.0 | 4.0 | 8.5 | 9.5 | ns |
| $\mathrm{t}_{\mathrm{H}}$ | $\begin{aligned} & \text { Hold Time, HIGH or LOW } \\ & \overrightarrow{\text { PE to CP }} \end{aligned}$ | 5.0 | $-5.5$ | -0.5 | -0.5 | ns |
| $\mathrm{t}_{\mathrm{s}}$ | Setup Time, HIGH or LOW CEP or CET to CP | 5.0 | 2.5 | 5.5 | 6.5 | ns |
| $\mathrm{t}_{\mathrm{H}}$ | Hold Time, HIGH or LOW CEP or CET to CP | 5.0 | -3.0 | 0 | 0 | ns |
| $\mathrm{t}_{\mathrm{W}}$ | Clock Pulse Width, (Load) HIGH or LOW | 5.0 | 2.0 | 3.0 | 3.5 | ns |
| $\mathrm{t}_{\mathrm{W}}$ | Clock Pulse Width, (Count) HIGH or LOW | 5.0 | 2.0 | 3.0 | 3.5 | ns |
| $t_{\text {W }}$ | $\overline{\text { MR Pulse Width, LOW }}$ | 5.0 | 3.0 | 3.0 | 7.5 | ns |
| $\mathrm{t}_{\text {REC }}$ | Recovery Time $\overline{\mathrm{MR}}$ to CP | 5.0 | 0 | 0 | 0.5 | ns |

## Capacitance

| Symbol | Parameter | Typ | Units | Conditions |
| :--- | :--- | :---: | :---: | :--- |
| $\mathrm{C}_{\text {IN }}$ | Input Capacitance | 4.5 | pF | $\mathrm{V}_{\mathrm{CC}}=\mathrm{OPEN}$ |
| $\mathrm{C}_{\mathrm{PD}}$ | Power Dissipation Capacitance | 45.0 | pF | $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ |

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION


DIMENSIONS ARE IN MILLIMETERS

NOTES:
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B. DIMENSIONS ARE IN MILLIMETERS
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M16DRevB1


16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M16D


Physical Dimensions inches (millimeters) unless otherwise noted (Continued)


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