

## 3.3V/2.5V 1:9 LVCMOS Clock Fanout Buffer

The MPC9447 is a 3.3V or 2.5V compatible, 1:9 clock fanout buffer targeted for high performance clock tree applications. With output frequencies up to 350 MHz and output skews less than 150 ps, the device meets the needs of most demanding clock applications.

### Features

- 9 LVCMOS Compatible Clock Outputs
- 2 Selectable, LVCMOS Compatible Inputs
- Maximum Clock Frequency of 350 MHz
- Maximum Clock Skew of 150 ps
- Synchronous Output Stop in Logic Low State Eliminates Output Runt Pulses
- High-Impedance Output Control
- 3.3V or 2.5V Power Supply
- Drives up to 18 Series Terminated Clock Lines
- Ambient Temperature Range -40°C to +85°C
- 32 Lead LQFP Packaging
- Supports Clock Distribution in Networking, Telecommunications, and Computer Applications
- Pin and Function Compatible to MPC947

### Functional Description

MPC9447 is specifically designed to distribute LVCMOS compatible clock signals up to a frequency of 350 MHz. Each output provides a precise copy of the input signal with a near zero skew. The outputs buffers support driving of 50Ω terminated transmission lines on the incident edge: each is capable of driving either one parallel terminated or two series terminated transmission lines.

Two selectable independent LVCMOS compatible clock inputs are available, providing support of redundant clock source systems. The MPC9447 CLK\_STOP control is synchronous to the falling edge of the input clock. It allows the start and stop of the output clock signal only in a logic low state, thus eliminating potential output runt pulses. Applying the OE control will force the outputs into high-impedance mode.

All inputs have an internal pull-up or pull-down resistor preventing unused and open inputs from floating. The device supports a 2.5V or 3.3V power supply and an ambient temperature range of -40°C to +85°C. The MPC9447 is pin and function compatible but performance-enhanced to the MPC947.

**MPC9447**

**LOW VOLTAGE  
3.3 V/2.5 V LVCMOS 1:9  
CLOCK FANOUT BUFFER**



**FA SUFFIX**  
32-LEAD LQFP PACKAGE  
CASE 873A



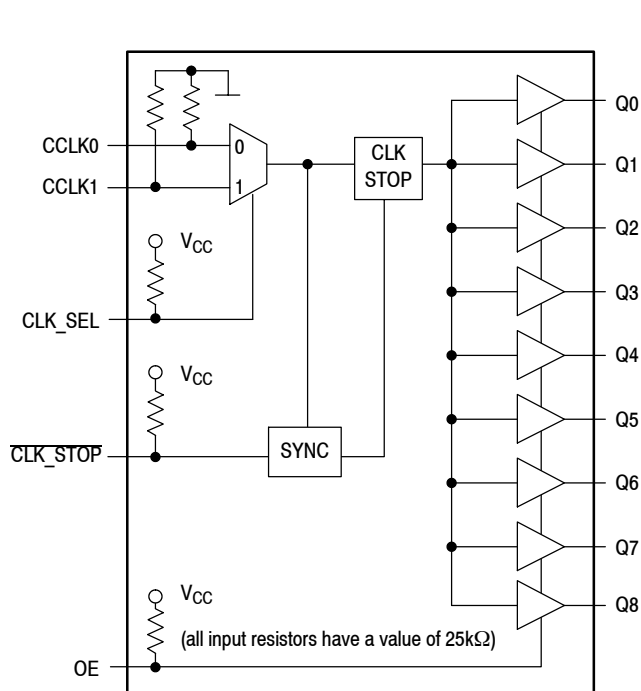


Figure 1. Logic Diagram

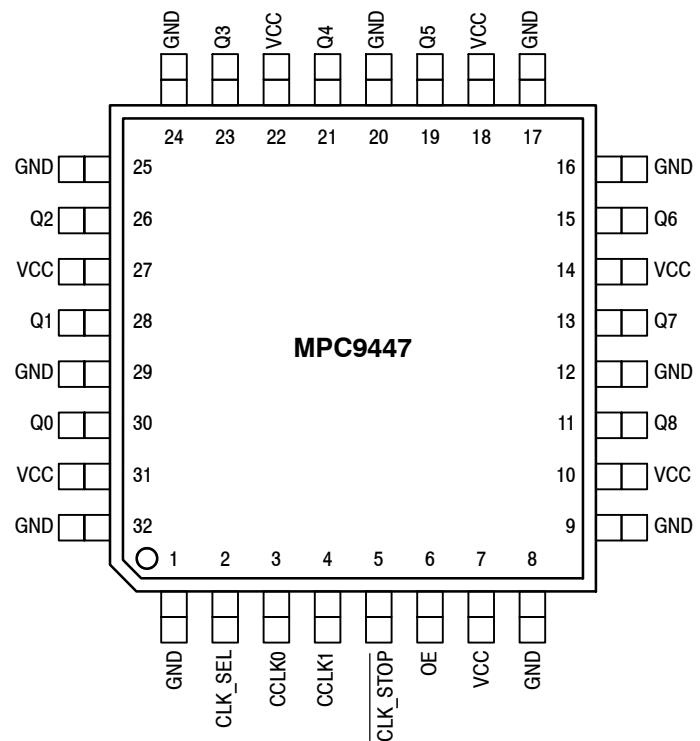


Figure 2. 32-Lead Pinout (Top View)

Table 1. Function Table

Control	Default	0	1
CLK_SEL	1	CLK0 input selected	CLK1 input selected
OE	1	Outputs disabled (high-impedance state) <sup>a</sup>	Outputs enabled
CLK_STOP	1	Outputs synchronously stopped in logic low state	Outputs active

a. OE = 0 will high-impedance tristate all outputs independent on CLK\_STOP

Table 2. Pin Configuration

Pin	I/O	Type	Function
CCLK0	Input	LVC MOS	Clock signal input
CCLK1	Input	LVC MOS	Alternative clock signal input
CLK_SEL	Input	LVC MOS	Clock input select
CLK_STOP	Input	LVC MOS	Clock output enable/disable
OE	Input	LVC MOS	Output enable/disable (high-impedance tristate)
Q0-8	Output	LVC MOS	Clock outputs
GND	Supply	Ground	Negative power supply (GND)
V <sub>CC</sub>	Supply	V <sub>CC</sub>	Positive power supply for I/O and core. All V <sub>CC</sub> pins must be connected to the positive power supply for correct operation

Table 3. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V <sub>TT</sub>	Output termination voltage		V <sub>CC</sub> ÷ 2		V	
MM	ESD protection (Machine model)	200			V	
HBM	ESD protection (Human body model)	2000			V	
LU	Latch-up immunity	200			mA	
C <sub>PD</sub>	Power dissipation capacitance		10		pF	Per output
C <sub>IN</sub>	Input capacitance		4.0		pF	Inputs

**Table 4. Absolute Maximum Ratings<sup>a</sup>**

Symbol	Characteristics	Min	Max	Unit	Condition
V <sub>CC</sub>	Supply Voltage	-0.3	3.9	V	
V <sub>IN</sub>	DC Input Voltage	-0.3	V <sub>CC</sub> + 0.3	V	
V <sub>OUT</sub>	DC Output Voltage	-0.3	V <sub>CC</sub> + 0.3	V	
I <sub>IN</sub>	DC Input Current		±20	mA	
I <sub>OUT</sub>	DC Output Current		±50	mA	
T <sub>S</sub>	Storage temperature	-65	125	°C	

- a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 5. DC Characteristics (V<sub>CC</sub> = 3.3V ± 5%, T<sub>A</sub> = 40°C to +85°C)**

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V <sub>IH</sub>	Input High Voltage	2.0		V <sub>CC</sub> + 0.3	V	LVC MOS
V <sub>IL</sub>	Input Low Voltage	-0.3		0.8	V	LVC MOS
V <sub>OH</sub>	Output High Voltage	2.4			V	I <sub>OH</sub> = -24 mA <sup>a</sup>
V <sub>OL</sub>	Output Low Voltage			0.55 0.30	V V	I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 12 mA
Z <sub>OUT</sub>	Output Impedance		17		Ω	
I <sub>IN</sub>	Input Current <sup>b</sup>			±300	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
I <sub>CCQ</sub>	Maximum Quiescent Supply Current <sup>c</sup>			2.0	mA	All V <sub>CC</sub> Pins

- a. The MPC9447 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V<sub>TT</sub>. Alternatively, the device drives up to two 50Ω series terminated transmission lines (for V<sub>CC</sub>=3.3V).
- b. Inputs have pull-down or pull-up resistors affecting the input current.
- c. I<sub>CCQ</sub> is the DC current consumption of the device with all outputs open and the input in its default state or open.

**Table 6. AC Characteristics (V<sub>CC</sub> = 3.3V ± 5%, T<sub>A</sub> = -40°C to +85°C)<sup>a</sup>**

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f <sub>ref</sub>	Input Frequency	0		350	MHz	
f <sub>max</sub>	Output Frequency	0		350	MHz	
f <sub>P,REF</sub>	Reference Input Pulse Width	1.4			ns	
t <sub>r</sub> , t <sub>f</sub>	CCLK0, CCLK1 Input Rise/Fall Time			1.0 <sup>b</sup>	ns	0.8 to 2.0V
t <sub>PLH/HL</sub>	Propagation Delay CCLK0 or CCLK1 to any Q	1.3		3.3	ns	
t <sub>PLZ, HZ</sub>	Output Disable Time			11	ns	
t <sub>PZL, ZH</sub>	Output Enable Time			11	ns	
t <sub>S</sub>	Setup Time CCLK0 or CCLK1 to CLK_STOP <sup>c</sup>	0.0			ns	
t <sub>H</sub>	Hold Time CCLK0 or CCLK1 to CLK_STOP <sup>c</sup>	1.0			ns	
t <sub>sk(O)</sub>	Output-to-Output Skew			150	ps	
t <sub>sk(PP)</sub>	Device-to-Device Skew			2.0	ns	
t <sub>SK(P)</sub> DC <sub>Q</sub>	Output Pulse Skew <sup>d</sup> Output Duty Cycle	f <sub>Q</sub> < 170 MHz	45 50	300 55	ps %	DC <sub>REF</sub> = 50%
t <sub>r</sub> , t <sub>f</sub>	Output Rise/Fall Time	0.1		1.0	ns	0.55 to 2.4V
t <sub>JIT(CC)</sub>	Cycle-to-cycle jitter RMS (1 σ)		TBD		ps	

- a. AC characteristics apply for parallel output termination of 50Ω to V<sub>TT</sub>.
- b. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
- c. Setup and hold times are referenced to the falling edge of the selected clock signal input.
- d. Output pulse skew is the absolute difference of the propagation delay times: | t<sub>PLH</sub> - t<sub>PHL</sub> |.

**Table 7. DC Characteristics** ( $V_{CC} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ )

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
$V_{IH}$	Input High Voltage	1.7		$V_{CC} + 0.3$	V	LVC MOS
$V_{IL}$	Input Low Voltage	-0.3		0.7	V	LVC MOS
$V_{OH}$	Output High Voltage	1.8			V	$I_{OH} = -15 \text{ mA}^a$
$V_{OL}$	Output Low Voltage			0.6	V	$I_{OL} = 15 \text{ mA}$
$Z_{OUT}$	Output Impedance		19		$\Omega$	
$I_{IN}$	Input Current <sup>b</sup>			$\pm 300$	$\mu A$	$V_{IN} = V_{CC}$ or GND
$I_{CCQ}$	Maximum Quiescent Supply Current <sup>c</sup>			2.0	mA	All $V_{CC}$ Pins

- a. The MPC9447 is capable of driving 50 $\Omega$  transmission lines on the incident edge. Each output drives one 50 $\Omega$  parallel terminated transmission line to a termination voltage of  $V_{TT}$ . Alternatively, the device drives one 50 $\Omega$  series terminated transmission lines per output ( $V_{CC}=2.5V$ ).
- b. Inputs have pull-down or pull-up resistors affecting the input current.
- c.  $I_{CCQ}$  is the DC current consumption of the device with all outputs open and the input in its default state or open.

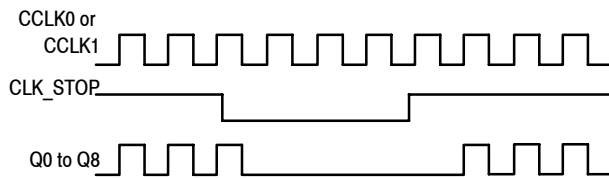
**Table 8. AC Characteristics** ( $V_{CC} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ )<sup>a</sup>

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
$f_{ref}$	Input Frequency	0		350	MHz	
$f_{max}$	Output frequency	0		350	MHz	
$t_{p,REF}$	Reference Input Pulse Width	1.4			ns	
$t_r, t_f$	CCLK0, CCLK1 Input Rise/Fall Time			1.0 <sup>b</sup>	ns	0.7 to 1.7V
$t_{PLH/HL}$	Propagation Delay CCLK0 or CCLK1 to any Q	1.7		4.4	ns	
$t_{PLZ, HZ}$	Output Disable Time			11	ns	
$t_{PZL, ZH}$	Output Enable Time			11	ns	
$t_s$	Setup Time CCLK0 or CCLK1 to CLK_STOP <sup>c</sup>	0.0			ns	
$t_h$	Hold Time CCLK0 or CCLK1 to CLK_STOP <sup>c</sup>	1.0			ns	
$t_{sk(O)}$	Output-to-Output Skew			150	ps	
$t_{sk(PP)}$	Device-to-Device Skew			2.7	ns	
$t_{sk(P)}$	Output Pulse Skew <sup>d</sup>			200	ps	
$DC_Q$	Output Duty Cycle $f_Q < 350 \text{ MHz}$	45	50	55	%	$DC_{REF} = 50\%$
$t_r, t_f$	Output Rise/Fall Time	0.1		1.0	ns	0.6 to 1.8V
$t_{JIT(CC)}$	Cycle-to-cycle jitter RMS (1 $\sigma$ )		TBD		ps	

- a. AC characteristics apply for parallel output termination of 50 $\Omega$  to  $V_{TT}$ .
- b. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
- c. Setup and hold times are referenced to the falling edge of the selected clock signal input.
- d. Output pulse skew is the absolute difference of the propagation delay times:  $|t_{PLH} - t_{PHL}|$ .

## APPLICATION INFORMATION

Figure 3. Output Clock Stop (CLK\_STOP) Timing Diagram



## Driving Transmission Lines

The MPC9447 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user, the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of  $17\Omega$  ( $V_{CC}=3.3V$ ), the outputs can drive either parallel or series terminated transmission lines. For more information on transmission lines, the reader is referred to Motorola application note AN1091. In most high performance clock networks, point-to-point distribution of signals is the method of choice. In a point-to-point scheme, either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a  $50\Omega$  resistance to  $V_{CC}+2$ .

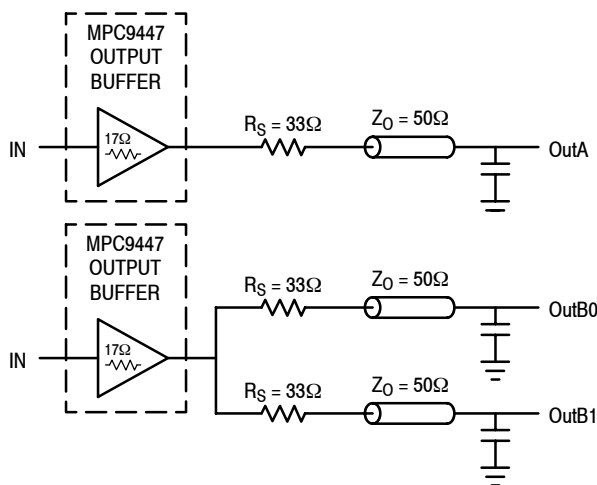


Figure 4. Single versus Dual Transmission Lines

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9447 clock driver. For the series terminated case, however, there is no DC current draw; thus, the outputs can drive multiple series terminated lines. Figure 4 “Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme, the fanout of the MPC9447 clock driver is effectively doubled due to its capability to drive multiple lines at  $V_{CC}=3.3V$ .

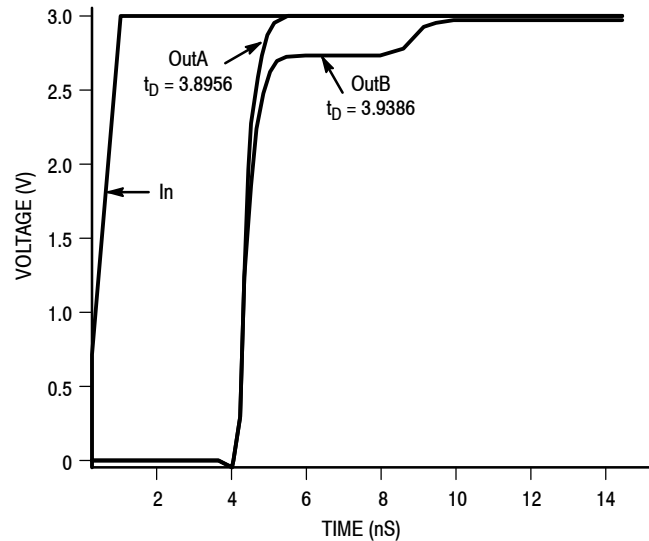


Figure 5. Single versus Dual Line Termination Waveforms

The waveform plots in Figure 5 “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases, the drive capability of the MPC9447 output buffer is more than sufficient to drive  $50\Omega$  transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9447. The output waveform in Figure 5 “Single versus Dual Line Termination Waveforms” shows a step in the waveform; this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the  $33\Omega$  series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$\begin{aligned}
 V_L &= V_S (Z_0 \div (R_S + R_0 + Z_0)) \\
 Z_0 &= 50\Omega \parallel 50\Omega \\
 R_S &= 33\Omega \parallel 33\Omega \\
 R_0 &= 17\Omega \\
 V_L &= 3.0 (25 \div (16.5 + 17 + 25)) \\
 &= 1.28V
 \end{aligned}$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.5V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

Since this step is well above the threshold region it will not cause any false clock triggering; however, designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines, the situation in Figure 6 “Optimized Dual Line Termination” should be used. In this case, the series terminating resistors

are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

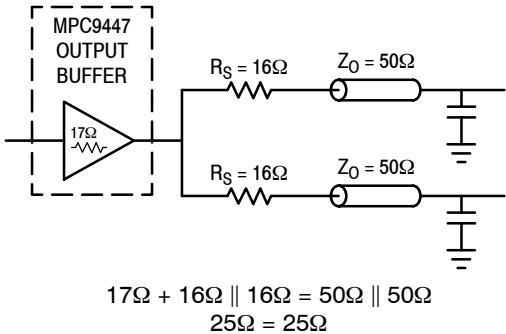


Figure 6. Optimized Dual Line Termination

The Following Figures Illustrate the Measurement Reference for the MPC9447 Clock Driver Circuit

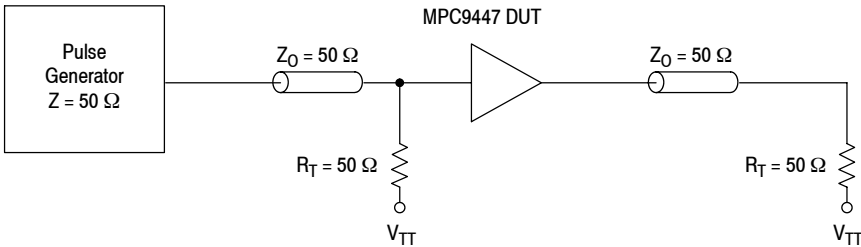


Figure 7. CCLK MPC9447 AC Test Reference for V<sub>cc</sub> = 3.3V and V<sub>cc</sub> = 2.5V

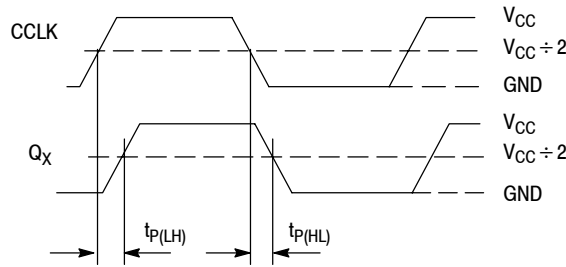
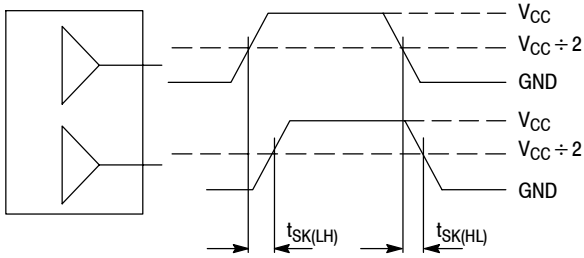


Figure 8. Propagation Delay ( $t_{PD}$ ) Test Reference



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 9. Output-to-Output Skew  $t_{SK(LH, HL)}$

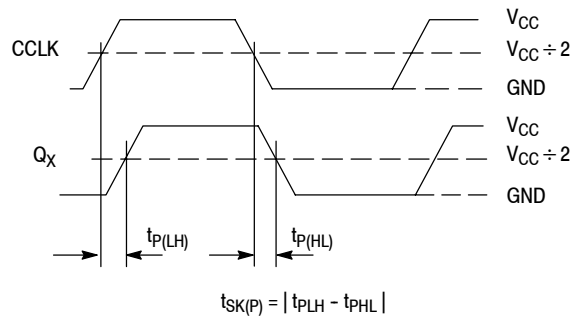
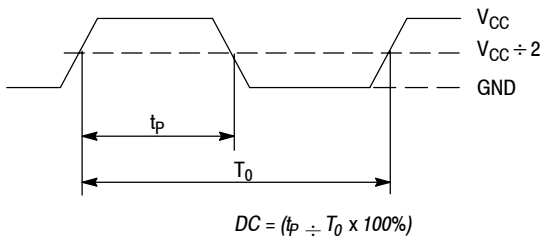


Figure 10. Output Pulse Skew ( $t_{SK(P)}$ ) Test Reference



The time from the output controlled edge to the non-controlled edge, divided by the time between output controlled edges, expressed as a percentage

Figure 11. Output Duty Cycle (DC)

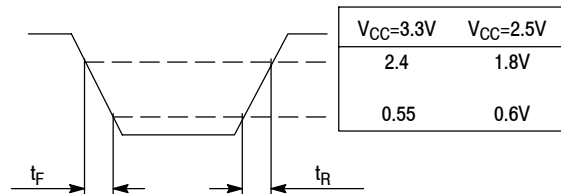
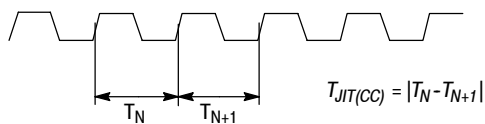


Figure 12. Output Transition Time Test Reference



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 13. Cycle-to-Cycle Jitter

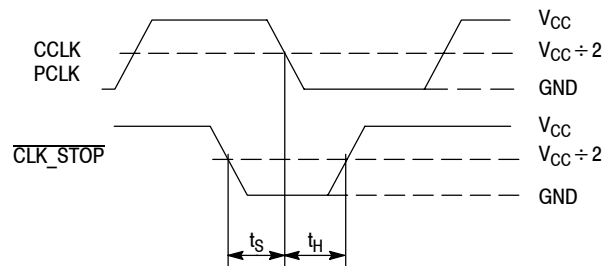
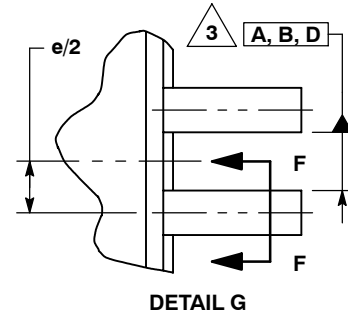
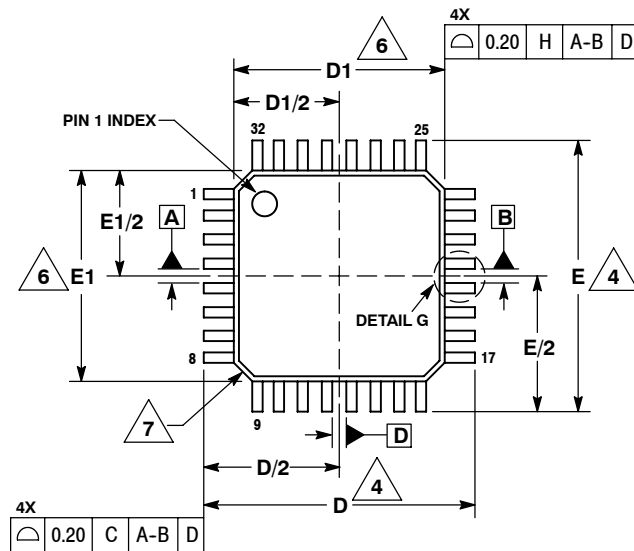


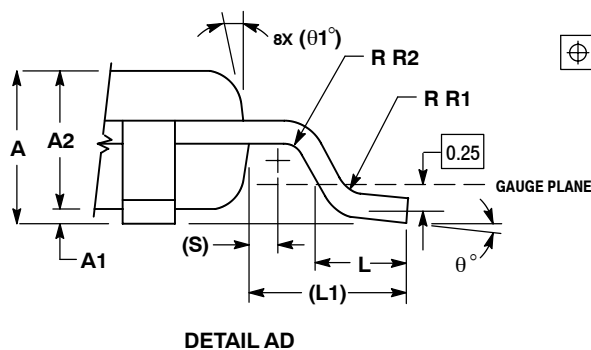
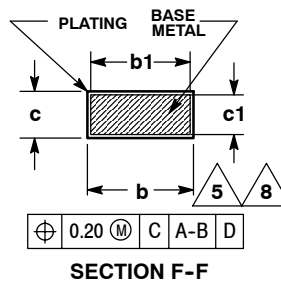
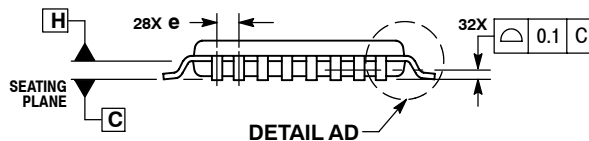
Figure 14. Setup and Hold Time ( $t_S, t_H$ ) Test Reference

**OUTLINE DIMENSIONS**

**FA SUFFIX**  
**LQFP PACKAGE**  
**CASE 873A-03**  
**ISSUE B**



- NOTES:**
1. DIMENSIONS ARE IN MILLIMETERS.
  2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
  3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
  4. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE C.
  5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08-mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07-mm.
  6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25-mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
  7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
  8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1-mm AND 0.25-mm FROM THE LEAD TIP.



DIM	MILLIMETERS	
	MIN	MAX
A	1.40	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.30	0.45
b1	0.30	0.40
c	0.09	0.20
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
e	0.80 BSC	
E	9.00 BSC	
E1	7.00 BSC	
L	0.50	0.70
L1	1.00	REF
θ	0°	7°
θ1	12°	REF
R1	0.08	0.20
R2	0.08	---
S	0.20 REF	



## NOTES

# NOTES

## NOTES

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**MPC9447/D**