

Low Voltage 1:18 Clock Distribution Chip

The MPC9109 is a 1:18 low voltage clock distribution chip with 2.5 V or 3.3 V LVCMOS output capabilities. The device features the capability to select either a differential LVPECL or an LVCMOS compatible input. The 18 outputs are 2.5 V or 3.3 V LVCMOS compatible and feature the drive strength to drive 50 Ω series or parallel terminated transmission lines. With output-to-output skews of 200 ps, the MPC9109 is ideal as a clock distribution chip for the most demanding of synchronous systems. The 2.5 V outputs also make the device ideal for supplying clocks for a high performance Pentium II™ microprocessor based design. For a higher performance version of the 9109 refer to the MPC940L data sheet.

Features

- LVPECL or LVCMOS clock input
- 2.5 V LVCMOS outputs for Pentium II microprocessor support
- 200 ps maximum output-to-output skew @ 3.3 V output
- Maximum output frequency of 250 MHz @ 3.3 V core
- 32-lead QFP packaging
- Dual or single supply device:
 - Dual V_{CC} supply voltage, 3.3 V core and 2.5 V output
 - Single 3.3 V V_{CC} supply voltage for 3.3 V outputs
 - Single 2.5 V V_{CC} supply voltage for 2.5 V I/O

Functional Description

With a low output impedance ($\approx 20 \Omega$), in both the HIGH and LOW logic states, the output buffers of the MPC9109 are ideal for driving series terminated transmission lines. With a 20 Ω output impedance the 9109 has the capability of driving two series terminated lines from each output. This gives the device an effective fanout of 1:36. If a lower output impedance is desired please see the MPC942 data sheet. If better performance is desired please see the MPC940L data sheet.

The differential LVPECL inputs of the MPC9109 allow the device to interface directly with a LVPECL fanout buffer like the MC100EP111 to build very wide clock fanout trees or to couple to a high frequency clock source. The LVCMOS input provides a more standard interface for applications requiring only a single clock distribution chip at relatively low frequencies. In addition, the two clock sources can be used to provide for a test clock interface as well as the primary system clock. A logic HIGH on the LVCMOS_CLK_Sel pin will select the LVCMOS level clock input. All inputs of the MPC9109 have internal pullup/pulldown resistor so they can be left open if unused.

The MPC9109 is a single or dual supply device. The device power supply offers a high degree of flexibility. The device can operate with a 3.3 V core and 3.3 V output, a 3.3 V core and 2.5 V outputs as well as a 2.5 V core and 2.5 V outputs. The 32-lead QFP package was chosen to optimize performance, board space and cost of the device. The 32-lead TQFP has a 7x7mm body size with a conservative 0.8 mm pin spacing.

MPC9109

**LOW VOLTAGE
1:18 CLOCK
DISTRIBUTION CHIP**



**FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-04**



**AC SUFFIX
32-LEAD LQFP PACKAGE
Pb-FREE PACKAGE
CASE 873A-04**

Pentium II is a trademark of Intel Corporation.



Figure 1. Logic Diagram

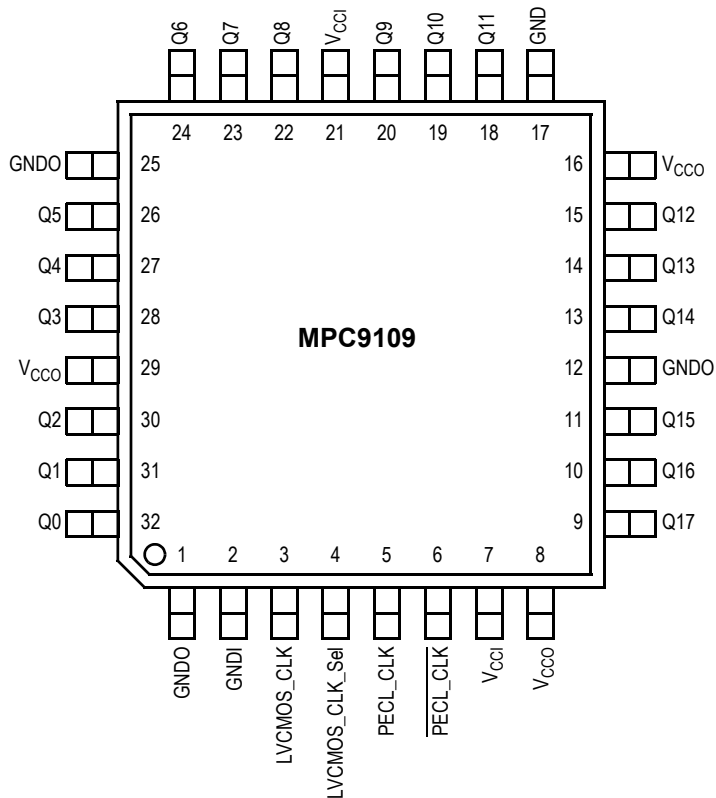


Figure 2. Pinout: 32-Lead TQFP (Top View)

Table 1. Function Table

LVCOS_CLK_Sel	Input
0	PECL_CLK
1	LVCOS_CLK

Table 2. Power Supply Voltages

Supply Pin	Voltage Level
VCC1	2.5 V or 3.3 V \pm 5%
VCC0	2.5 V or 3.3 V \pm 5%

Table 3. Absolute Maximum Ratings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage	−0.3	3.6	V
V _I	Input Voltage	−0.3	V _{CC} + 0.3	V
I _{IN}	Input Current		±20	mA
T _{Stor}	Storage Temperature Range	−40	125	°C

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 4. DC Characteristics (T_A = 0° to 70°C, V_{CCI} = 3.3 V ± 5%; V_{CCO} = 3.3 V ± 5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V _{IH}	Input HIGH Voltage CMOS_CLK	2.4		V _{CCI}	V	
V _{IL}	Input LOW Voltage CMOS_CLK			0.8	V	
V _{PP}	Peak-to-Peak Input Voltage PECL_CLK	500		1000	mV	
V _{CMR}	Common Mode Range PECL_CLK	V _{CC} −1.4		V _{CC} −0.6	V	
V _{OH}	Output HIGH Voltage	2.4			V	I _{OH} = −20 mA
V _{OL}	Output LOW Voltage			0.5	V	I _{OH} = 20 mA
I _{IN}	Input Current			±200	μA	
C _{IN}	Input Capacitance		4.0		pF	
C _{pd}	Power Dissipation Capacitance		10		pF	Per output
Z _{OUT}	Output Impedance	18	23	28	Ω	
I _{CC}	Maximum Quiescent Supply Current		0.5		mA	

Table 5. AC Characteristics (T_A = 0° to 70°C, V_{CCI} = 3.3 V ± 5%; V_{CCO} = 3.3 V ± 5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
F _{max}	Maximum Input Frequency			250	MHz	
t _{PLH}	Propagation Delay PECL_CLK CMOS_CLK	1.8 1.6	2.8 2.5	3.8 3.3	ns	Note ⁽¹⁾
t _{sk(o)}	Output-to-Output Skew PECL_CLK CMOS_CLK			200 200	ps	Note ⁽¹⁾
t _{sk(pr)}	Part-to-Part Skew PECL_CLK CMOS_CLK			2.0 1.7	ns	Note ⁽¹⁾
d _t	Duty Cycle	45		55	%	Note ⁽¹⁾
t _r , t _f	Output Rise/Fall Time	0.1		1.3	ns	Note ⁽¹⁾

1. Guaranteed by statistical analysis, not 100% tested in production.

Table 6. Absolute Maximum Ratings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage	−0.3	3.6	V
V _I	Input Voltage	−0.3	V _{CC} + 0.3	V
I _{IN}	Input Current		±20	mA
T _{Stor}	Storage Temperature Range	−40	125	°C

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 7. DC Characteristics (T_A = 0° to 70°C, V_{CCI} = 3.3 V ± 5%; V_{CCO} = 2.5 V ± 5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V _{IH}	Input HIGH Voltage CMOS_CLK	2.4		V _{CCI}	V	
V _{IL}	Input LOW Voltage CMOS_CLK			0.8	V	
V _{PP}	Peak-to-Peak Input Voltage PECL_CLK	500		1000	mV	
V _{CMR}	Common Mode Range PECL_CLK	V _{CC} −1.4		V _{CC} −0.6	V	
V _{OH}	Output HIGH Voltage	1.8			V	I _{OH} = −20 mA
V _{OL}	Output LOW Voltage			0.5	V	I _{OH} = 20 mA
I _{IN}	Input Current			±200	μA	
C _{IN}	Input Capacitance		4.0		pF	
C _{pd}	Power Dissipation Capacitance		10		pF	Per output
Z _{OUT}	Output Impedance		23		Ω	
I _{CC}	Maximum Quiescent Supply Current		0.5		mA	

Table 8. AC Characteristics (T_A = 0° to 70°C, V_{CCI} = 3.3 V ± 5%; V_{CCO} = 2.5 V ± 5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
F _{max}	Maximum Input Frequency			250	MHz	
t _{PLH}	Propagation Delay PECL_CLK CMOS_CLK	1.8 1.6	2.8 2.5	3.9 3.4	ns	Note ⁽¹⁾
t _{sk(o)}	Output-to-Output Skew PECL_CLK CMOS_CLK			250 250	ps	Note ⁽¹⁾
t _{sk(pr)}	Part-to-Part Skew PECL_CLK CMOS_CLK			2.1 1.8	ns	Note ⁽¹⁾
d _t	Duty Cycle	45		55	%	Note ⁽¹⁾
t _r , t _f	Output Rise/Fall Time	0.1		1.3	ns	Note ⁽¹⁾

1. Guaranteed by statistical analysis, not 100% tested in production.

Table 9. Absolute Maximum Ratings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage	−0.3	3.6	V
V _I	Input Voltage	−0.3	V _{CC} + 0.3	V
I _{IN}	Input Current		±20	mA
T _{Stor}	Storage Temperature Range	−40	125	°C

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 10. DC Characteristics (T_A = 0° to 70°C, V_{CCI} = 2.5 V ± 5%; V_{CCO} = 2.5 V ± 5%)

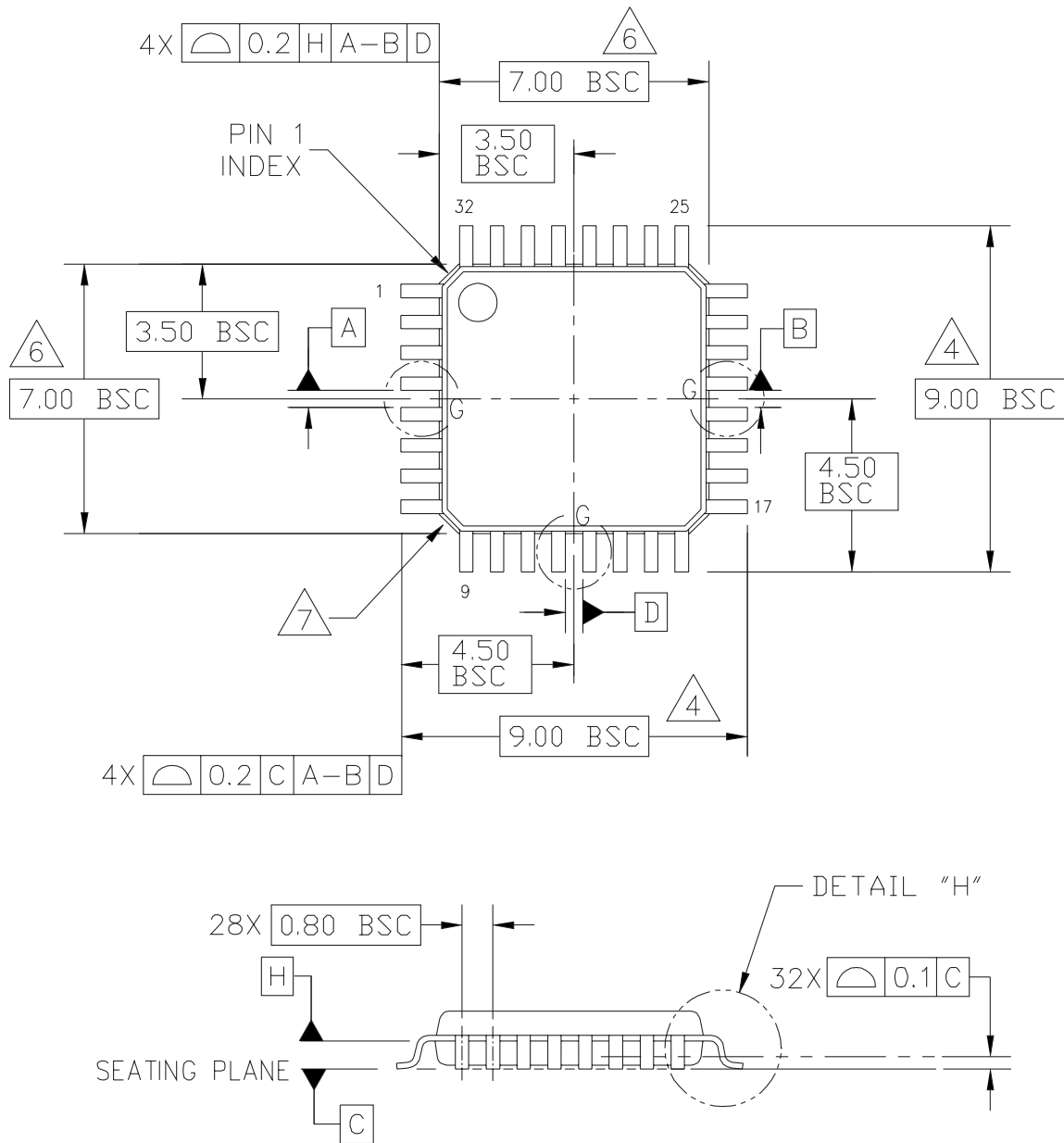
Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V _{IH}	Input HIGH Voltage CMOS_CLK	2.0		V _{CCI}	V	
V _{IL}	Input LOW Voltage CMOS_CLK			0.8	V	
V _{PP}	Peak-to-Peak Input Voltage PECL_CLK	500		1000	mV	
V _{CMR}	Common Mode Range PECL_CLK	V _{CC} −1.0		V _{CC} −0.6	V	
V _{OH}	Output HIGH Voltage	1.8			V	I _{OH} = −12 mA
V _{OL}	Output LOW Voltage			0.5	V	I _{OH} = 12 mA
I _{IN}	Input Current			±200	μA	
C _{IN}	Input Capacitance		4.0		pF	
C _{pd}	Power Dissipation Capacitance		10		pF	Per output
Z _{OUT}	Output Impedance	18	23	28	Ω	
I _{CC}	Maximum Quiescent Supply Current		0.5		mA	

Table 11. AC Characteristics (T_A = 0° to 70°C, V_{CCI} = 2.5 V ± 5%; V_{CCO} = 2.5 V ± 5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
F _{max}	Maximum Input Frequency			200	MHz	
t _{PLH}	Propagation Delay PECL_CLK CMOS_CLK	2.2 2.0	2.8 2.5	4.9 4.2	ns	Note ⁽¹⁾
t _{sk(o)}	Output-to-Output Skew PECL_CLK CMOS_CLK			250 250	ps	Note ⁽¹⁾
t _{sk(pr)}	Part-to-Part Skew PECL_CLK CMOS_CLK			2.7 2.2	ns	Note ⁽¹⁾
d _t	Duty Cycle	45		55	%	Note ⁽¹⁾
t _r , t _f	Output Rise/Fall Time	0.1		1.3	ns	Note ⁽¹⁾

1. Guaranteed by statistical analysis, not 100% tested in production.

PACKAGE DIMENSIONS

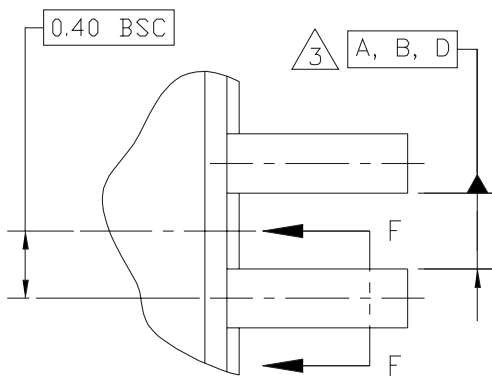


© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4)	DOCUMENT NO: 98ASH70029A	REV: C
	CASE NUMBER: 873A-04	01 APR 2005
	STANDARD: JEDEC MS-026 BBA	

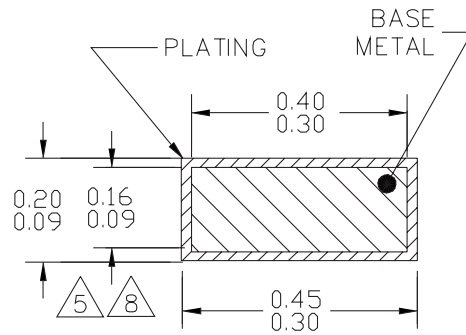
PAGE 1 OF 3

CASE 873A-04 ISSUE C 32-LEAD LQFP PACKAGE

PACKAGE DIMENSIONS

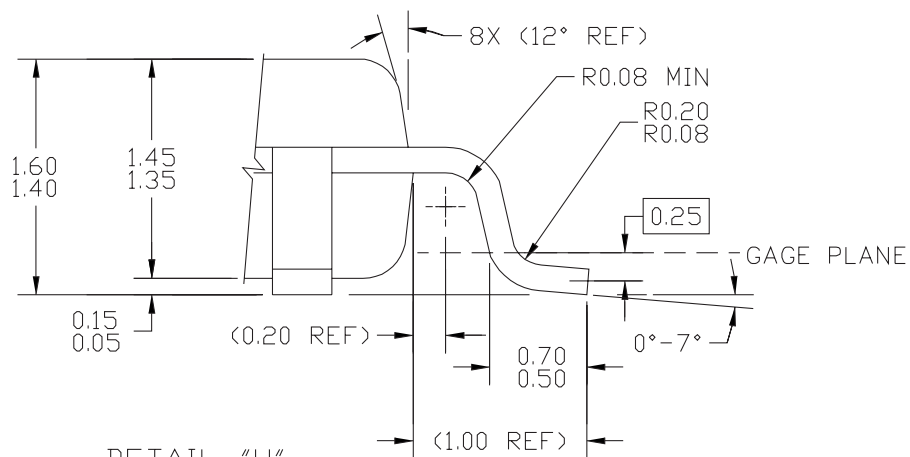


DETAIL G



⊕ 0.2 Ⓜ C A-B D

SECTION F-F
ROTATED 90°CW
32 PLACES



DETAIL "H"

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4)	DOCUMENT NO: 98ASH70029A		REV: C
	CASE NUMBER: 873A-04		01 APR 2005
	STANDARD: JEDEC MS-026 BBA		

PAGE 2 OF 3

**CASE 873A-04
ISSUE C
32-LEAD LQFP PACKAGE**

MPC9109

PACKAGE DIMENSIONS

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5-1994.
3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE DATUM C.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07 MM.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4)	DOCUMENT NO: 98ASH70029A		REV: C
	CASE NUMBER: 873A-04		01 APR 2005
	STANDARD: JEDEC MS-026 BBA		

PAGE 3 OF 3

**CASE 873A-04
ISSUE C
32-LEAD LQFP PACKAGE**

How to Reach Us:

Home Page:

www.freescale.com

E-mail:

support@freescale.com

USA/Europe or Locations Not Listed:

Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2005. All rights reserved.

