Document Number: MPC17511A
Rev. 5.0, 9/2008

1.0 A 6.8 V H-Bridge Motor Driver IC

The 17511A is a monolithic H-Bridge designed to be used in portable electronic applications to control small DC motors or bipolar step motors. End applications include head positioners (CDROM or disk drive), camera focus motors, and camera shutter solenoids.

The 17511A can operate efficiently with supply voltages as low as 2.0V to as high as 6.8V. Its low $R_{DS(ON)}$ H-Bridge output MOSFETs (0.46 Ω typical) can provide continuos motor drive currents of 1.0A and handle peak currents up to 3.0A. It is easily interfaced to low-cost MCUs via parallel 3.0V- or 5.0V- compatible logic. The device can be pulse width modulated (PWM-ed) at up to 200 kHz.

This device contains an integrated charge pump and level shifter (for gate drive voltages), integrated shoot-through current protection (cross-conduction suppression logic and timing), and undervoltage detection and shutdown circuitry.

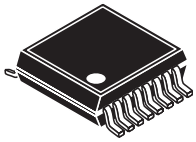
The 17511A has four operating modes: Forward, Reverse, Brake, and Tri-Stated (High Impedance).

Features

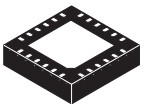
- 2.0V to 6.8V Continuous Operation
- Output Current 1.0 A(DC), 3.0A (Peak)
- MOSFETs < 600 mΩ $R_{DS(ON)}$ @ 25°C Guaranteed
- 3.0V/5.0V TTL-/CMOS-Compatible Inputs
- PWM Frequencies up to 200 kHz
- Undervoltage Shutdown
- Cross-Conduction Suppression
- Low Power Consumption
- Pb-Free Packaging Designated by Suffix Codes EV and EP

17511A

H-BRIDGE MOTOR DRIVER IC



EV SUFFIX (PB-FREE)
98ASA10614D
16-PIN VMFP



EP SUFFIX (PB-FREE)
98ARL10577D
24-PIN QFN

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MPC17511AEV	-20°C to 65°C	16 VMFP
MPC17511AEV/EL		
MPC17511AEP		24 QFN
MPC17511AEP/R2		

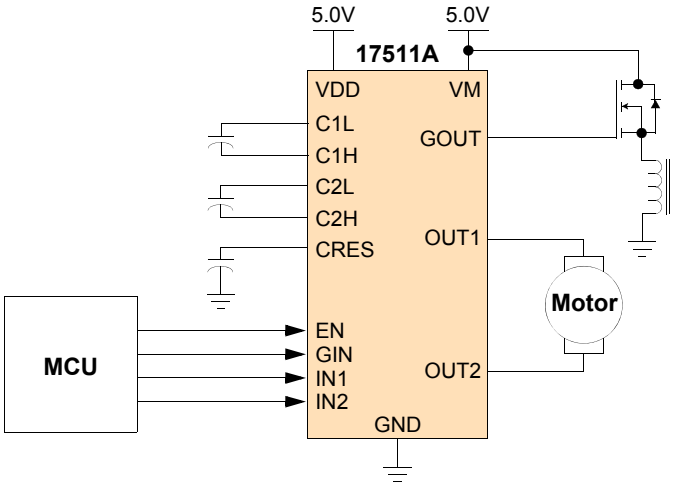


Figure 1. 17511A Simplified Application Diagram

INTERNAL BLOCK DIAGRAM

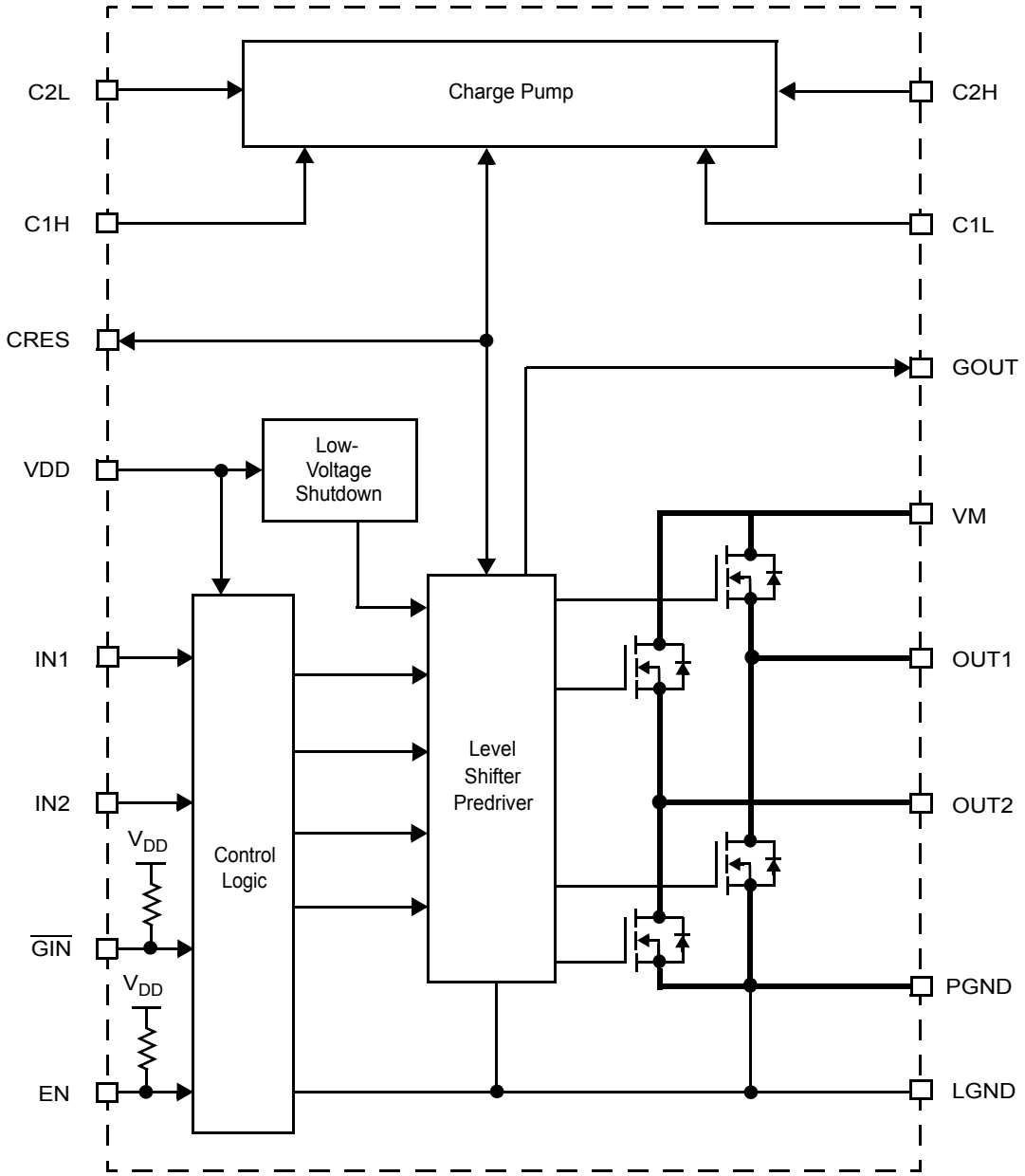


Figure 2. 17511A Simplified Internal Block Diagram

PIN CONNECTIONS

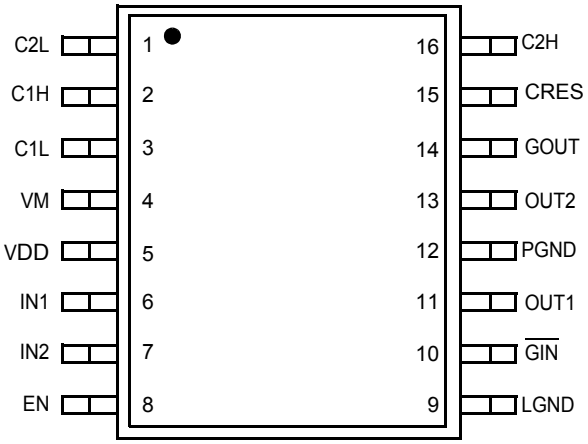


Figure 3. VMFP Pin Connections

Table 1. VMFP Pin Function Description

Pin Number	Pin Name	Formal Name	Definition
1	C2L	Charge Pump 2L	Charge pump bucket capacitor 2 (negative pole).
2	C1H	Charge Pump 1H	Charge pump bucket capacitor 1 (positive pole).
3	C1L	Charge Pump 1L	Charge pump bucket capacitor 1 (negative pole).
4	VM	Motor Drive Power Supply	Driver power supply voltage input pin.
5	VDD	Logic Supply	Control circuit power supply pin.
6	IN1	Input Control 1	Control signal input 1
7	IN2	Input Control 2	Control signal input 2.
8	EN	Enable Control	Enable control signal input pin.
9	LGND	Logic Ground	Logic ground pin.
10	GIN	Gate Driver Input	LOW = True control signal for GOUT pin.
11	OUT1	H-Bridge Output 1	Driver output 1 (right half of H-Bridge).
12	PGND	Power Ground	Driver ground pin.
13	OUT2	H-Bridge Output 2	Driver output 2 (left half of H-Bridge).
14	GOUT	Gate Driver Output	Output gate driver signal to external MOSFET switch.
15	CRES	Charge Pump Output Capacitor Connection	Charge pump reservoir capacitor pin.
16	C2H	Charge Pump 2H	Charge pump bucket capacitor 2 (positive pole).

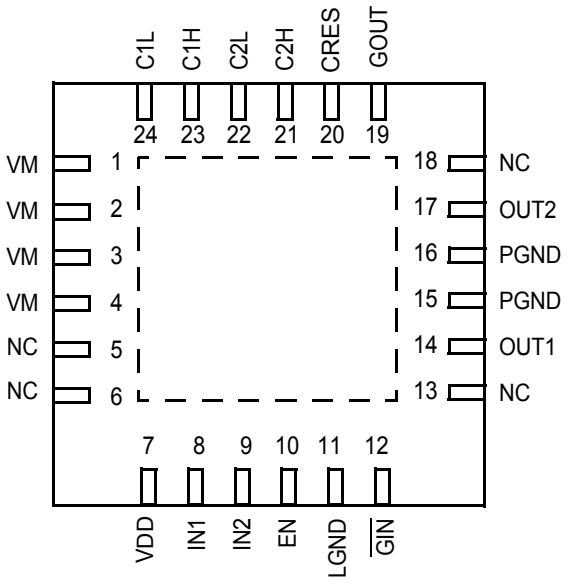


Figure 4. QFN Pin Connections

Table 2. QFN Pin Function Description

Pin Number	Pin Name	Formal Name	Definition
1, 2, 3, 4	VM	Motor Drive Power Supply	Driver power supply voltage input pin.
5, 6, 13, 18	NC	No Connect	This pin is not used.
7	VDD	Logic Supply	Control circuit power supply pin.
8	IN1	Logic Input Control 1	Control signal input 1.
9	IN2	Logic Input Control 2	Control signal input 2.
10	EN	Enable Control	Enable control signal input pin.
11	LGND	Logic Ground	Logic ground pin.
12	GIN	Gate Driver Input	LOW = True control signal for GOUT pin.
14	OUT1	Output 1	Driver output 1 (right half of H-Bridge).
15, 16	PGND	Power Ground	Driver ground pin.
17	OUT2	Output 2	Driver output 2 (left half of H-Bridge).
19	GOUT	Gate Driver Output	Output gate driver signal to external MOSFET switch.
20	CRES	Pre-Driver Power Supply	Pre-driver circuit power supply pin.
21	C2H	Charge Pump 2H	Charge pump bucket capacitor 2 (positive pole).
22	C2L	Charge Pump 2L	Charge pump bucket capacitor 2 (negative pole).
23	C1H	Charge Pump 1H	Charge pump bucket capacitor 1 (positive pole).
24	C1L	Charge Pump 1L	Charge pump bucket capacitor 1 (negative pole).

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 3. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding the ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
Motor Supply Voltage	V_M	-0.5 to 8.0	V
Charge Pump Output Voltage	V_{CRES}	-0.5 to 14.0	V
Logic Supply Voltage	V_{DD}	-0.5 to 7.0	V
Signal Input Voltage (EN, IN1, IN2, $\overline{GIN}$)	V_{IN}	-0.5 to V_{DD}+0.5	V
Driver Output Current Continuous Peak (1)	 I_O I_{OPK}	 1.0 3.0	A
ESD Voltage (2) Human Body Model Machine Model	 V_{ESD1} V_{ESD2}	 ±1800 ±100	V
Storage Temperature Range	T_{STG}	-65 to 150	°C
Operating Ambient Temperature	T_A	-20 to 65	°C
Operating Junction Temperature	T_J	-20 to 150	°C
Thermal Resistance (3) 24 Pin QFN 16 Pin VMFP	$R_{\theta JA}$	 50 150	°C/W
Power Dissipation (4) 24 Pin QFN 16 Pin VMFP	P_D	 2500 830	mW
Soldering Temperature (5)	T_{SOLDER}	260	°C
Peak Package Reflow Temperature During Reflow (6), (7)	T_{PPRT}	Note 7	°C

Notes

1. T_A = 25°C, 10 ms pulse width at 200 ms intervals.
2. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
3. QFN24: 45 x 30 x 1 [mm] glass EPOXY board mount. (See: recommended heat pattern) VMFP16: 37 x 50 x 1.6 [mm] glass EPOXY board mount. When the exposed pad is bonded, Rsj will not be performed.
4. Maximum at T_A = 25°C. When the exposed pad is bonded, Rsj will not be performed.
5. Soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
6. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
7. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL),
Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 4. Static Electrical Characteristics

Characteristics noted under conditions T_A = 25°C, $V_M = V_{DD}$ = 5.0V, GND = 0V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER					
Driver Circuit Power Supply Voltage	V_M	2.0	5.0	6.8	V
Logic Supply Voltage	V_{DD}	2.7	5.0	5.7	V
Capacitor for Charge Pump	C1, C2, C3	0.01	0.1	1.0	µF
Standby Power Supply Current					
Motor Supply Standby Current	I_{VMSTBY}	–	–	1.0	µA
Logic Supply Standby Current (8)	$I_{VDDSTBY}$	–	–	1.0	mA
Operating Power Supply Current					
Logic Supply Current (9)	I_{VDD}	–	–	3.0	mA
Charge Pump Circuit Supply Current	I_{CRES}	–	–	0.7	mA
Low V_{DD} Detection Voltage (10)	$V_{DD}DET$	1.5	2.0	2.5	V
Driver Output ON Resistance (11)	$R_{DS(ON)}$	–	0.46	0.60	Ω
GATE DRIVE					
Gate Drive Voltage (12)	V_{CRES}				V
No Current Load		12	13	13.5	
Gate Drive Ability (Internally Supplied)	$V_{CRESLOAD}$				V
I_{CRES} = -1.0 mA		10	11.2	–	
Gate Drive Output					V
I_{OUT} = -50 µA	$V_{GOUTHIGH}$	V_{CRES}-0.5	V_{CRES}-0.1	V_{CRES}	
I_{IN} = 50 µA	$V_{GOUTLOW}$	LGND	LGND+0.1	LGND+0.5	
CONTROL LOGIC					
Logic Input Voltage	V_{IN}	0	–	V_{DD}	V
Logic Input Function (2.7V < V_{DD} < 5.7V)					
High-Level Input Voltage	V_{IH}	V_{DD} x 0.7	–	–	V
Low-Level Input Voltage	V_{IL}	–	–	V_{DD} x 0.3	V
High-Level Input Current	I_{IH}	–	–	1.0	µA
Low-Level Input Current	I_{IL}	-1.0	–	–	µA
Pull-Up Resistance (EN, $\overline{GIN}$)	R_{PU}	50	100	200	kΩ

Notes

8. $I_{VDDSTBY}$ includes current to the predriver circuit.
9. I_{VDD} includes current to the predriver circuit.
10. Detection voltage is defined as when the output becomes high-impedance after V_{DD} drops below the detection threshold. When the gate voltage V_{CRES} is applied from an external source, V_{CRES} = 7.5V.
11. I_O = 1.0A source + sink.
12. Input logic signal not present.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 5. Dynamic Electrical Characteristics

Characteristics noted under conditions T_A = 25°C, $V_M = V_{DD}$ = 5.0V, GND = 0V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT (EN, IN1, IN2, $\overline{GIN}$)					
Pulse Input Frequency	f_{IN}	–	–	200	kHz
Input Pulse Rise Time (13)	t_R	–	–	1.0 (14)	µs
Input Pulse Fall Time (15)	t_F	–	–	1.0 (14)	µs
OUTPUT					
Propagation Delay Time					µs
Turn-ON Time	t_{PLH}	–	0.55	1.0	
Turn-OFF Time	t_{PHL}	–	0.55	1.0	
GOUT Propagation Delay Time					µs
Turn-ON Time	t_{SON}	–	0.15	0.5	
Turn-OFF Time	t_{SOFF}	–	0.15	0.5	
Charge Pump Circuit (16)	$t_{VCRESON}$				ms
Rise Time (17)		–	0.1	3.0	
Low-Voltage Detection Time	t_{VDDDET}	–	–	10	ms

Notes
13. Time is defined between 10% and 90%.
14. That is, the input waveform slope must be steeper than this.
15. Time is defined between 90% and 10%.
16. When C1 = C2 = C3 = 0.1 µF.
17. Time to charge C_{RES} to 11V after application of V_{DD}.

TIMING DIAGRAMS

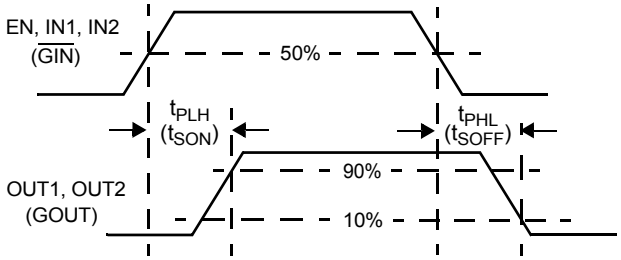


Figure 5. t_{PLH}, t_{PHL}, and t_{PZH} Timing

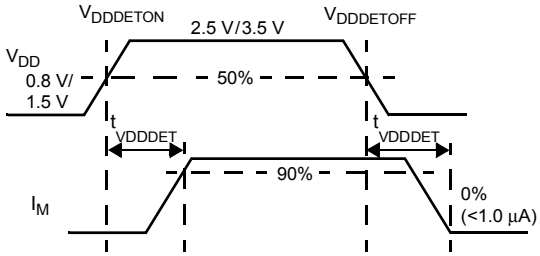


Figure 6. Low-Voltage Detection

Table 6. Truth Table

INPUT				OUTPUT		
EN	IN1	IN2	GIN	OUT1	OUT2	GOUT
H	H	H	X	L	L	X
H	H	L	X	H	L	X
H	L	H	X	L	H	X
H	L	L	X	Z	Z	X
L	X	X	X	L	L	L
H	X	X	H	X	X	L
H	X	X	L	X	X	H

H = High.
L = Low.
Z = High impedance.
X = Don’t care.

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 17511A is a monolithic H-Bridge power IC applicable to small DC motors used in portable electronics. The 17511A can operate efficiently with supply voltages as low as 2.0V to as high as 6.8V, and it can provide continuos motor drive currents of 1.0A while handling peak currents up to 3.0A. It is easily interfaced to low-cost MCUs via parallel 3.0 V- or 5.0V-compatible logic. The device can be pulse width modulated (PWM-ed) at up to 200 kHz. The 17511A has four operating modes: Forward, Reverse, Brake, and Tri-State (High Impedance).

Basic protection and operational features (direction, dynamic braking, PWM control of speed and torque, main power supply undervoltage detection and shutdown, logic power supply undervoltage detection and shutdown), in addition to the 1.0A rms output current capability, make the 17511A a very attractive, cost-effective solution for controlling a broad range of small DC motors. In addition, a pair of 17511A devices can be used to control bipolar step motors. The 17511A can also be used to excite transformer primary windings with a switched square wave to produce secondary winding AC currents.

As shown in Figure 2, 17511A Simplified Internal Block Diagram, page 2, the 17511A is a monolithic H-Bridge with built-in charge pump circuitry. For a DC motor to run, the input conditions need to be set as follows: ENable input logic HIGH, one INput logic LOW, and the other INput logic HIGH (to define output polarity). The 17511A can execute dynamic braking by setting both IN1 and IN2 logic HIGH, causing both low-side MOSFETs in the output H-Bridge to turn ON. Dynamic braking can also implemented by taking the ENable logic LOW. The output of the H-Bridge can be set to an open-circuit high-impedance (Z) condition by taking both IN1 and IN2 logic LOW. (refer to Table 6, Truth Table, page 8).

The 17511A outputs are capable of providing a continuous DC load current of up to 1.2A. An internal charge pump supports PWM frequencies to 200 kHz. The EN pin also controls the charge pump, turning it off when EN = LOW, thus allowing the 17511A to be placed in a power-conserving sleep mode.

FUNCTIONAL PIN DESCRIPTION

OUT1 AND OUT2

The OUT1 and OUT2 pins provide the connection to the internal power MOSFET H-Bridge of the IC. A typical load connected between these pins would be a small DC motor. These outputs will connect to either VM or PGND, depending on the states of the control inputs (refer to Table 6, Truth Table, page 8).

PGND AND LGND

The power and logic ground pins (PGND and LGND) should be connected together with a very low-impedance connection.

CRES

The CRES pin provides the connection for the external reservoir capacitor (output of the charge pump). Alternatively this pin can also be used as an input to supply gate-drive voltage from an external source via a series current-limiting resistor. The voltage at the CRES pin will be approximately three times the VDD voltage, as the internal charge pump utilizes a voltage tripler circuit. The VCRES voltage is used by the IC to supply gate drive for the internal power MOSFET H-Bridge.

VM

The VM pins carry the main supply voltage and current into the power sections of the IC. This supply then becomes controlled and/or modulated by the IC as it delivers the power to the load attached between OUT1 and OUT2. All VM pins must be connected together on the printed circuit board with as short as possible traces offering as low impedance as possible between pins.

VM has an undervoltage threshold. If the supply voltage drops below the undervoltage threshold, the output power stage switches to a tri-state condition. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input pins.

IN1, IN2, AND EN

The IN1, IN2, and EN pins are input control pins used to control the outputs. These pins are 5.0 V CMOS-compatible inputs with hysteresis. The IN1, IN2, and EN work together to control OUT1 and OUT2 (refer to Table 6, Truth Table).

$\overline{\text{GIN}}$

The $\overline{\text{GIN}}$ input controls the GOUT pin. When $\overline{\text{GIN}}$ is set logic LOW, GOUT supplies a level-shifted high-side gate drive signal to an external MOSFET. When $\overline{\text{GIN}}$ is set logic HIGH, GOUT is set to GND potential.

C1L AND C1H, C2L AND C2H

These two pairs of pins, the C1L and C1H and the C2L and C2H, connect to the external bucket capacitors required by the internal charge pump. The typical value for the bucket capacitors is 0.1 μF.

GOUT

The GOUT output pin provides a level-shifted, high-side gate drive signal to an external MOSFET with C_{ISS} up to 500pF.

VDD

The VDD pin carries the 5.0V supply voltage and current into the logic sections of the IC. VDD has an undervoltage threshold. If the supply voltage drops below the undervoltage threshold, the output power stage switches to a tri-state condition. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input pins.

TYPICAL APPLICATIONS

Figure 7 shows a typical application for the 17511A. When applying the gate voltage to the CRES pin from an external source, be sure to connect it via a resistor equal to, or greater than, $R_G = {}^{V}C_{RES}/0.02\Omega$.

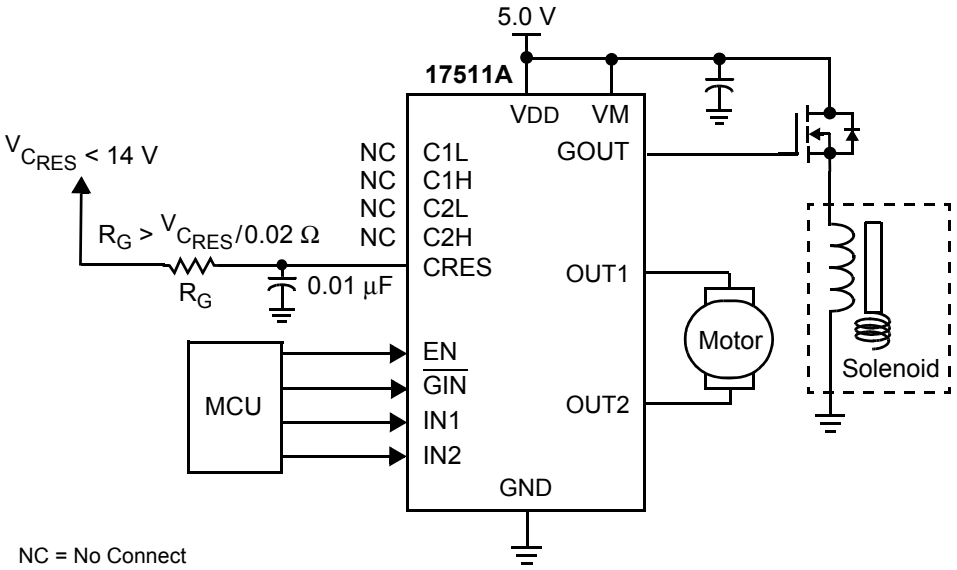


Figure 7. 17511A Typical Application Diagram

CEMF SNUBBING TECHNIQUES

Care must be taken to protect the IC from potentially damaging CEMF spikes induced when commutating currents in inductive loads. Typical practice is to provide snubbing of voltage transients via placing a capacitor or zener at the supply pin (VM) (see Figure 8).

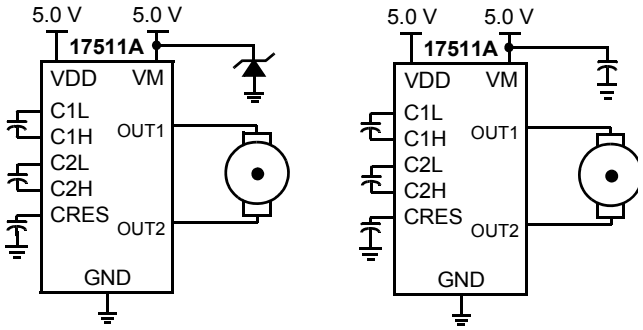


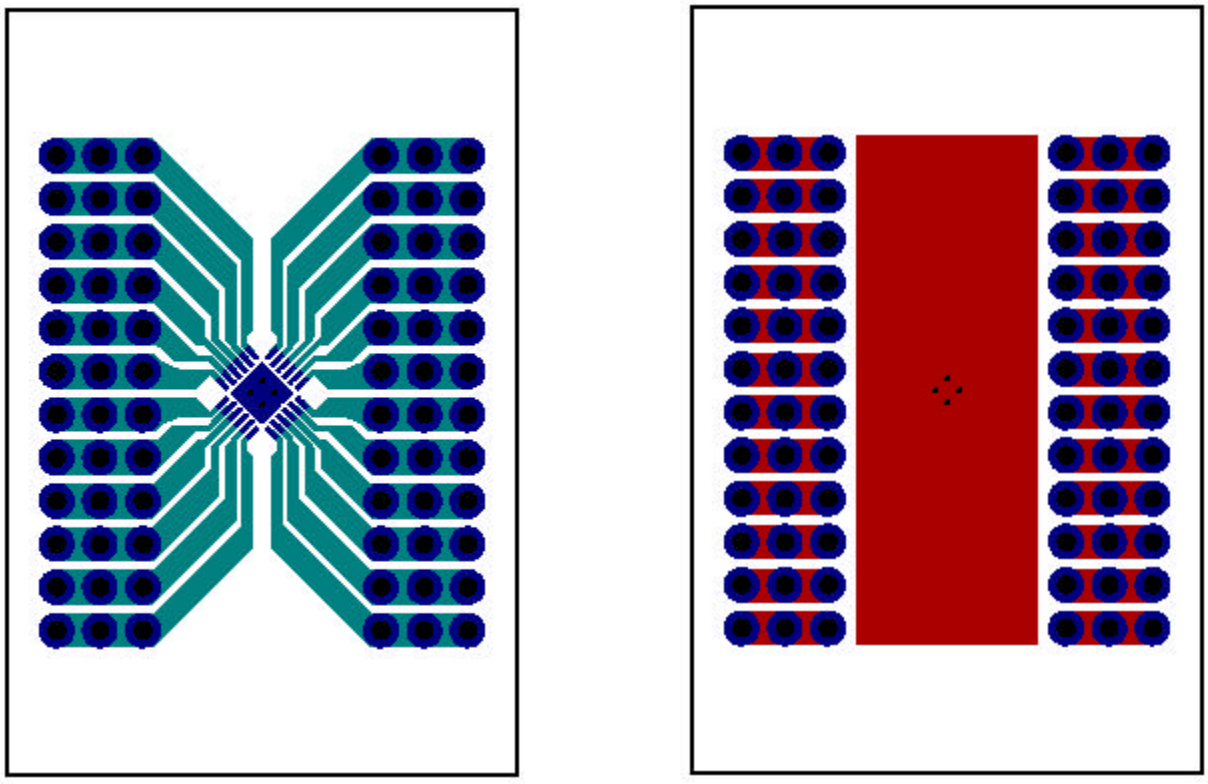
Figure 8. CEMF Snubbing Techniques

PACKAGING

SOLDERING

THERMAL PERFORMANCE

Below are the recommended heat patterns for the QFN24 Exposed Pad thermal package.

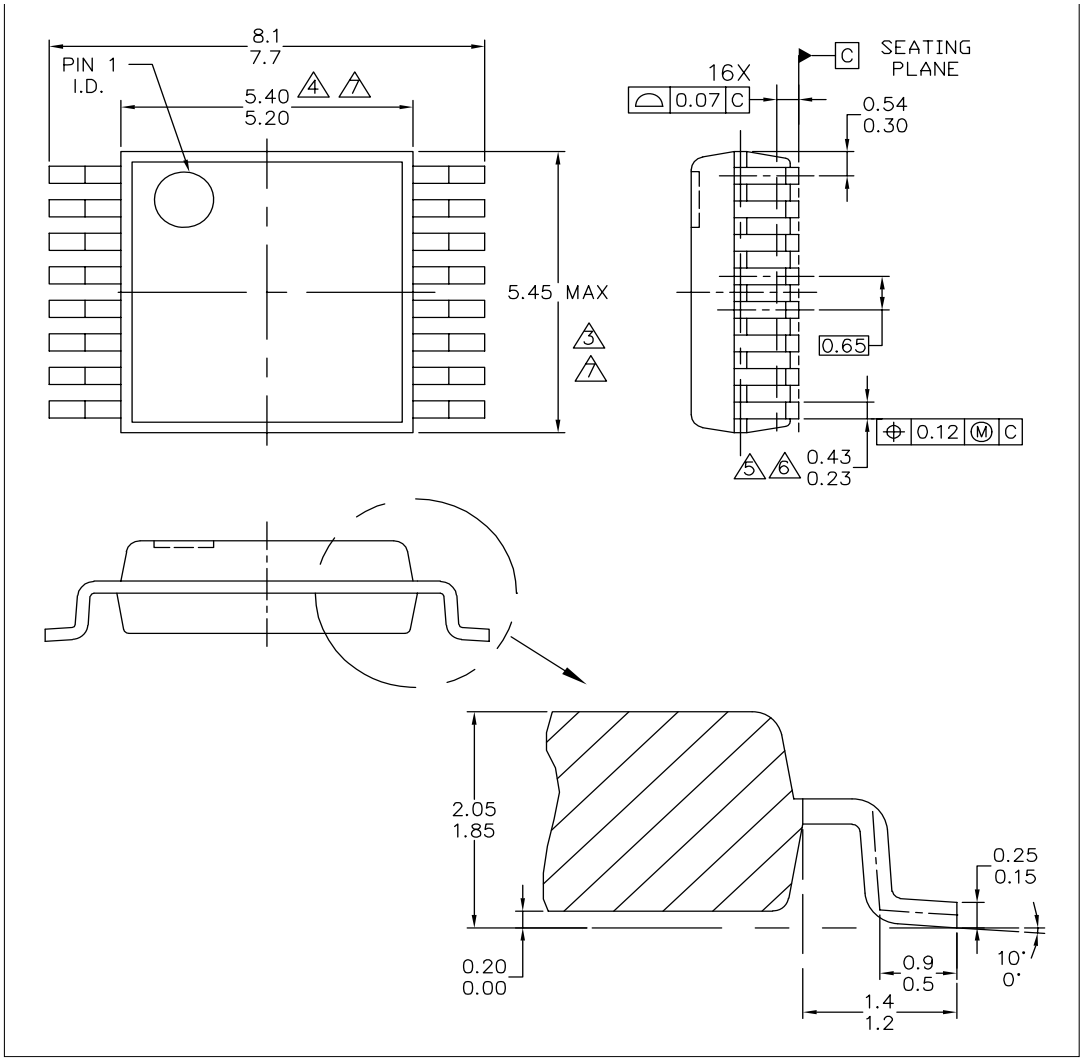


Obverse **Reverse**

Figure 9. Recomended Heat Patterns for QFN24 EP

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.



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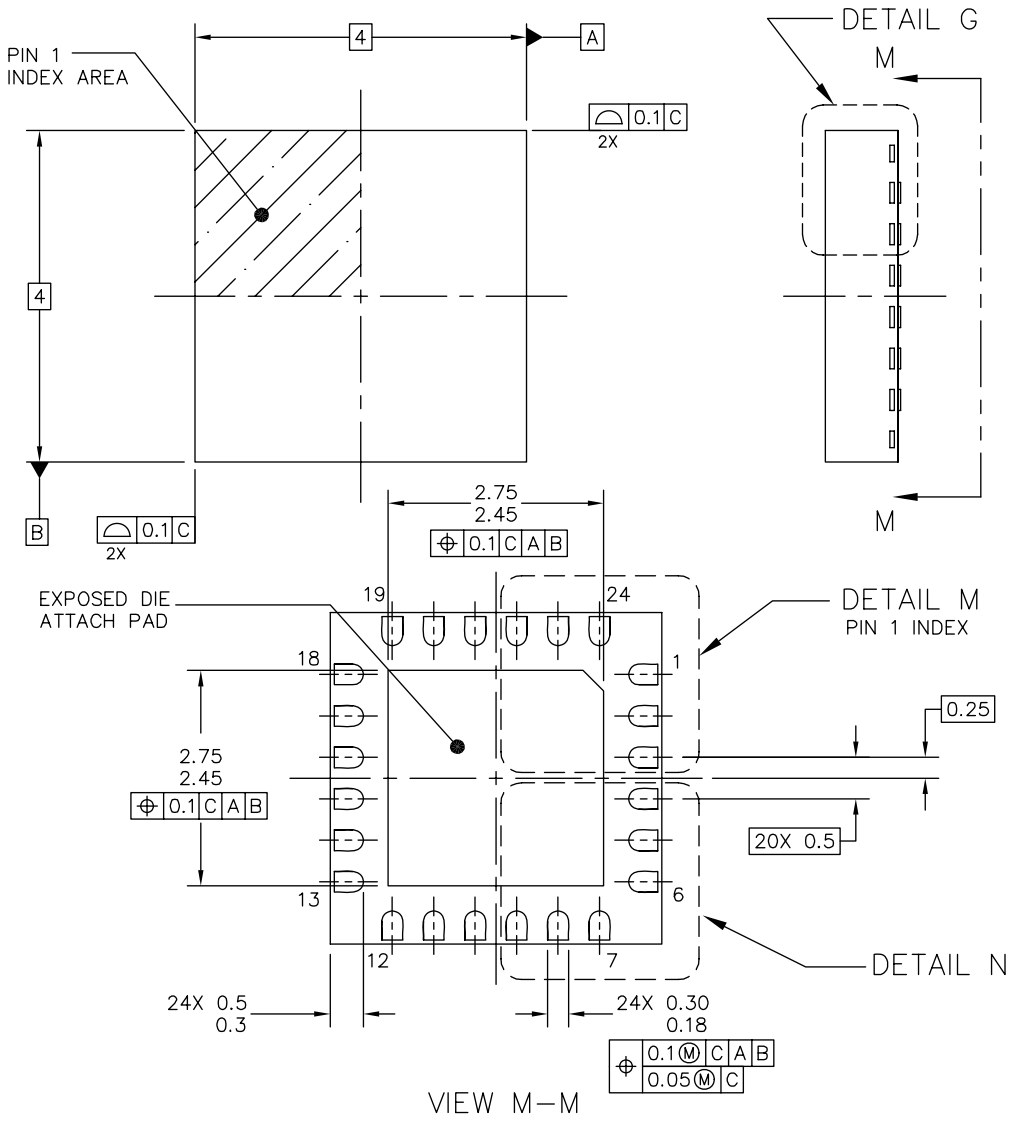
TITLE: 16LD VMFP, 5.30 X 5.45 PKG 0.65 PITCH CASE OUTLINE	DOCUMENT NO: 98ASA10614D	REV: B
	CASE NUMBER: 1563-02	07 NOV 2007
	STANDARD: NON-JEDEC	

EV (PB-FREE) SUFFIX
16-PIN VMFP
PLASTIC PACKAGE
98ASA10614D
ISSUE B

17511A

PACKAGE DIMENSIONS (CONTINUED)



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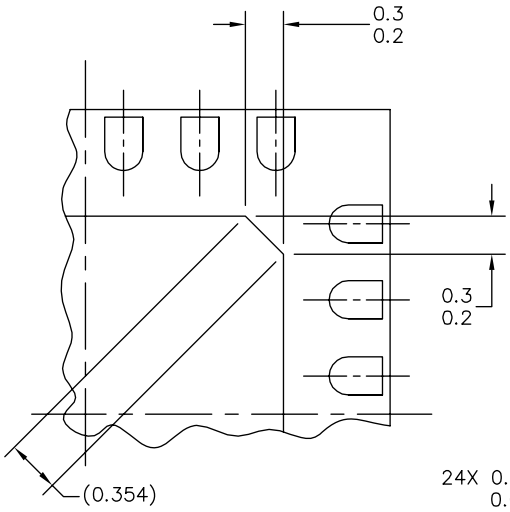
TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 24 TERMINAL, 0.5 PITCH (4 X 4 X 1)	DOCUMENT NO: 98ARL10577D	REV: B
	CASE NUMBER: 1508–02	28 DEC 2005
	STANDARD: NON–JEDEC	

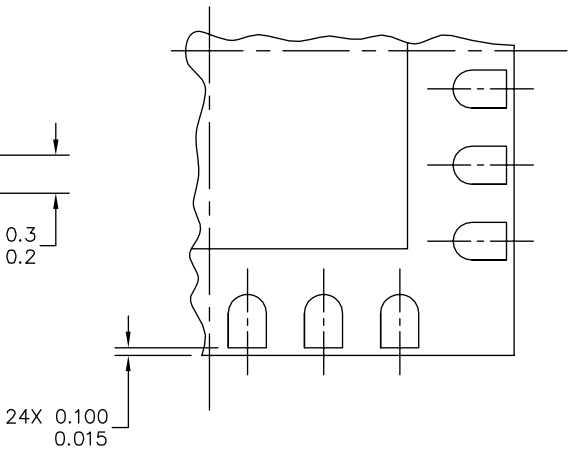
EP (PB-FREE) SUFFIX
24-PIN QFN
NON-LEADED PACKAGE
98ARL10577D
ISSUE B

17511A

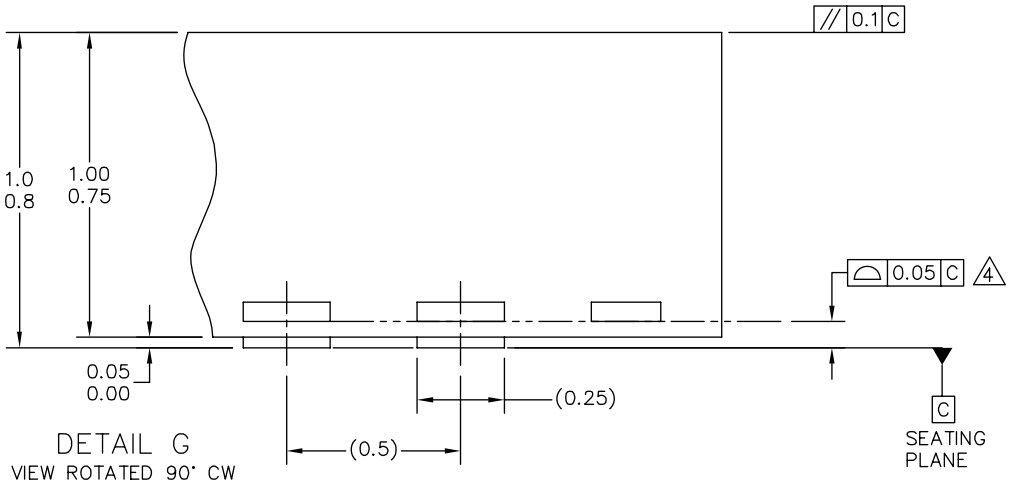
PACKAGE DIMENSIONS (CONTINUED)



DETAIL M
PIN 1 BACKSIDE IDENTIFIER



DETAIL N
CORNER CONFIGURATION



DETAIL G
VIEW ROTATED 90° CW

SEATING
PLANE

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TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 24 TERMINAL, 0.5 PITCH (4 X 4 X 1)	DOCUMENT NO: 98ARL10577D	REV: B
	CASE NUMBER: 1508–02	28 DEC 2005
	STANDARD: NON–JEDEC	

17511A

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
2.0	4/2007	• Implemented Revision History page • Converted to Freescale format • Added Peak Package Reflow Temperature During Reflow (solder reflow) parameter and Note with instructions from www.freescale.com to Maximum Ratings Table 3
3.0	11/2007	• Replaced 16 pin package drawing with 98ASA10614D, REV. B and replaced 24 pin package drawing with 98ARL10577D, REV. B.
4.0	2/2008	• Revised Siplified Application Diagram on page 1; Corrected typo - VM voltage from 15V to 5V.
5.0	8/2008	• Further Defined Thermal Resistance and Power Disapation in Table 2, Page 5 for both packages.

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