

2.5 V/3.3 V 1:5 Differential ECL/PECL/HSTL/LVDS Clock Driver

The MC100ES6014 is a low skew 1-to-5 differential driver, designed with clock distribution in mind, accepting two clock sources into an input multiplexer. The ECL/PECL input signals can be either differential or single-ended (if the V_{BB} output is used). HSTL and LVDS inputs can be used when the ES6014 is operating under PECL conditions.

The ES6014 specifically guarantees low output-to-output skew. Optimal design, layout, and processing minimize skew within a device and from device to device.

To ensure that the tight skew specification is realized, both sides of any differential output need to be terminated identically into $50\ \Omega$ even if only one output is being used. If an output pair is unused, both outputs may be left open (unterminated) without affecting skew.

The common enable (\overline{EN}) is synchronous, outputs are enabled/disabled in the LOW state. This avoids a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock; therefore, all associated specification limits are referenced to the negative edge of the clock input.

The MC100ES6014, as with most other ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the ES6014 to be used for high performance clock distribution in +3.3 V or +2.5 V systems. Single ended CLK input pin operation is limited to a $V_{CC} \geq 3.0\text{ V}$ in PECL mode, or $V_{EE} \leq -3.0\text{ V}$ in ECL mode. Designers can take advantage of the ES6014's performance to distribute low skew clocks across the backplane or the board.

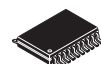
Features

- 25 ps Within Device Skew
- 400 ps Typical Propagation Delay
- Maximum Frequency > 2 GHz Typical
- The 100 Series Contains Temperature Compensation
- PECL and HSTL Mode: $V_{CC} = 2.375\text{ V}$ to 3.8 V with $V_{EE} = 0\text{ V}$
- ECL Mode: $V_{CC} = 0\text{ V}$ with $V_{EE} = -2.375\text{ V}$ to -3.8 V
- LVDS and HSTL Input Compatible
- Open Input Default State
- 20-Lead Pb-Free Package Available

MC100ES6014



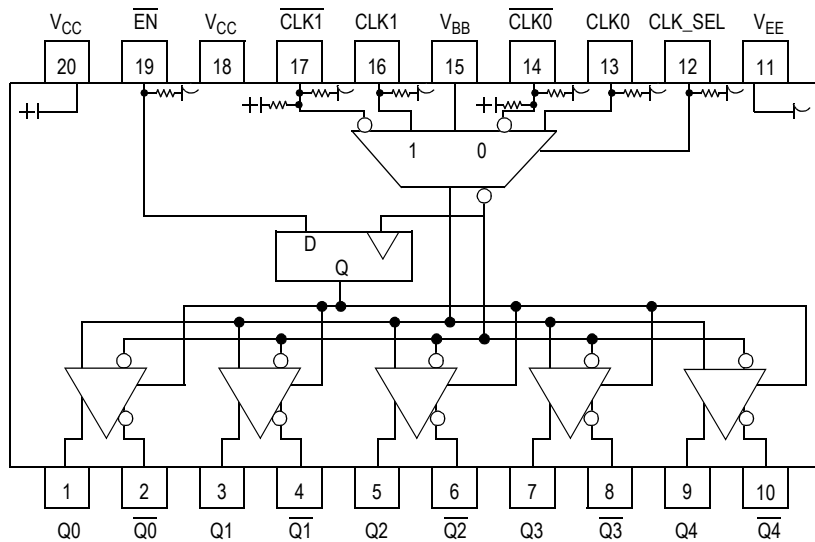
DT SUFFIX
20-LEAD TSSOP PACKAGE
CASE 948E-03



EJ SUFFIX
20-LEAD TSSOP PACKAGE
Pb-FREE PACKAGE
CASE 948E-03

ORDERING INFORMATION

Device	Package
MC100ES6014DT	TSSOP-20
MC100ES6014DTR2	TSSOP-20
MC100ES6014EJ	TSSOP-20 (Pb-Free)
MC100ES6014EJR2	TSSOP-20 (Pb-Free)



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 20-Lead Pinout (Top View) and Logic Diagram

Table 1. Pin Description

Pin	Function
CLK0*, CLK0**	ECL/PECL/HSTL CLK Input
CLK1*, CLK1**	ECL/PECL/HSTL CLK Input
Q0:4, Q0:4	ECL/PECL Outputs
CLK_SEL*	ECL/PECL Active Clock Select Input
EN*	ECL Sync Enable
V _{BB}	Reference Voltage Output
V _{CC}	Positive Supply
V _{EE}	Negative Supply

* Pins will default LOW when left open.

** Pins will default to $V_{CC}/2$ when left open.

Table 2. Function Table

CLK0	CLK1	CLK_SEL	EN	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L*

* On next negative transition of CLK0 or CLK1

Table 3. General specifications

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pullup Resistor		75 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2000 V > 200 V > 1500 V
Thermal Resistance (Junction-to-Ambient)	0 LFPM, 20 TSSOP 500 LFPM, 20 TSSOP	140°C/W 100°C/W

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

Table 4. Absolute Maximum Ratings⁽¹⁾

Symbol	Characteristic	Conditions	Rating	Units
V _{SUPPLY}	Power Supply Voltage	Difference between V _{CC} & V _{EE}	3.9	V
V _{IN}	Input Voltage	V _{CC} – V _{EE} ≤ 3.6 V	V _{CC} + 0.3 V _{EE} – 0.3	V
I _{OUT}	Output Current	Continuous Surge	50 100	mA mA
I _{BB}	V _{BB} Sink/Source Current		±0.5	°C
T _A	Operating Temperature Range		–40 to +85	°C
T _{STG}	Storage Temperature Range		–65 to +150	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. DC Characteristics (V_{CC} = 0 V, V_{EE} = –2.5 V ± 5% or V_{CC} = 2.5 V ± 5%, V_{EE} = 0 V)

Symbol	Characteristics	–40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I _{EE}	Power Supply Current		30	60		30	60	mA
V _{OH}	Output HIGH Voltage ⁽¹⁾	V _{CC} –1250	V _{CC} –990	V _{CC} –800	V _{CC} –1200	V _{CC} –960	V _{CC} –750	mV
V _{OL}	Output LOW Voltage ⁽¹⁾	V _{CC} –2000	V _{CC} –1550	V _{CC} –1150	V _{CC} –1925	V _{CC} –1630	V _{CC} –1200	mV
V _{outPP}	Output Peak-to-Peak Voltage	200			200			mV
V _{IH}	Input HIGH Voltage	V _{CC} –1165		V _{CC} –880	V _{CC} –1165		V _{CC} –880	mV
V _{IL}	Input LOW Voltage	V _{CC} –1810		V _{CC} –1475	V _{CC} –1810		V _{CC} –1475	mV
V _{BB}	Output Reference Voltage I _{BB} = 200 μA	V _{CC} –1400		V _{CC} –1200	V _{CC} –1400		V _{CC} –1200	mV
V _{PP}	Differential Input Voltage ⁽²⁾	0.12		1.3	0.12		1.3	mV
V _{CMR}	Differential Cross Point Voltage ⁽³⁾	V _{EE} +0.2		V _{CC} –1.0	V _{EE} +0.2		V _{CC} –1.0	mV
I _{IN}	Input Current			±150			±150	μA

1. Output termination voltage V_{TT} = 0 V for V_{CC} = 2.5 V operation is supported but the power consumption of the device will increase.
2. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
3. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 6. DC Characteristics (V_{CC} = 0 V, V_{EE} = –3.8 V to –3.135 V or V_{CC} = 3.135 V to 3.8 V, V_{EE} = 0 V)

Symbol	Characteristics	–40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I _{EE}	Power Supply Current		30	60		30	60	mA
V _{OH}	Output HIGH Voltage ⁽¹⁾	V _{CC} –1150	V _{CC} –1020	V _{CC} –800	V _{CC} –1200	V _{CC} –970	V _{CC} –750	mV
V _{OL}	Output LOW Voltage ⁽¹⁾	V _{CC} –1950	V _{CC} –1620	V _{CC} –1250	V _{CC} –2000	V _{CC} –1680	V _{CC} –1300	mV
V _{outPP}	Output Peak-to-Peak Voltage	200			200			mV
V _{IH}	Input HIGH Voltage	V _{CC} –1165		V _{CC} –880	V _{CC} –1165		V _{CC} –880	mV
V _{IL}	Input LOW Voltage	V _{CC} –1810		V _{CC} –1475	V _{CC} –1810		V _{CC} –1475	mV
V _{BB}	Output Reference Voltage I _{BB} = 200 μA	V _{CC} –1400		V _{CC} –1200	V _{CC} –1400		V _{CC} –1200	mV
V _{PP}	Differential Input Voltage ⁽²⁾	0.12		1.3	0.12		1.3	V
V _{CMR}	Differential Cross Point Voltage ⁽³⁾	V _{EE} +0.2		V _{CC} –1.1	V _{EE} +0.2		V _{CC} –1.1	V
I _{IN}	Input Current			±150			±150	μA

1. Output termination voltage V_{TT} = 0 V for V_{CC} = 2.5 V operation is supported but the power consumption of the device will increase.
2. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
3. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 7. AC Characteristics ($V_{CC} = 0\text{ V}$, $V_{EE} = -3.8\text{ V}$ to -3.135 V or $V_{CC} = 3.135\text{ V}$ to 3.8 V , $V_{EE} = 0\text{ V}$)⁽¹⁾

Symbol	Characteristics	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{\max}	Maximum Output Frequency	2			2			2			GHz
t_{PLH} t_{PHL}	Propagation Delay (Differential) CLK to Q, \bar{Q}	300	355	425	300	375	475	300	400	525	ps
t_{SKEW}	Within Device Skew ⁽²⁾ Device-to-Device Skew ⁽²⁾ Q, \bar{Q}		23	45 125		23	45 175		23	45 225	ps ps
t_{JITTER}	Cycle-to-Cycle Jitter RMS (1σ)			1			1			1	ps
V_{PP}	Input Peak-to-Peak Voltage Swing (Differential)	200		1200	200		1200	200		1200	mV
V_{CMR}	Differential Cross Point Voltage	$V_{EE}+0.2$		$V_{CC}-1.2$	$V_{EE}+0.2$		$V_{CC}-1.2$	$V_{EE}+0.2$		$V_{CC}-1.2$	V
t_r/t_f	Output Rise/Fall Time (20%–80%)	70		225	70		250	70		275	ps

1. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 ohms to $V_{CC}-2.0\text{ V}$.

2. Skew is measured between outputs under identical transitions.

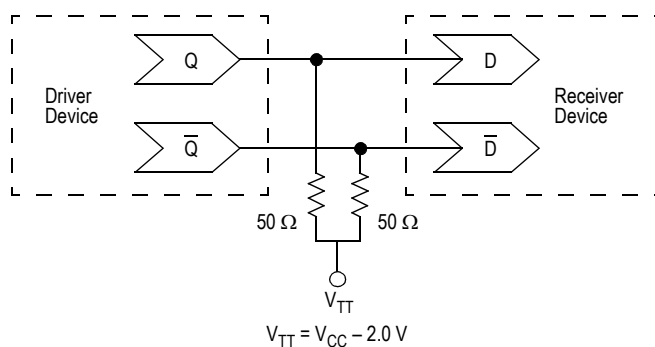
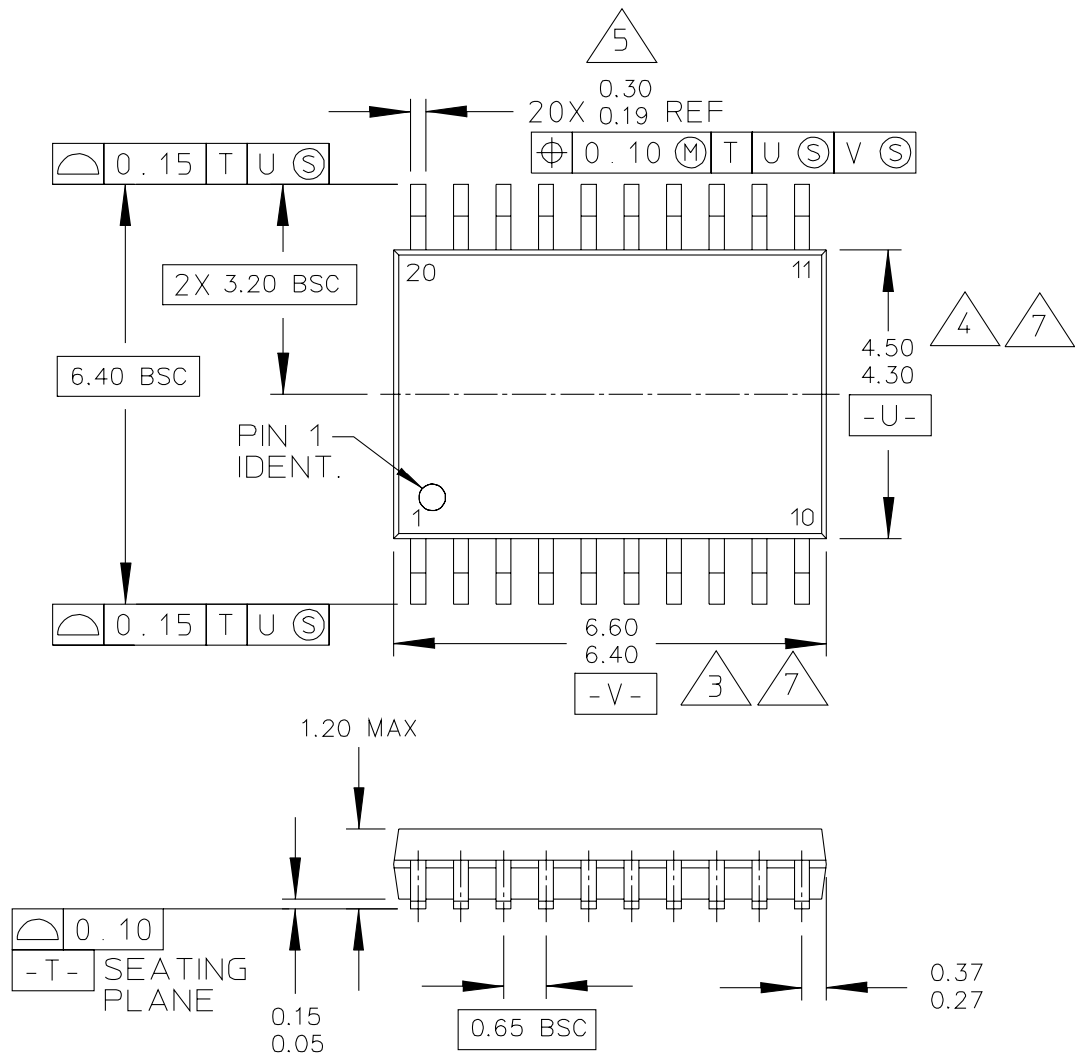


Figure 2. Typical Termination for Output Driver and Device Evaluation

PACKAGE DIMENSIONS



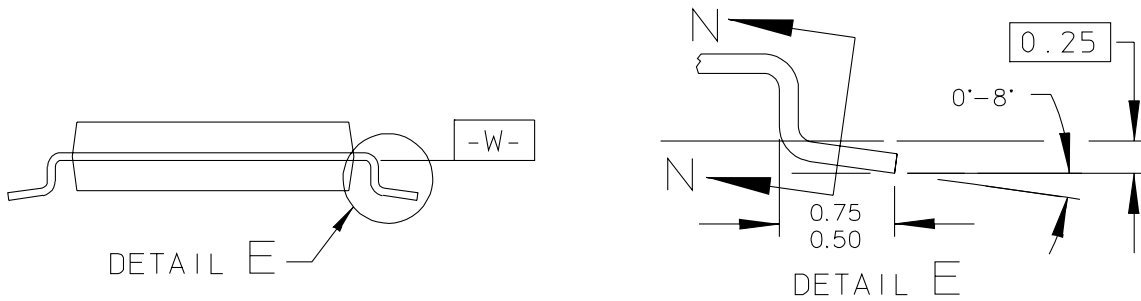
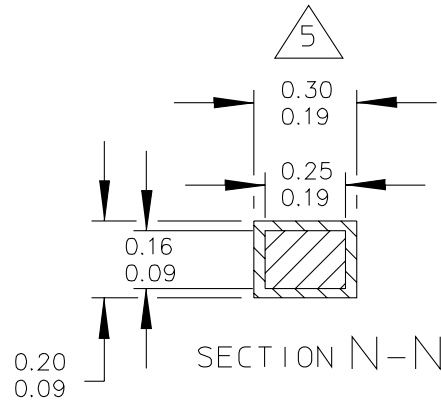
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CASE 948E-03 ISSUE B 20-LEAD TSSOP PACKAGE

MC100ES6014

PACKAGE DIMENSIONS



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ISSUE B
20-LEAD TSSOP PACKAGE**

PACKAGE DIMENSIONS

NOTES:

1. CONTROLLING DIMENSION: MILLIMETER
2. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1982.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS ARE TO BE DETERMINED AT DATUM PLANE -W-.

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