



Die Datasheet, Logic Gate Device

74HC4040

12-STAGE BINARY RIPPLE COUNTER

Die Source:



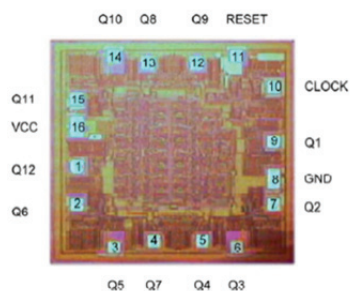
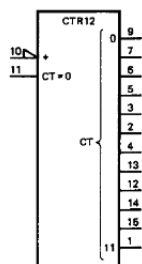
71 mils x 68 mils x 14 mils

Backside : Silicon
Topside Metal: Aluminum

General Description:

The 74HC4040 is a member of the Industries 74xxx series of Logic devices. The 74HC4040 is a device description which contains a 12-stage binary ripple counter.

IEEE / IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITIONS	LIMIT	UNITS
Supply Voltage	V_{CC}		-0.5 to +7.0	V
DC Input Diode Current	I_{IK}	$V_I = -0.5V$ $V_I = V_{CC} + 0.5V$	-20.0 20.0	mA
DC Input Voltage	V_I		-0.5 to $V_{CC} + 0.5$	V
DC Output Diode Current	I_{OK}	$V_O = -0.5V$ $V_O = V_{CC} + 0.5V$	-20.0 20.0	mA
DC Output Voltage	V_O		-0.5 to $V_{CC} + 0.5$	V
DC Output Source or Sink Current	I_O		± 25.0	mA
DC VCC Current	I_{CC}		+50	mA
DC GND Current	I_{DD}		-50.0	mA
Storage Temp	T_{STG}		-65.0 to +150	$^{\circ}C$
Max Junction Temp	T_J		150.0	$^{\circ}C$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	TECH	SYMBOL	LIMIT	UNITS
Supply Voltage	HC	V_{CC}	2.0 to 6.0	V
Input Voltage		V_I	0 to V_{CC}	V
Output Voltage		V_O	0 to V_{CC}	V
Operating Temperature		T_A	-40 to +85	$^{\circ}C$
Minimum Input Rise & Fall times (@5.0V $\pm$ 0.5V)	HC	$\Delta T/\Delta V$	500	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	TECH	SYMBOL	VCC (V)	CONDITIONS	Guaranteed Limits		UNITS	NOTE
					Min@25C	Min@85C		
Minimum HIGH level Input Voltage	HC	V_{IH}	2.0		1.50	1.50	V	
			4.5		3.15	3.15		
			6.0		4.20	4.20		
Maximum LOW level Input Voltage	HC	V_{IL}	2.0		0.50	0.50	V	
			4.0		1.35	1.35		
			4.5		1.80	1.80		
Minimum HIGH level Output Voltage	HC	V_{OH}	2.0	$I_{OUT} = -20\mu A$	1.90	1.90	V	
			4.5		4.40	4.40		
			6.0		5.90	5.90		
	HC	V_{OH}	4.5	$V_{IN} = V_{IL} \text{ or } V_{IH}, I_{OL} = -4mA$	3.98	3.84	V	
			6.0	$V_{IN} = V_{IL} \text{ or } V_{IH}, I_{OL} = -5.2mA$	5.48	5.34		



Die Datasheet, Logic Gate Device

74HC4040

12-STAGE BINARY RIPPLE COUNTER

DC ELECTRICAL CHARACTERISTICS - CONT'D

PARAMETER	TECH	SYMBOL	VCC (V)	CONDITIONS	Guarenteed Limits		UNITS	NOTE
					Min@25C	Min@85C		
Maximum LOW level Output Voltage	HC	V _{OL}	2.0	I _{OUT} = 20uA	0.1	0.1	V	
			4.5		0.1	0.1		
			6.0		0.1	0.1		
	HC	V _{OL}	4.5	V _{IN} = V _{IL} or V _{IH} , I _O = 4mA	0.36	0.44	V	
			6.0	V _{IN} = V _{IL} or V _{IH} , I _O = 5.2mA	0.36	0.44		
Maximum Input Leakage Current	HC	I _{IN}	6.0	V _I = V _{CC} or GND	±0.1	±1.0	uA	
3-State Output OFF Current	HC	I _{OZ}	6.0	V _I = V _{IH} or V _{IL} , V _O = V _{CC} or GND	--	±5.0	uA	
Maximum Quiescent Supply Current	HC	I _{CC}	6.0	V _{IN} = V _{CC} or GND	--	20	uA	

AC ELECTRICAL CHARACTERISTICS

PARAMETER	TECH	SYMBOL	VCC (V)	CONDITIONS	Guarenteed Limits		Guarenteed Limits		UNITS
					Min@25C	Max@25C	Min@85C	Max@85C	
Propagation Delay, CP\ to Q0	HC	t _{PLH}	2.0	GND = 0V, tr = tf = 6ns, CL = 50pF	--	150.0	--	190.0	ns
			4.5		--	30.0	--	38.0	
			6.0		--	26.0	--	33.0	
	HC	t _{PHL}	2.0	GND = 0V, tr = tf = 6ns, CL = 50pF	--	150.0	--	190.0	ns
			4.5		--	30.0	--	38.0	
			6.0		--	26.0	--	33.0	
Propagation Delay, Qn to Qn + 1	HC	t _{PLH}	2.0	GND = 0V, tr = tf = 6ns, CL = 50pF	--	100.0	--	125.0	ns
			4.5		--	20.0	--	25.0	
			6.0		--	17.0	--	21.0	
	HC	t _{PHL}	2.0	GND = 0V, tr = tf = 6ns, CL = 50pF	--	100.0	--	125.0	ns
			4.5		--	20.0	--	25.0	
			6.0		--	17.0	--	21.0	
Propagation Delay, MR to Qn	HC	t _{PHL}	2.0	GND = 0V, tr = tf = 6ns, CL = 50pF	--	185.0	--	230.0	ns
			4.5		--	37.0	--	46.0	
			6.0		--	31.0	--	39.0	



Die Datasheet, Logic Gate Device

74HC4040

12-STAGE BINARY RIPPLE COUNTER

AC ELECTRICAL CHARACTERISTICS - CONT'D									
PARAMETER	TECH	SYMBOL	VCC (V)	CONDITIONS	Guarenteed Limits		Guarenteed Limits		UNITS
					Min@25C	Max@25C	Min@85C	Max@85C	
Output Transition Time	HC	tTLH	2.0	GND = 0V, tr = tf = 6ns, CL = 50pF	--	75.0	--	95.0	ns
			4.5		--	15.0	--	19.0	
			6.0		--	13.0	--	16.0	
	HC	tTHL	2.0	GND = 0V, tr = tf = 6ns, CL = 50pF	--	75.0	--	95.0	ns
			4.5		--	15.0	--	19.0	
			6.0		--	13.0	--	16.0	
Clock Pulse Width, HIGH or LOW	HC	tW	2.0	GND = 0V, tr = tf = 6ns, CL = 50pF	80.0	--	100.0	--	ns
			4.5		16.0	--	20.0	--	
			6.0		14.0	--	16.0	--	
Master Reset Pulse Width, HIGH	HC	tW	2.0	GND = 0V, tr = tf = 6ns, CL = 50pF	80.0	--	100.0	--	ns
			4.5		16.0	--	20.0	--	
			6.0		14.0	--	16.0	--	
Removal Time, MR to CP\	HC	tREM	2.0	GND = 0V, tr = tf = 6ns, CL = 50pF	50.0	--	65.0	--	ns
			4.5		10.0	--	13.0	--	
			6.0		9.0	--	11.0	--	
Maximum Clock Pusle Frequency	HC	fMAX	2.0	GND = 0V, tr = tf = 6ns, CL = 50pF	6.0	--	4.8	--	MHz
			4.5		30.0	--	24.0	--	
			6.0		35.0	--	28.0	--	