TIMING AND SYNCHRONIZATION

PRODUCT CATALOG

ZARLINK SEMICONDUCTOR

QUICK GLANCE SELECTOR GUIDE

LINE CARD SYNCHRONIZATION

Zarlink offers the industry's widest range of phase locked-loops (PLLs) for high performance line card synchronization. Complying with Telecordia and ITU-T jitter performance from T1/E1 up to 10G/OC-192/STM-64, the products support a wide range of input frequencies required for telecom and datacom equipment.

The highly integrated, feature-rich chips—with multiple outputs, redundancy protection, and low-power consumption—help simplify the design of networking equipment that meets the latest performance requirements.

Applications

- Optical equipment used in DWDM & WDM networks
- SONET/SDH equipment such as Multi-Service Provisioning Platforms (MSPP)
- Routers and switches
- Add-Drop Multiplexers (ADM)
- Wireless base stations and Node B
- Wireless base station controllers and radio network controllers
- Metro Ethernet equipment
- Integrated Access Devices (IAD)
- Multi-Service Access Platforms (MSAP)
- Passive Optical Network (PON) equipment
- Gateways
- Digital Subscriber Line Access Multiplexers (DSLAM)

Product Features

- Meets Ethernet/SONET/SDH jitter generation requirements up to 10G/OC-192/STM-64
- Multiple PLLs per device for rate conversion
- Supports ITU-T G.8262 requirements for Synchronous Ethernet slave clocks (EEC option 1 & option 2)
- Input synchronizes to telecom reference clocks or to Ethernet reference clocks
- Output generates standard SONET/SDH clock rates or standard Ethernet clock rates
- Line card redundancy protection such as manual or automatic hitless reference switching
- Low power consumption

		SyncE/SONET/SDH				SyncE		SONET/SDH	PDH
		ZL30131	**ZL30132**	**ZL30146**	**ZL30145**	**ZL30136**	**ZL30321**	**ZL30108**	**ZL30106**
Jitter compliance		up to 10G/ OC-192/ STM-64	up to 10G/ OC-192/ STM-64	up to 10G/ OC-192/ STM-64	up to 10G/ OC-192/ STM-64	Gigabit	Gigabit	OC-3/ STM-1	PDH, OC-3/ STM-1
Number of rate conversion Digital PLLs		2	1	2	1	1	2	1	1
Maximum frequency (MHz)		622.08	622.08	622.08	622.08	125	125	19.44	65.536
Number of SONET/SDH/ Ethernet outputs	CMOS	2	1	1	1	1	2	1	1
	Differential	2	1	1	1	0	0	0	0
Number of PDH/TDM outputs (CMOS)		4	1	1	0	1	4	0	7
Number of frame pulse outputs (CMOS)		2	1	1	0	1	2	2	4
Programmable synthesizers (N x 8 kHz)		2	1	1	0	1	2	0	0
Number of reference inputs		8	3	5	1	3	8	2	3
Sync inputs for output frame pulse alignment		3	3	1	0	3	3	0	2
Package size		9 x 9 mm CABGA	9 x 9 mm CABGA	9 x 9 mm CABGA	9 x 9 mm CABGA	9 x 9 mm CABGA	9 x 9 mm CABGA	5 x 5 mm QFN	10 x 10 mm TQFP

TIMING CARD SYNCHRONIZATION

Zarlink's timing card synchronization products are easy-to-adopt, standards-compliant solutions that deliver critical end-to-end network timing performance while helping equipment manufactures reduce costs and speed time-to-market

The highly integrated, single-chip solutions ease system integration, lower component count and reduce power consumption, while meeting ANSI, ETSI and Telecordia standards as well as the ITU-T Recommendation G.8262 for Synchronous Ethernet timing requirements. Deployed in a range of access, wireless, router and Metro Ethernet applications, Zarlink's timing card synchronization solutions allow service providers to deliver truly reliable voice, video, data and mobile services over packet networks.

Applications

- Optical equipment used in DWDM & WDM networks
- SONET/SDH equipment such as Multi-Service Provisioning Platforms (MSPP)
- Routers and switches
- Add-Drop Multiplexers (ADM)
- Wireless base stations and Node B
- Wireless base station controllers and radio network controllers
- Metro Ethernet equipment
- Integrated Access Devices (IAD)
- Multi-Service Access Platforms (MSAP)
- Passive Optical Network (PON) equipment
- Gateways
- Digital Subscriber Line Access Multiplexers (DSLAM)

Product Features

- Meets the requirements of ITU-T G.8262 for synchronous Ethernet Equipment slave clocks (EEC Option 1 & Option 2)
- Generates standard SONET/SDH clock rates or Ethernet clock rates up to 622 MHz
- Additional programmable output synthesizer generates telecom clock frequencies from any multiple of 8 kHz to 100 MHz
- Generates several styles of telecom frame pulses with selectable pulse width, polarity & frequency
- Provides automatic reference switching & holdover during loss of reference input
- Internal state machine automatically controls mode of operation (free-run, locked, hold-over)
- Supports master/slave configuration
- Configurable input to output delay
- Configurable output to output phase alignment
- Lowest power for similar solutions

		SyncE/SONET/SDH			
		ZL30138	**ZL30130**	**ZL30143**	**ZL30142**
ITU-T G.8262 (EEC Option 1/Option 2)		✓	✓	✓	✓
GR-1244 SONET Stratum 2/3E		✓	✓		
GR-253 SONET Stratum 3		✓	✓	✓	✓
GR-1244 Stratum 3		✓	✓	✓	✓
GR-1244 Stratum 4/4E		✓	✓	✓	✓
ITU-T G.813 Option 1/Option 2		✓	✓	✓	✓
Number of independent digital PLLs		2	2	2	1
Number of reference inputs		9	9	9	3
Sync inputs for output frame pulse alignment		4	4	4	3
Number of SONET/SDH/ Ethernet outputs	CMOS	2	2	2	1
	Differential	2	2	2	1
Number of PDH/TDM outputs (CMOS)		4	4	4	1
Number of frame pulse outputs (CMOS)		4	4	4	1
Programmable synthesizers (N x 8 kHz)		2	2	2	1
Jitter compliance		up to 10G/OC-192/STM-64	up to 1G/OC-12/STM-4	up to 10G/OC-48/STM-16	up to 10G/OC-48/STM-16
Maximum frequency Ethernet (MHz)		312.5	125	312.5	312.5
Maximum frequency SONET/SDH (MHz)		622.08	622.08	622.08	622.08
Package size		9 x 9 mm CABGA	9 x 9 mm CABGA	9 x 9 mm CABGA	9 x 9 mm CABGA

Product Features

- Supports standards from Telecordia , ANSI, ETSI & ITU
- Accepts wide range of common telecom input frequencies
- Provides a wide range of telecom clocks & frame pulses
- Holdover accuracy equal to or better than 1.5×10^{-7}
- Manual or automatic hitless reference switching
- Simple hardware control interface

	ZL30105	ZL30101	ZL30102	ZL30109	ZL30100
GR-1244 Stratum 3	✓	✓			
GR-1244 Stratum 4/4E	✓	✓	✓	✓	✓
Number of independent digital PLLs	1	1	1	1	1
Number of reference inputs	3	2	3	2	2
Sync inputs for output frame pulse alignment	1	0	1	0	0
Number of SONET/SDH/Ethernet outputs (CMOS)	1	0	0	1	0
Number of PDH/TDM outputs (CMOS)	7	5	7	5	5
Number of frame pulse outputs (CMOS)	4	3	3	4	3
Jitter compliance	up to OC-3/ STM-1	PDH Interfaces	PDH Interfaces	up to OC-3/ STM-1	PDH Interfaces
Maximum output frequency (MHz)	65.536	65.536	65.536	65.536	65.536
Package size	10 x 10 mm TGFP	10 x 10 mm TGFP	10 x 10 mm TGFP	10 x 10 mm TGFP	10 x 10 mm TGFP

RATE CONVERSION PLLs

Zarlink's telecom rate conversion phase locked loops (PLLs) provide accurate and reliable frequency conversion for telecom, enterprise and access equipment. Targeting volume designs, the products deliver required performance with integrated reference monitoring to ensure system reliability.

Applications

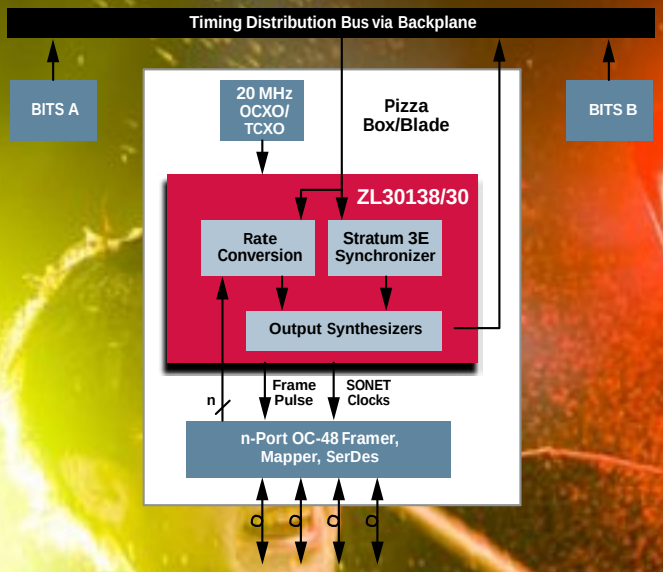
- Passive Optical Network Terminal (ONT)
- Integrated Access Device (IAD)
- Voice over IP (VoIP) line cards
- Private Branch Exchange (PBX)
- Channel bank

Product Features

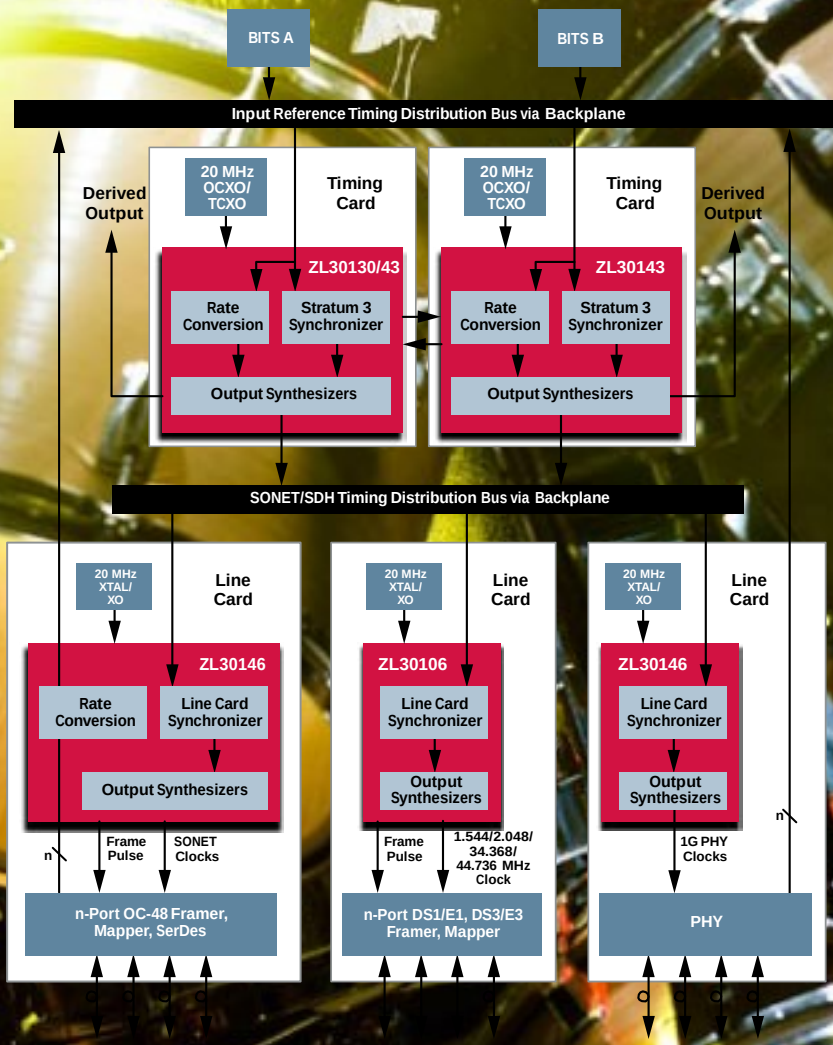
- Standard input frequencies of 8 kHz, 2.048 MHz, 8.192 MHz, or 19.44 MHz
- Provides a selection of telecom frequencies
- Less than 0.6 nspp intrinsic jitter on TDM clock outputs
- Status output pins for lock indication & reference failure
- Goes to free run mode when the reference fails
- Provides reset pin for control
- Simple hardware control interface
- Small package: 5mm x 5mm, QFN package

	ZL30110	ZL30112	ZL30113
Rate conversion DPLL with stand by capability	✓		
Number of reference inputs	1	1	1
Number of CMOS outputs	9	1	1
Synthesizers	65.536 MHz, 100/66 MHz 125 & 25 MHz	2.048 MHz 8.192 MHz	65.536 MHz
Fanout capability	✓		
Number of frame pulse outputs	0	1	1
Package	5 x 5 mm QFN	5 x 5 mm QFN	5 x 5 mm QFN

Distributed Timing For Pizza Box



Centralized System Timing And Blade Applications



Zarlink's Timing and Synchronization solutions are based on a foundation of over 20 years of expertise in designing leading-edge products that ensure maximum network uptime while meeting strict performance requirements.

Highly Integrated Solutions: Complete solutions that reduce bill-of-material costs, board space and power consumption

Simplify Design: Easy-to-adopt products, fully supported by design tools, evaluation boards, software and dedicated support teams, to simplify and shorten your design cycle

Standards Compliant: Designed to meet the latest performance requirements, including ITU-T Recommendation G.8262 for Synchronous Ethernet, to achieve quality of transmission and reliable carrier-grade services

Our state-of-the-art Line Card and Timing Card synchronization solutions increase performance, reduce costs and keep our customers ahead of the technology curve.

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www.zarlink.com/**timing**.htm