

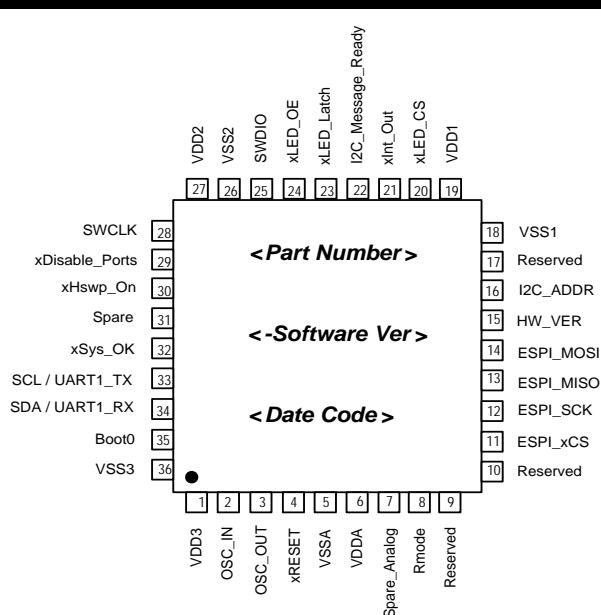
PoE Controller Unit
DATASHEET
DESCRIPTION

Microsemi's[™] PoE controller, PD69100, is a cost-effective, pre-programmed unit designed to implement Enhanced mode. It is used in conjunction with Microsemi's PoE Managers PD69108 and PD69104 in Ethernet switches to enable next generation network devices to share power and data over the same cable, as specified in IEEE802.3af and IEEE802.3at standards. Enhanced mode operation along with PD69108/PD69104 managers enables operation in a total Power-over-Ethernet stand-alone mode.

The controller features an ESPI bus for each PoE device and a communication interface with Host CPU via UART or I²C protocol.

Device is based on STMicroelectronics family STM32F101T6 embedded with ARM Cortex[™]-M3 core. It includes the following peripherals:

- 3 x Timers
- 2 x Uarts
- 1 x SPI
- 1 x I²C
- 1 x 12-bit analog-to-digital converter

PIN CONFIGURATION

KEY FEATURES

- ♦ Controls up to 48 PoE ports (6 x PD69108)
- ♦ Pre-Standard / Capacitor detection
- ♦ Detection of Cisco devices
- ♦ Supports both UART and I²C interfaces to Host CPU
- ♦ Backwards compatible with PD69000, PD63000, PD62000 and PDIC66000
- ♦ Supports 2 pair RJ or 4 pair RJ
- ♦ 16 power banks support using four discrete lines connected directly to PD69108 / PD69104.
- ♦ Power management for up to 96 ports
- ♦ Rmode pin for default parameters selection
- ♦ Programmable over-voltage and under voltage
- ♦ Predefined power budget; 16 discrete levels
- ♦ LED stream support
- ♦ System OK indication
- ♦ Software download via I²C or UART
- ♦ System and port measurements
- ♦ Detailed port status
- ♦ Thermal protection and monitoring
- ♦ Programmable temperature alarm limit
- ♦ Interrupt out pin for system and port events
- ♦ Forced power for system testing
- ♦ System reset
- ♦ Port power limit setting
- ♦ Port matrix and priority
- ♦ Automatic PoE device type detection
- ♦ RoHS compliant

MARKETING DEFINITIONS

Device's label includes the following:

- ♦ <Part number> Hardware P/N (for example PD69100)
- ♦ <-Software Ver> Software version (for example. 0120)
- ♦ <Date Code> Burning date code in the following format: yyww (yy = year, ww = week)

FIRMWARE DOWNLOAD

Initial burning of controller's firmware is performed in factory. Firmware upgrades can be performed by users using communication interface (see *application note 126 catalogue number 06-0006-080*).

ORDERING INFORMATION

| | |
|--------------------|---|
| Part Number | PD69100y-gggg |
| Detection | y = R: Resistor y = C: Resistor/legacy |
| Version | gggg |

* For latest firmware version available, refer to Microsemi's website or Customer Care Support.

**APPLICABLE DOCUMENTS**

- ♦ IEEE 802.3af-2003 standard, DTE Power via MDI
- ♦ IEEE 802.3at-2009 standard, DTE Power via MDI
- ♦ Microsemi PD69108 datasheet , catalogue number DS_PD69108
- ♦ Microsemi PD69104 datasheet , catalogue number DS_PD69104
- ♦ Microsemi Serial communication protocol user guide , catalogue number 06-0054-080
- ♦ Microsemi application note 174 for Designing 48-port Enhanced PoE System (802.3af/802.3at Compliant), catalogue number 06-0054-080
- ♦ Microsemi Application note 126 Software Download for PoE Units, catalogue number 06-0006-080
- ♦ ST-Microelectronics STM32F101x6 datasheet

PIN FUNCTIONALITY

| PIN | PIN NAME | PIN TYPE | PIN DESCRIPTION |
|-----|---------------|------------|-----------------------------------|
| 1. | VDD3 | Supply | Main Supply 3.3V |
| 2. | OSC_IN | Oscillator | Oscillator Input |
| 3. | OSC_OUT | Oscillator | Oscillator Output |
| 4. | xRESET (NRST) | IN | Reset Input |
| 5. | VSSA | AGND | Analog Ground |
| 6. | VDDA | Supply | Main Supply 3.3V |
| 7. | Spare_Analog | Analog_IN | N/A |
| 8. | Rmode | Analog_IN | Pre Defined Power Budget Settings |
| 9. | Reserved | OUT | Software Debug Uart |
| 10. | Reserved | IN | Software Debug Uart |
| 11. | ESPI_xCS | OUT | ESPI Bus to PoE Manager |
| 12. | ESPI_SCK | OUT | ESPI Bus to PoE Manager |
| 13. | ESPI_MISO | IN | ESPI Bus to PoE Manager |
| 14. | ESPI_MOSI | OUT | ESPI Bus to PoE Manager |
| 15. | HW_VER | Analog_IN | Hardware Version |
| 16. | I2C_ADDR | Analog_IN | I2C address of PD69100 |
| 17. | Reserved | IN | Not Used (Must be Puledl Up) |
| 18. | VSS1 | DGND | Digital Ground |
| 19. | VDD1 | Supply | Main Supply 3.3V |
| 20. | xLed_Cs | OUT | Chip Select for LED Stream |

| PIN | PIN NAME | PIN TYPE | PIN DESCRIPTION |
|-----|-------------------|-------------------------------|--|
| 21. | xInt_Out | OUT | Interrupt Output Indication |
| 22. | I2C_Message_Ready | OUT | Signals message is ready to be read by Host, |
| 23. | xLED_Latch | OUT | Latch for LED stream |
| 24. | xLED_OE | OUT | Enable for status LED |
| 25. | SWDIO | DEBUG | Serial Debug Data Bus |
| 26. | VSS2 | DGND | Digital Ground |
| 27. | VDD2 | Supply | Main Supply 3.3V |
| 28. | SWCLK | DEBUG | Serial Debug Data Bus Clock |
| 29. | xDisable_Ports | IN | Disable all PoE Ports |
| 30. | xHswp_On | OUT | External Hot Swap Device Enable |
| 31. | Spare | SPARE I/O | N/A (PB4) |
| 32. | xSys_OK | OUT | System Validity Indication |
| 33. | SCL / UART1_Tx | IN / OUT | I2C Clock or UART Transmit |
| 34. | SDA / UART1_RX | IN / OUT | I2C Data or UART Receive |
| 35. | | input only Must pulled low | |
| 36. | Boot0 | | Device Boot Configuration |
| | VSS3 | DGND | Digital Ground |

ELECTRICAL SPECIFICATION

For a detailed electrical specification refer to the following datasheets at www.st.com.

- **Manufacturer:** STMicroelectronics
- **Manufacturer part number:** STM32F101T6U6



MAIN FEATURES DESCRIPTION

| Function | Description |
|---|---|
| Supports up to eight PoE devices – 96 ports | Up to 12 PoE devices can be cascaded, fitting into a 96 port PoE system that utilizes one PoE controller (PD69100) |
| Power Management | The system supports three power management modes: Class (LLDP) mode, Dynamic mode and Static mode. For more details see <i>technical note 113, catalogue number 06-0002-081</i> . |
| Threshold Configuration | Configure overvoltage and under-voltage thresholds for disconnection purposes. |
| High power ports, 2 pairs or 4 pairs | PoE devices can be configured (both hardware and software) to enable higher current through ports (up to ~720mA) or double power RJ in case of 4 pairs. |
| Communication | Supports both I ² C and UART interfaces with Host CPU. |
| Legacy (capacitor) Detection | Enables detection and powering of pre-standard devices (PDs). |
| LED Stream | Direct SPI interface to an external LED stream circuitry. Enables designers to implement a simple LED circuit that does not require a software code. |
| System OK Indication | Digital output pin to Host, indicating voltage and temperature range are valid. |
| System and Port Measurements | Measurements of the following parameters: Current (mA), Power Consumption (W), V _{main} (V), Port Voltage (V), PD Class (0-4). |
| Detailed Port Status | Port statuses are received from PoE managers. Statuses such as 'port on' and 'port off due to disconnection or due to overload' |
| Interrupt Pin | Interrupt out from PoE controller indicating events such as: port on, port off, port fault, PoE device fault, voltage out of range, and more. For a full list of interrupt events refer to <i>Serial Communication Protocol, catalogue number 06-0032-056</i> . |
| Port Power Limit | Configurable port power limit; when a port exceeds the limit, it is automatically disconnected |
| Port Matrix Control | Enables layout designers to connect all physical ports to logical ports whenever required. |
| 'Power Good' Interrupt from Power Supply Directly to POE Drivers. | For systems comprising more than a single power supply, in case one power supply fails, a fast port disconnection mechanism is executed to maintain operation and prevent collapse of other power supplies. |

I²C ADDRESS SELECTION

I²C interface between Host CPU and a specific PD69000 requires setting the device address; this is done by applying a specific voltage level to pin #25 (I2C_ADDR) as shown below:

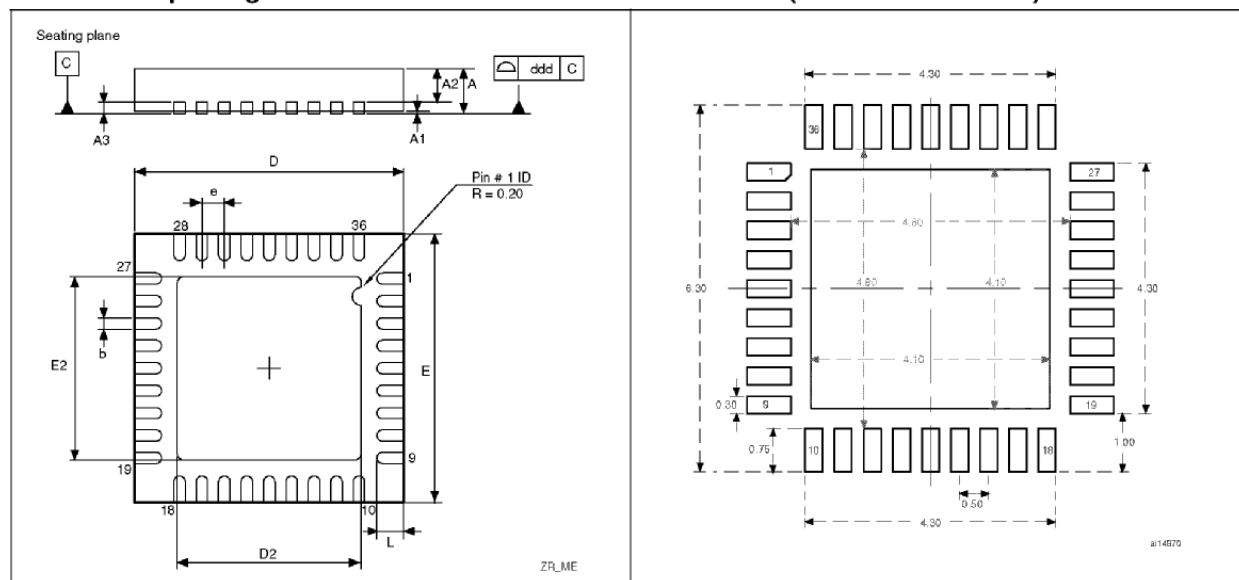
| I2C_ADDR VOLTAGE LEVEL | I ² C ADDRESS (HEXADECIMAL) |
|-----------------------------|---|
| 0.00 to 0.21V _{DC} | UART |
| 0.21 to 0.41V _{DC} | 0x4 |
| 0.41 to 0.62V _{DC} | 0x8 |
| 0.62 to 0.83V _{DC} | 0xC |
| 0.83 to 1.03V _{DC} | 0x10 |
| 1.03 to 1.24V _{DC} | 0x14 |
| 1.24 to 1.44V _{DC} | 0x18 |
| 1.44 to 1.65V _{DC} | 0x1C |
| 1.65 to 1.86V _{DC} | 0x20 |
| 1.86 to 2.06V _{DC} | 0x24 |
| 2.06 to 2.27V _{DC} | 0x28 |
| 2.27 to 2.48V _{DC} | 0x2C |
| 2.48 to 2.68V _{DC} | 0x30 |
| 2.68 to 2.89V _{DC} | 0x34 |
| 2.89 to 3.09V _{DC} | 0x38 |
| 3.09 to 3.30V _{DC} | 0x3C |



PACKAGE INFORMATION

PD69100 is housed in a 36-pin VQFPN plastic package, 6 x 6 x 0.9 mm.

Figure 31. VFQFPN36 6 x 6 mm, 0.5 mm pitch, package outline⁽¹⁾ **Figure 32. Recommended footprint (dimensions in mm)⁽¹⁾⁽²⁾⁽³⁾**



1. Drawing is not to scale.
2. The back-side pad is not internally connected to the V_{SS} or V_{DD} power pads.
3. There is an exposed die pad on the underside of the VFQFPN package. It should be soldered to the PCB. All leads should also be soldered to the PCB.

Table 47. VFQFPN36 6 x 6 mm, 0.5 mm pitch, package mechanical data

| Symbol | millimeters | | | inches ⁽¹⁾ | | |
|--------|-------------|-------|-------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.800 | 0.900 | 1.000 | 0.0315 | 0.0354 | 0.0394 |
| A1 | | 0.020 | 0.050 | | 0.0008 | 0.0020 |
| A2 | | 0.650 | 1.000 | | 0.0256 | 0.0394 |
| A3 | | 0.250 | | | 0.0098 | |
| b | 0.180 | 0.230 | 0.300 | 0.0071 | 0.0091 | 0.0118 |
| D | 5.875 | 6.000 | 6.125 | 0.2313 | 0.2362 | 0.2411 |
| D2 | 1.750 | 3.700 | 4.250 | 0.0689 | 0.1457 | 0.1673 |
| E | 5.875 | 6.000 | 6.125 | 0.2313 | 0.2362 | 0.2411 |
| E2 | 1.750 | 3.700 | 4.250 | 0.0689 | 0.1457 | 0.1673 |
| e | 0.450 | 0.500 | 0.550 | 0.0177 | 0.0197 | 0.0217 |
| L | 0.350 | 0.550 | 0.750 | 0.0138 | 0.0217 | 0.0295 |
| ddd | | 0.080 | | | 0.0031 | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.



The information contained in the document is PROPRIETARY AND CONFIDENTIAL information of Microsemi and cannot be copied, published, uploaded, posted, transmitted, distributed or disclosed or used without the express duly signed written consent of Microsemi. If the recipient of this document has entered into a disclosure agreement with Microsemi, then the terms of such Agreement will also apply. This document and the information contained herein may not be modified, by any person other than authorized personnel of Microsemi. No license under any patent, copyright, trade secret or other intellectual property right is granted to or conferred upon you by disclosure or delivery of the information, either expressly, by implication, inducement, estoppels or otherwise. Any license under such intellectual property rights must be approved by Microsemi in writing signed by an officer of Microsemi. Microsemi reserves the right to change the configuration, functionality and performance of its products at anytime without any notice. This product has been subject to limited testing and should not be used in conjunction with life-support or other mission-critical equipment or applications. Microsemi assumes no liability whatsoever, and Microsemi disclaims any express or implied warranty, relating to sale and/or use of Microsemi products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right. The product is subject to other terms and conditions which can be located on the web at <http://www.microsemi.com/legal/tnc.asp>

Revision History

| Revision Level / Date | Para. Affected | Description |
|------------------------|----------------|--------------------------------|
| 0.1 / 15 February 2010 | | Initial release |
| 0.2 Dec 2010 | | Ordering information update |
| 1.1 / Jan 2011 | | Updating template and proofing |

© 2009 Microsemi Corp.
All rights reserved.

For support contact: sales_AMSG@microsemi.com

Visit our web site at: www.microsemi.com

Cat. No. DS_PD69100