NX2838

SINGLE SUPPLY HIGH FREQUENCY ADJUSTABLE SYNCHRONOUS PWM CONTROLLER WITH A 3.3V/700mA LDO

Pb Free Product

DESCRIPTION

The NX2838 controller IC is a single power supply synchronous Buck controller IC designed for step down DC to DC converter applications. NX2838 is optimized to convert bus voltages from 8V to 32V to output voltage as low as 0.8V. The internal 3.3V output LDO can provide output current up to 700mA. An internal regulator converts bus voltage to 5V, which provides voltage supply to internal logic and driver circuit. The NX2838 operates from 200kHz to 1MHz and employs loss-less current limiting by sensing the Rdson of synchronous MOSFET followed by hiccup feature.Feedback under voltage triggers Hiccup.

Other features of the device are: 3.3V LDO power good indicator, Thermal shutdown, 5V gate drive, Adaptive deadband control, Internal digital soft start, Vcc undervoltage lock out and Shutdown capability via the comp pin.

FEATURES

- Single supply voltage from 8V to 32V
- Internal 5V regulator
- Programmable frequency up to 1MHz
- Internal Digital Soft Start Function
- Internal 700mA 3.3VLDO with Power Goood indicator
- Prebias Startup
- Less than 50 nS adaptive deadband
- Current limit triggers hiccup by sensing Rdson of Synchronous MOSFET
- Pb-free and RoHS compliant

APPLICATIONS

- LCD TV
- Graphic Card on board converters
- On board DC to DC application
- Hard Disk Drive
- Set Top Box

TYPICAL APPLICATION

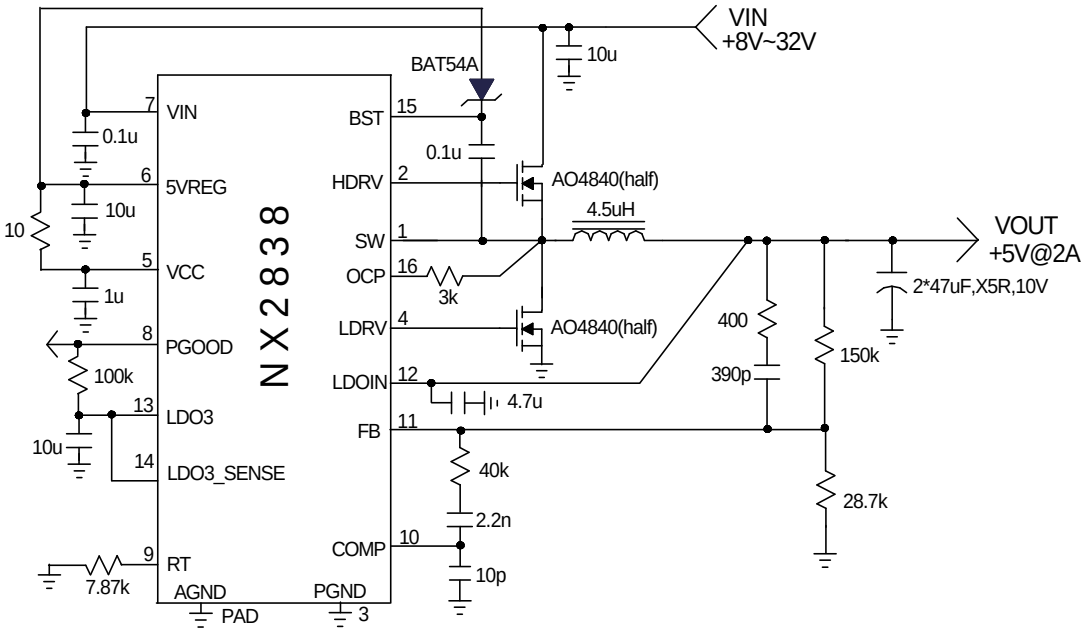


Figure1 - Typical application of 2838

ORDERING INFORMATION

Device	Temperature	Package	Frequency	Pb-Free
NX2838CMTR	0 to 70° C	3X3 MLPQ-16L	200kHz to 1MHz	Yes

Package Marking : NX2838XXX XXX is date code. For example, 735 means that this NX2838 is packaged in the 35th week of 2007

Microsemi
Analog Mixed Signal Group
11861 Western Avenue, Garden Grove, CA. 92841, 800-877-6458, 714-898-8121, Fax: 714-893-2570

ABSOLUTE MAXIMUM RATINGS(NOTE1)

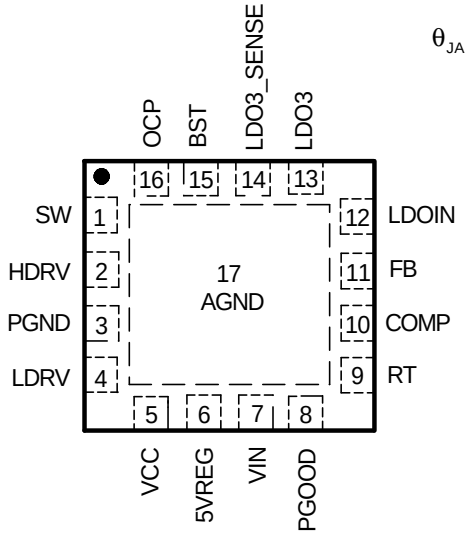
VCC to GND & BST to SW voltage 6.5V
BST to GND Voltage 45V
VIN to GND Voltage 35V
SW to GND ..... -2V(100nS pulse) to 45V
All other pins ..... -0.3V to 6.5V
Operating Junction Temperature Range ..... -40°C to 125°C
Storage Temperature Range ..... -65°C to 150°C

NOTE1: Stresses above those listed in "ABSOLUTE MAXIMUM RATINGS", may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

PACKAGE INFORMATION

16-LEAD PLASTIC 3X3 MLPQ

$\theta_{JA} \approx 46^{o}C/W$



ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vin = 12V, Vcc=5VREG, LDOIN=5V, LDO LOAD=5mA and T_A = 25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature. Followings are bypass capacitors:C_{VIN}=1uF, C_{5VREG}=10uF, C_{LDO3}=10uF, all X5R ceramic capacitors.

PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
Reference Voltage						
Ref Voltage	V_{REF}		0.784	0.8	0.816	V
Ref Voltage line regulation		V_{in}=8V to 30V		0.4		%
Supply Voltage(Vin)						
V_{in} Voltage Range	V_{in}		8		32	V
Input Voltage Current(Static)		V_{in}=12V,no switching	3	3.9	5.3	mA
Input Voltage Current (Dynamic)		V_{in}=12V, switching with HDRV and LDRV open	3.5	5.2	6	mA
Vin UVLO						
V_{in}-Threshold	V_{in}_UVLO	V_{in} Rising	6	6.5	7.5	V
V_{in}-Hysteresis	V_{in}_Hyst	V_{in} Falling		0.6		V

Microsemi
Analog Mixed Signal Group
11861 Western Avenue, Garden Grove, CA. 92841, 800-877-6458, 714-898-8121, Fax: 714-893-2570

PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
5V REG						
5VREG Output			4.75	5	5.3	V
5VREG Line Regulation		V_{IN}=8V to 30V		10	20	mV
5VREG Max Current			20	50		mA
Under Voltage Lockout						
V_{CC}-Threshold	V_{CC}_UVLO	V_{CC} Rising	3.4	3.9	4.4	V
V_{CC}-Hysteresis	V_{CC}_Hyst	V_{CC} Falling		0.2		V
SS						
Soft Start time	Tss	F_S=1MHz		1		mS
Oscillator (Rt)						
Frequency	F_S	Rt=7.87k	800	1000	1200	kHz
Ramp-Amplitude Voltage	V_{RAMP}		1.4	1.5	1.9	V
Max Duty Cycle		F_S=1MHz	68	78	85	%
Min Controlable On Time					150	nS
Error Amplifiers						
Transconductance			1500	2000	2500	umho
Input Bias Current	Ib			10		nA
Comp SD Threshold			0.24	0.3	0.36	V
FBUVLO						
Feedback UVLO threshold			0.54	0.6	0.66	V
High Side Driver(C_L=2200pF)						
Output Impedance , Sourcing	R_{source}(Hdrv)	I=200mA		1.9		ohm
Output Impedance , Sinking	R_{sink}(Hdrv)	I=200mA		1.7		ohm
Rise Time	THdrv(Rise)			14		ns
Fall Time	THdrv(Fall)			17		ns
Deadband Time	Tdead(L to H)	Ldrv going Low to Hdrv going High, 10%-10%		30		ns
Low Side Driver (C_L=2200pF)						
Output Impedance, Sourcing Current	R_{source}(Ldrv)	I=200mA		1.9		ohm
Output Impedance, Sinking Current	R_{sink}(Ldrv)	I=200mA		1		ohm
Rise Time	TLdrv(Rise)			13		ns
Fall Time	TLdrv(Fall)			12		ns
Deadband Time	Tdead(H to L)	SW going Low to Ldrv going High, 10% to 10%		10		ns
3.3V LDO						
LDOIN voltage range					5.5	V
Output Voltage		LDO_SENSE connected to LDO OUT	3.23	3.3	3.37	V
Line regulation		LDO_IN=4.5V to 5.5V		5	10	mV
Load regulation					2	%
Current limit				900		mA
Drop out Voltage		LDOIN ramping down till LDOOUT drops by 50mV. I_{LOAD}=500mA		500	900	mV

Microsemi
Analog Mixed Signal Group
11861 Western Avenue, Garden Grove, CA. 92841, 800-877-6458, 714-898-8121, Fax: 714-893-2570

PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
OCP						
OCP current			30	37	45	uA
Power Good(Pgood)						
Threshold Voltage as % of Vref		FB ramping up	88	90	94	%
Hysteresis				5		%
Over temperature						
Threshold				150		^{o}C
Hysteresis				20		^{o}C

Microsemi
Analog Mixed Signal Group
11861 Western Avenue, Garden Grove, CA. 92841, 800-877-6458, 714-898-8121, Fax: 714-893-2570

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
1	SW	This pin is connected to the source of the high side MOSFET and provides return path for the high side driver.
2	HDRV	High side MOSFET gate driver.
3	PGND	Power Ground.
4	LDRV	Low side MOSFET gate driver.
5	VCC	IC's supply voltage. This pin biases the internal logic circuits. A high freq 1uF ceramic capacitor is placed as close as possible to and connected from this pin to ground pin.
6	5VREG	An internal 5V regulator output which provides supply voltage for the low side fet driver . A high frequency 10uF ceramic capacitor must be connected from this pin to the GND pin as close as possible.
7	VIN	Voltage supply for the internal 5V regulator.
8	PGOOD	An open drain output that requires a pull up resistor to LDO3 or Vcc. When LDO3_sense reaches threshold, PGOOD transitions from LO to HI state.
9	RT	Oscillator's frequency can be set by using an external resistor from this pin to GND.
10	COMP	This pin is the output of the error amplifier and is used to compensate the voltage control feedback loop. This pin is also used as a shut down pin. When this pin is pulled below 0.3V, both drivers are turned off and internal soft start is reset.
11	FB	This pin is the error amplifier inverting input. This pin is connected via resistor divider to the output of the switching regulator to set the output DC voltage.
12	LDOIN	3.3V LDO input supply voltage.
13	LDO3	This pin is the output of internal 3.3V LDO. A minimum of 10uF/X5R capacitor must be connected from this pin to ground to ensure stability.
14	LDO3_SENSE	This pin is used to sense the output voltage of LDO. This pin is directly connected to the output of the LDO regulator.
15	BST	This pin supplies voltage to the high side driver. A high frequency ceramic capacitor of 0.1 to 1 uF must be connected from this pin to SW pin.
16	OCP	This pin is connected to the drain of the external low side MOSFET and is the input of the over current protection(OCP) comparator. An internal current source is flown to the external resistor which sets the OCP voltage across the Rdson of the low side MOSFET. Current limit point is this voltage divided by the Rds-on.
PAD	AGND	Analog ground.

Microsemi
Analog Mixed Signal Group
11861 Western Avenue, Garden Grove, CA. 92841, 800-877-6458, 714-898-8121, Fax: 714-893-2570

Typical Application (8~32V to 5V/2A)

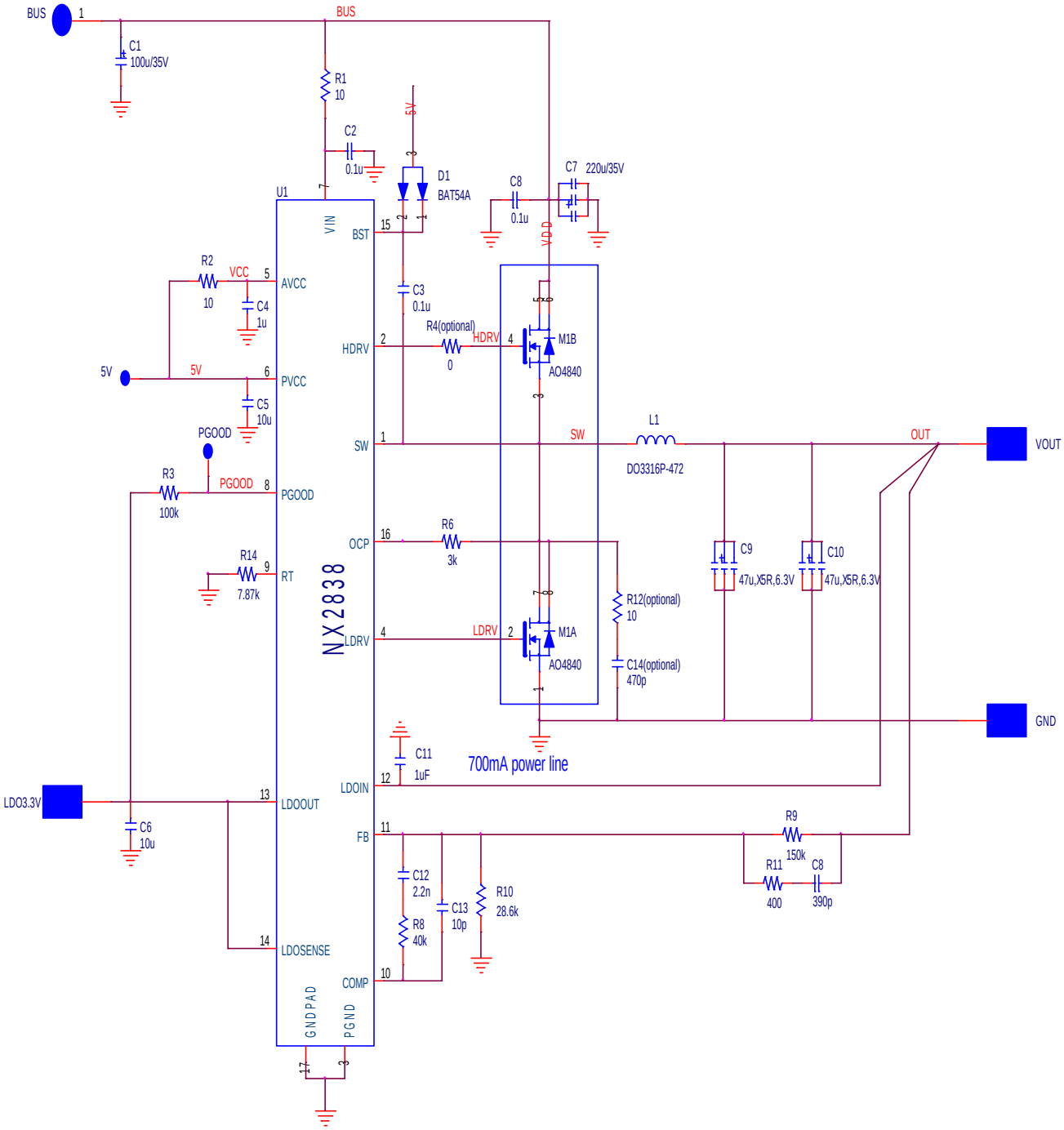


Figure2 - Schematic of typical application

Microsemi
Analog Mixed Signal Group
11861 Western Avenue, Garden Grove, CA. 92841, 800-877-6458, 714-898-8121, Fax: 714-893-2570

Bill of Materials

Item	Quantity	Reference	Part
1	1	C1	100u/35V
2	3	C2,C3,C8	0.1u
3	2	C4	1u
4	1	C6,C5	10u
5	1	C7	220u/35V
6	1	C8	390p
7	2	C9,C10	47u,X5R,6.3V
8	1	C11	1uF
9	1	C12	2.2n
10	1	C13	10p
11	1	C14	470p
12	1	D1	BAT54A
13	1	L1	DO3316P-472
14	1	M1	AO4840
15	3	R1,R2,R12	10
16	1	R3	100k
17	3	R4	0
18	1	R6	3k
19	1	R8	40k
20	1	R9	150k
21	1	R10	28.6k
22	1	R11	400
23	1	R14	7.87k
24	1	U1	NX2838

Microsemi
Analog Mixed Signal Group
11861 Western Avenue, Garden Grove, CA. 92841, 800-877-6458, 714-898-8121, Fax: 714-893-2570

Demoboard waveforms(VIN=8~32V,VOUT=5V)

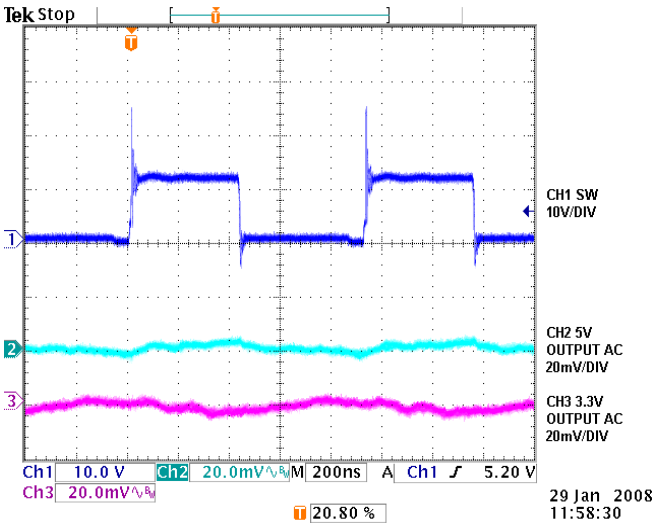


Figure 3 - Output ripple

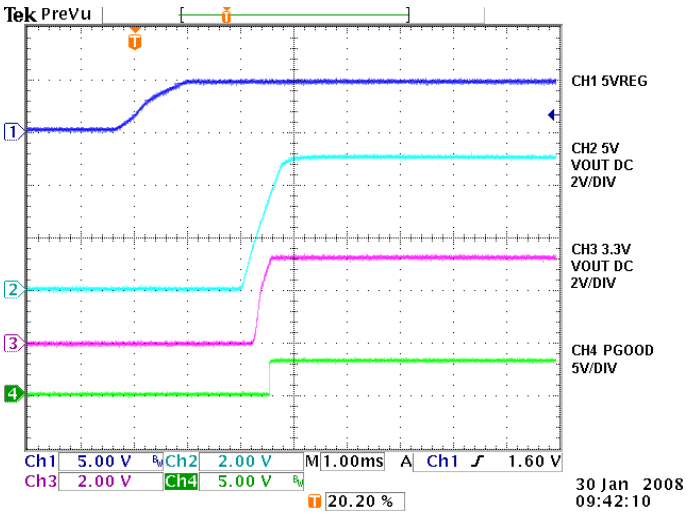


Figure 4 - Start up time

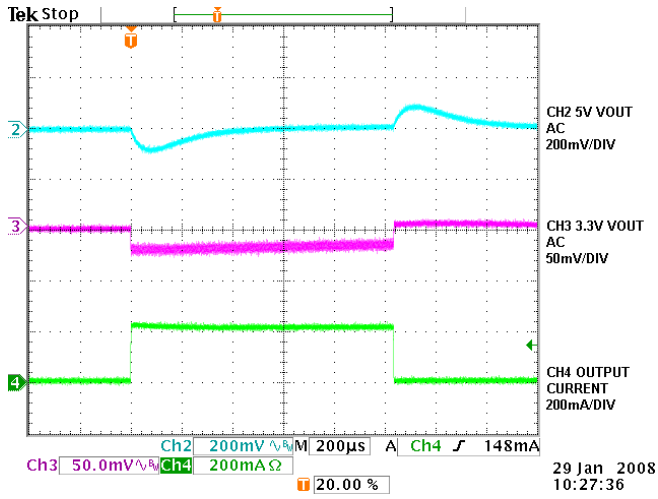


Figure 5 - Transient response with 200mA@3.3V output

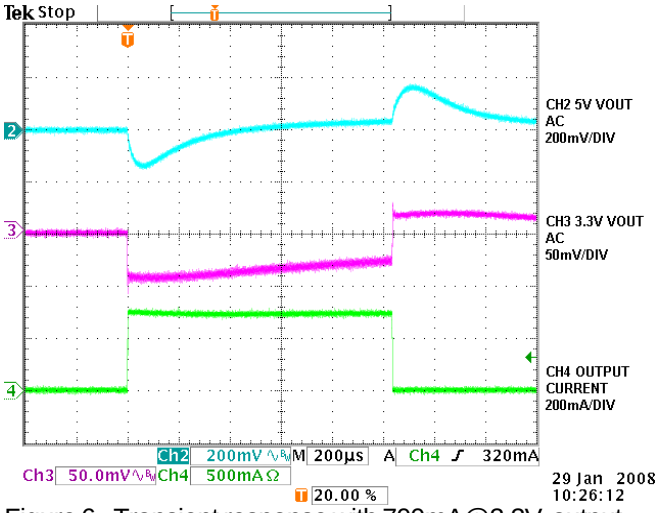


Figure 6 - Transient response with 700mA@3.3V output

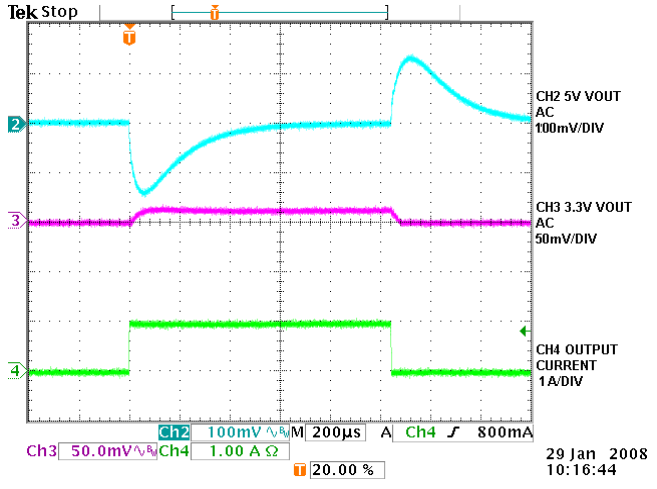


Figure 7 - Transient response with 1A@5V output

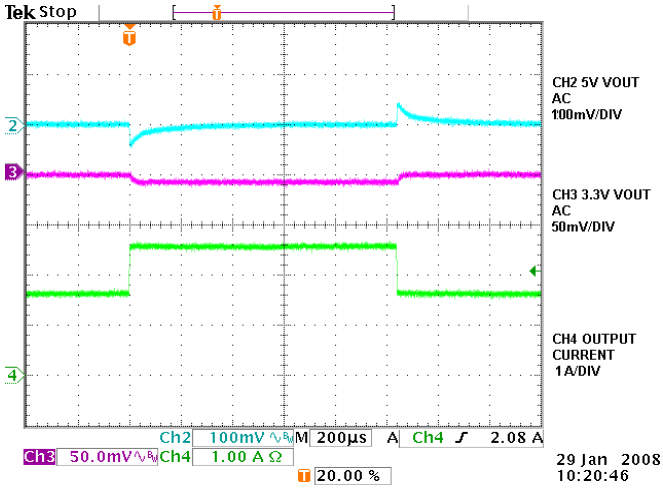


Figure 8 - Transient response with 1A@5V output

Microsemi
Analog Mixed Signal Group
11861 Western Avenue, Garden Grove, CA. 92841, 800-877-6458, 714-898-8121, Fax: 714-893-2570

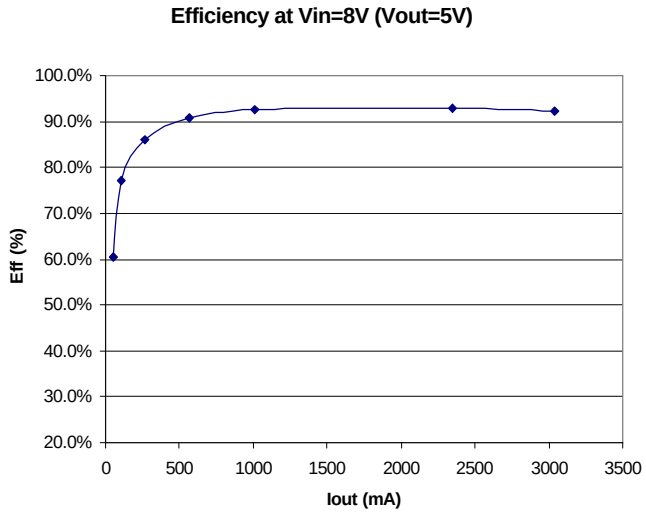


Figure 9 - Efficiency (VIN=8V,VOUT=5V)

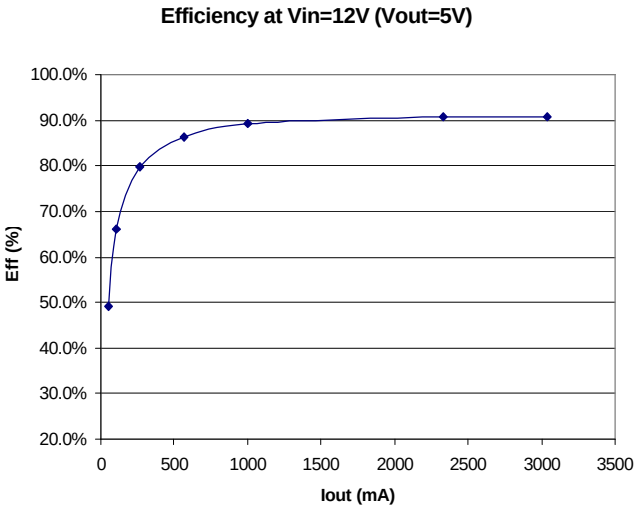


Figure 10 - Efficiency (VIN=12V,VOUT=5V)

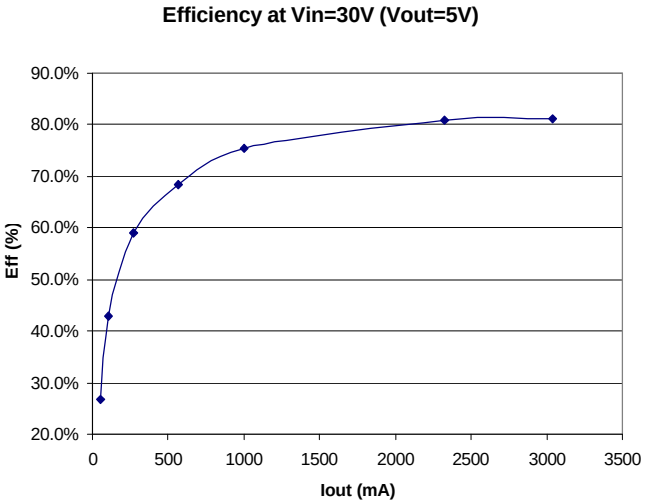


Figure 11 - Efficiency (VIN=30V,VOUT=5V)

Microsemi
Analog Mixed Signal Group
11861 Western Avenue, Garden Grove, CA. 92841, 800-877-6458, 714-898-8121, Fax: 714-893-2570

APPLICATION INFORMATION

Symbol Used In Application Information:

V_{IN} - Input voltage
V_{OUT} - Output voltage
I_{OUT} - Output current
ΔV_{RIPPLE} - Output voltage ripple
F_S - Working frequency
ΔI_{RIPPLE} - Inductor current ripple

Design Example

The following is typical application for NX2838, the schematic is figure 1.

V_{IN} = 8V to 32V
V_{OUT}=5V
F_S=1MHz
I_{OUT}=2A
ΔV_{RIPPLE}<=50mV
ΔV_{DROOP}<=250mV @ 1A step

Output Inductor Selection

The selection of inductor value is based on inductor ripple current, power rating, working frequency and efficiency. Larger inductor value normally means smaller ripple current. However if the inductance is chosen too large, it brings slow response and lower efficiency. Usually the ripple current ranges from 20% to 40% of the output current. This is a design freedom which can be decided by design engineer according to various application requirements. The inductor value can be calculated by using the following equations:

$$L_{OUT}=\frac{V_{IN}-V_{OUT}}{\Delta I_{RIPPLE}}\times\frac{V_{OUT}}{V_{IN}}\times\frac{1}{F_S} \quad ...(1)$$

$$I_{RIPPLE}=k\times I_{OUTPUT}$$

where k is between 0.2 to 0.4.
Select k=0.4, then

$$L_{OUT}=\frac{32V-5V}{0.4\times 2A}\times\frac{5V}{32V}\times\frac{1}{1MHz}$$

$$L_{OUT}=5.3uH$$

Choose inductor from COILCRAFT DO3308P-472 with L=4.7uH is a good choice.

Current Ripple is recalculated as

$$\Delta I_{RIPPLE}=\frac{V_{IN}-V_{OUT}}{L_{OUT}}\times\frac{V_{OUT}}{V_{IN}}\times\frac{1}{F_S}$$
$$=\frac{32V-5V}{4.7uH}\times\frac{5V}{32V}\times\frac{1}{1MHz}=0.898A \quad ...(2)$$

Output Capacitor Selection

Output capacitor is basically decided by the amount of the output voltage ripple allowed during steady state(DC) load condition as well as specification for the load transient. The optimum design may require a couple of iterations to satisfy both condition.

Based on DC Load Condition

The amount of voltage ripple during the DC load condition is determined by equation(3).

$$\Delta V_{RIPPLE}=ESR\times\Delta I_{RIPPLE}+\frac{\Delta I_{RIPPLE}}{8\times F_S\times C_{OUT}} \quad ...(3)$$

Where ESR is the output capacitors' equivalent series resistance,C_{OUT} is the value of output capacitors.

Typically ceramic capacitors are chosen as output capacitors, both terms in equation (3) need to be evaluated to determine the overall ripple. Usually when this type of capacitors are selected, the amount of capacitance per single unit is not sufficient to meet the transient specification, which results in parallel configuration of multiple capacitors .

For example, two 47uF(10V,X5R, 2mΩ) ceramic capacitor are used. The amount of output ripple is

$$\Delta V_{RIPPLE}=1m\Omega\times 0.887A+\frac{0.887A}{8\times 1MHz\times 94uF} \quad ...(4)$$
$$=2mV$$

If large value capacitors are selected such as Aluminum Electrolytic,POSCAP and OSCON types are used, the amount of the output voltage ripple is dominated by the first term in equation(3) and the second term can be neglected. The ESR and inductor current typically determines the output voltage ripple.

$$ESR_{desire}=\frac{\Delta V_{RIPPLE}}{\Delta I_{RIPPLE}}$$

If low ESR is required, for most applications, multiple capacitors in parallel are better than a big capacitor. The number of capacitor is calculated as follows:

$$N = \frac{ESR_E \times \Delta I_{RIPPLE}}{\Delta V_{RIPPLE}} \quad ...(5)$$

Although these calculation meets DC ripple spec, it still needs to be studied for transient requirement. Overall, we choose N=2.

Compensator Design

Due to the double pole generated by LC filter of the power stage, the power system has 180° phase shift , and therefore, is unstable by itself. In order to achieve accurate output voltage and fast transient response,compensator is employed to provide highest possible bandwidth and enough phase margin.Ideally,the Bode plot of the closed loop system has crossover frequency between1/10 and 1/5 of the switching frequency, phase margin greater than 50° and the gain crossing 0dB with -20dB/decade. Power stage output capacitors usually decide the compensator type. If electrolytic capacitors are chosen as output capacitors, type II compensator can be used to compensate the system, because the zero caused by output capacitor ESR is lower than crossover frequency. Otherwise type III compensator should be chosen.

A. Type III compensator design

For low ESR output capacitors, typically such as Sanyo oscap and poscap, the frequency of ESR zero caused by output capacitors is higher than the crossover frequency. In this case, it is necessary to compensate the system with type III compensator. The following figures and equations show how to realize the type III compensator by transconductance amplifier.

$$F_{Z1} = \frac{1}{2 \times \pi \times R_4 \times C_2} \quad ...(6)$$

$$F_{Z2} = \frac{1}{2 \times \pi \times (R_2 + R_3) \times C_3} \quad ...(7)$$

$$F_{P1} = \frac{1}{2 \times \pi \times R_3 \times C_3} \quad ...(8)$$

$$F_{P2} = \frac{1}{2 \times \pi \times R_4 \times \frac{C_1 \times C_2}{C_1 + C_2}} \quad ...(9)$$

where F_{Z1},F_{Z2},F_{P1} and F_{P2} are poles and zeros in the compensator. Their locations are shown in figure 4.

The transfer function of type III compensator for transconductance amplifier is given by:

$$\frac{V_e}{V_{OUT}} = \frac{1 - g_m \times Z_f}{1 + g_m \times Z_{in} + Z_{in} / R_1}$$

For the voltage amplifier, the transfer function of compensator is

$$\frac{V_e}{V_{OUT}} = \frac{-Z_f}{Z_{in}}$$

To achieve the same effect as voltage amplifier, the compensator of transconductance amplifier must satisfy this condition: R_4>>2/gm. And it would be desirable if $R_1||R_2||R_3$>>1/gm can be met at the same time.

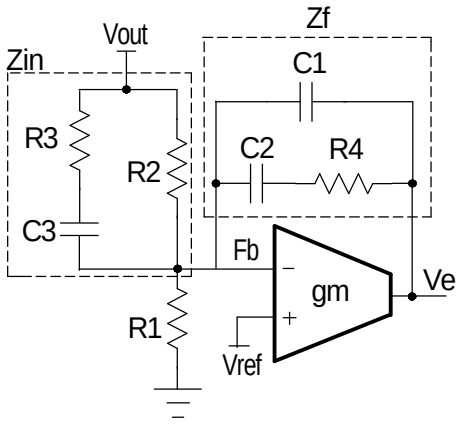


Figure 12 - Type III compensator using transconductance amplifier

Case 1: $F_{LC}<F_O<F_{ESR}$

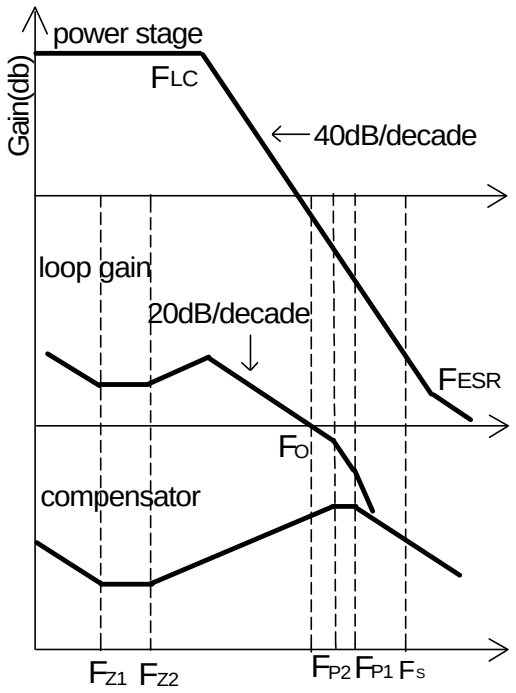


Figure 13 - Bode plot of Type III compensator

Design example for type III compensator are in order. The crossover frequency has to be selected as $F_{LC}<F_O<F_{ESR,}$ and $F_O<=1/10\sim1/5F_{s.}$

1.Calculate the location of LC double pole F_{LC} and ESR zero F_{ESR}.

$$F_{LC}=\frac{1}{2\times\pi\times\sqrt{L_{OUT}\times C_{OUT}}}=\frac{1}{2\times\pi\times\sqrt{4.7uH\times 94uF}}=7.5kHz$$

$$F_{ESR}=\frac{1}{2\times\pi\times ESR\times C_{OUT}}=\frac{1}{2\times\pi\times 2m\Omega\times 47uF}=1.7MHz$$

2. Set R_2 equal to 150kΩ.

$$R_1=\frac{R_2\times V_{REF}}{V_{OUT}-V_{REF}}=\frac{150k\Omega\times 0.8V}{5V-0.8V}=28.6k\Omega$$

Choose R_1=28.6kΩ.

3. Set zero $F_{Z2}=0.35F_{LC}$ and $F_{p1}=F_{ESR}$.

4. Calculate R_4 and C_3 with the crossover frequency at 1/10~ 1/5 of the switching frequency. Set F_O=100kHz.

$$C_3=\frac{1}{2\times\pi\times R_2}\times\left(\frac{1}{F_{z2}}-\frac{1}{F_{p1}}\right)=\frac{1}{2\times\pi\times 150k\Omega}\times\left(\frac{1}{0.35\times 7.5kHz}-\frac{1}{1.7MHz}\right)=400pF$$

$$R_4=\frac{V_{OSC}}{V_{in}}\times\frac{2\times\pi\times F_O\times L}{C_3}\times C_{out}=\frac{1.5V}{32V}\times\frac{2\times\pi\times 100kHz\times 4.7uH}{390pF}\times 94uF=44k\Omega$$

Choose C_3=390pF, R_4=40kΩ.

5. Calculate C_2 with zero F_{z1} at 25% of the LC double pole by equation (6).

$$C_2=\frac{1}{2\times\pi\times F_{Z1}\times R_4}=\frac{1}{2\times\pi\times 0.25\times 7.5kHz\times 40k\Omega}=2.1nF$$

Choose C_2=2.2nF.

6. Calculate C_1 by equation (9) with pole F_{p2} at half the switching frequency.

$$C_1=\frac{1}{2\times\pi\times R_4\times F_{P2}}=\frac{1}{2\times\pi\times 40k\Omega\times 500kHz}=8pF$$

Choose C_1=10pF

7. Calculate R_3 by equation (8).

$$R_3=\frac{1}{2\times\pi\times F_{P1}\times C_3}=\frac{1}{2\times\pi\times 1.7MHz\times 390pF}=241\Omega$$

Choose R_3=300Ω.

Case 2: $F_{LC}<F_{ESR}<F_O$

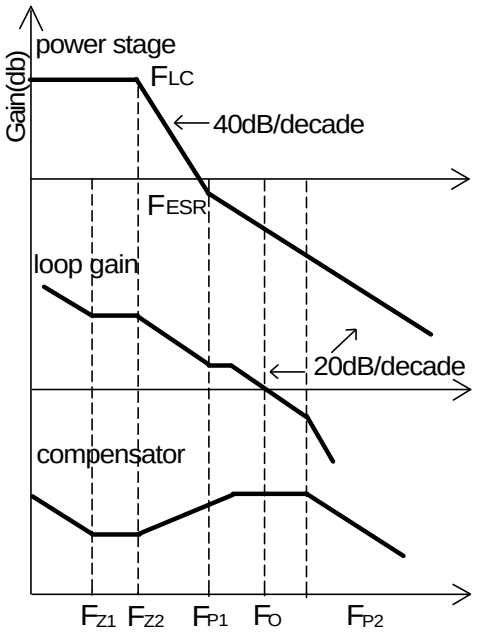


Figure 14 - Bode plot of Type III compensator ($F_{LC}<F_{ESR}<F_O$)

If electrolytic capacitors are used as output capacitors, typical design example of type III compensator in which the crossover frequency is selected as $F_{LC}<F_{ESR}<F_O$ and $F_O<=1/10~1/5F_s$ is shown as the following steps. In this example, Vin is 12V,Vout is 1.2V, two SANYO MV-WG1000 with 30 mΩ is chosen as output capacitor, output inductor is 2.2uH, frequency is 300kHz.

1. Calculate the location of LC double pole F_{LC} and ESR zero F_{ESR}.

$$F_{LC}=\frac{1}{2\times\pi\times\sqrt{L_{OUT}\times C_{OUT}}}=\frac{1}{2\times\pi\times\sqrt{2.2uH\times 2000uF}}=1.8kHz$$

$$F_{ESR}=\frac{1}{2\times\pi\times ESR\times C_{OUT}}=\frac{1}{2\times\pi\times 15m\Omega\times 2000uF}=5.3kHz$$

2. Set R_2 equal to 15kΩ.

$$R_1=\frac{R_2\times V_{REF}}{V_{OUT}-V_{REF}}=\frac{15k\Omega\times 0.8V}{1.8V-0.8V}=12k\Omega$$

Choose R_1=12kΩ.

3. Set zero $F_{Z2}=F_{LC}$ and $F_{p1}=F_{ESR}$.

4. Calculate C_3.

$$C_3=\frac{1}{2\times\pi\times R_2}\times\left(\frac{1}{F_{z2}}-\frac{1}{F_{p1}}\right)=\frac{1}{2\times\pi\times 15k\Omega}\times\left(\frac{1}{1.8kHz}-\frac{1}{5.3kHz}\right)=2.4nF$$

Choose C_3=2.7nF.

5. Calculate R_3.

$$R_3=\frac{1}{2\times\pi\times F_{P1}\times C_3}=\frac{1}{2\times\pi\times 5.3kHz\times 2.7F}=11.1k\Omega$$

Choose R_3=11kΩ.

6. Calculate R_4 with F_O=30kHz.

$$R_4=\frac{V_{OSC}}{V_{in}}\times\frac{2\times\pi\times F_O\times L}{ESR}\times\frac{R_2\times R_3}{R_2+R_3}=\frac{1.5V}{12V}\times\frac{2\times\pi\times 30kHz\times 2.2uH}{15m\Omega}\times\frac{15k\Omega\times 11k\Omega}{15k\Omega+11k\Omega}=21.8k\Omega$$

Choose R_4=22kΩ.

7. Calculate C_2 with zero F_{z1} at 75% of the LC double pole by equation (11).

$$C_2=\frac{1}{2\times\pi\times F_{Z1}\times R_4}=\frac{1}{2\times\pi\times 0.75\times 1.8kHz\times 22k\Omega}=3.05nF$$

Choose C_2=3.3nF.

8. Calculate C_1 by equation (14) with pole F_{p2} at half the switching frequency.

$$C_1=\frac{1}{2\times\pi\times R_4\times F_{P2}}=\frac{1}{2\times\pi\times 22k\Omega\times 150kHz}=48pF$$

Choose C_1=47pF.

B. Type II compensator design

If the electrolytic capacitors are chosen as power stage output capacitors, usually the Type II compensator can be used to compensate the system.

Type II compensator can be realized by simple RC circuit without feedback as shown in figure 16. R_3 and C_1 introduce a zero to cancel the double pole effect. C_2 introduces a pole to suppress the switching noise. The following equations show the compensator pole zero location and constant gain.

$$Gain=g_m \times \frac{R_1}{R_1+R_2} \times R_3 \quad \text{... (10)}$$

$$F_z=\frac{1}{2\times\pi\times R_3\times C_1} \quad \text{... (11)}$$

$$F_p \approx \frac{1}{2\times\pi\times R_3\times C_2} \quad \text{... (12)}$$

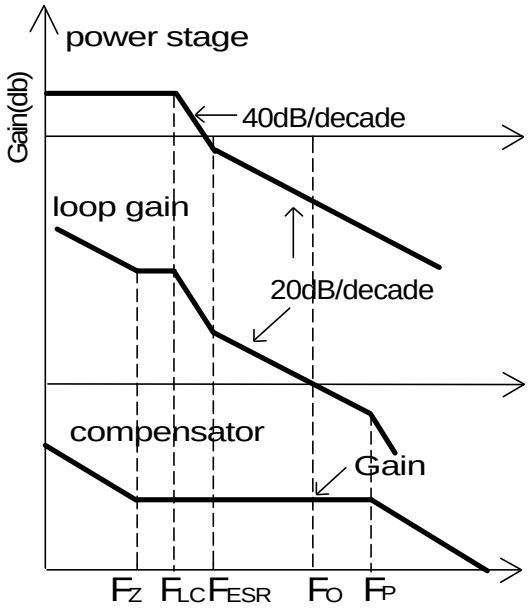


Figure 15 - Bode plot of Type II compensator

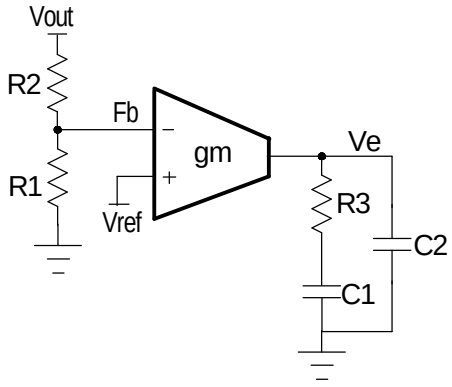


Figure 16 - Type II compensator with transconductance amplifier

For this type of compensator, F_O has to satisfy $F_{LC}<F_{ESR}<<F_O<=1/10\sim1/5F_s$.

The following is parameters for type II compensator design. Input voltage is 30V, output voltage is 5V, output inductor is 10uH, output capacitor is one 1000uF with 30mΩ electrolytic capacitor, frequency is 300kHz.

1.Calculate the location of LC double pole F_{LC} and ESR zero F_{ESR}.

$$F_{LC}=\frac{1}{2\times\pi\times\sqrt{L_{OUT}\times C_{OUT}}}$$
$$=\frac{1}{2\times\pi\times\sqrt{10uH\times1000uF}}$$
$$=1.6kHz$$

$$F_{ESR}=\frac{1}{2\times\pi\times ESR\times C_{OUT}}$$
$$=\frac{1}{2\times\pi\times30m\Omega\times1000uF}$$
$$=5.3kHz$$

2.R_1 and R_2 are set to have fixed 5V output. The value of R_1 is chosen 0.8kΩ, and the value of R_2 is chosen 4.2kΩ.

3. Set crossover frequency at 1/10~ 1/5 of the swithing frequency, here F_O=35kHz.

4.Calculate R_3 value by the following equation.

$$R_3 = \frac{V_{OSC}}{V_{in}} \times \frac{2 \times \pi \times F_O \times L}{R_{ESR}} \times \frac{1}{g_m} \times \frac{V_{OUT}}{V_{REF}}$$
$$= \frac{1.5V}{12V} \times \frac{2 \times \pi \times 35kHz \times 10uH}{30m\Omega} \times \frac{1}{2.0mA/V} \times \frac{5V}{0.8V}$$
$$= 28.6k\Omega$$

Choose R_3 =28kΩ.

5. Calculate C_1 by setting compensator zero F_z at 75% of the LC double pole.

$$C_1 = \frac{1}{2 \times \pi \times R_3 \times F_z}$$
$$= \frac{1}{2 \times \pi \times 28k\Omega \times 0.75 \times 1.6kHz}$$
$$= 4.76nF$$

Choose C_1=4.7nF.

6. Calculate C_2 by setting compensator pole F_p at half the swithing frequency.

$$C_2 = \frac{1}{\pi \times R_3 \times F_s}$$
$$= \frac{1}{p \times 28k\Omega \times 350kHz}$$
$$= 32.5pF$$

Choose C_1=33pF.

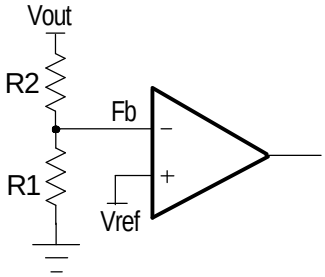
Output Voltage Calculation

Output voltage is set by reference voltage and external voltage divider. The reference voltage is fixed at 0.8V. The divider consists of two ratioed resistors so that the output voltage applied at the Fb pin is 0.8V when the output voltage is at the desired value. The following equation and picture show the relationship between V_{OUT} , V_{REF} and voltage divider.

$$R_1 = \frac{R_2 \times V_{REF}}{V_{OUT} - V_{REF}} \quad ...(13)$$

where R_2 is part of the compensator, and the value of R_1 value can be set by voltage divider.

See compensator design for R_1 and R_2 selection.



Voltage divider

Figure 17 - Voltage divider

Input Capacitor Selection

Input capacitors are usually a mix of high frequency ceramic capacitors and bulk capacitors. Ceramic capacitors bypass the high frequency noise, and bulk capacitors supply switching current to the MOSFETs. Usually 1uF ceramic capacitor is chosen to decouple the high frequency noise.The bulk input capacitors are decided by voltage rating and RMS current rating. The RMS current in the input capacitors can be calculated as:

$$I_{RMS} = I_{OUT} \times \sqrt{D} \times \sqrt{1-D}$$
$$D = \frac{V_{OUT}}{V_{IN}} \quad ...(14)$$

V_{IN} = 12V, V_{OUT}=5V, I_{OUT}=3A, using equation (14), the result of input RMS current is 1.48A.

For higher efficiency, low ESR capacitors are recommended. One Sanyo electrolytic capacitor 35ME470WX(35V 470uF) with 1.8A RMS rating are chosen as input bulk capacitors.

Power MOSFETs Selection

The power stage requires two N-Channel power MOSFETs. The selection of MOSFETs is based on maximum drain source voltage, gate source voltage, maximum current rating, MOSFET on resistance and power dissipation. The main consideration is the power loss contribution of MOSFETs to the overall converter efficiency. For example, two IRFR3706 are used. They have the following parameters: V_{DS}=30V, I_D=75A,R_{DSON} =9mΩ,Q_{GATE} =23nC.

There are two factors causing the MOSFET power loss:conduction loss, switching loss.

Conduction loss is simply defined as:

$$P_{HCON}=I_{OUT}^{2}\times D\times R_{DS(ON)}\times K$$
$$P_{LCON}=I_{OUT}^{2}\times(1-D)\times R_{DS(ON)}\times K \quad ...(15)$$
$$P_{TOTAL}=P_{HCON}+P_{LCON}$$

where the $R_{DS(ON)}$ will increases as MOSFET junction temperature increases, K is $R_{DS(ON)}$ temperature dependency. As a result, $R_{DS(ON)}$ should be selected for the worst case, in which K approximately equals to 1.4 at 125°C according to IRFR3706 datasheet. Conduction loss should not exceed package rating or overall system thermal budget.

Switching loss is mainly caused by crossover conduction at the switching transition. The total switching loss can be approximated.

$$P_{SW}=\frac{1}{2}\times V_{IN}\times I_{OUT}\times T_{SW}\times F_S \quad ...(16)$$

where I_{OUT} is output current, T_{SW} is the sum of T_R and T_F which can be found in mosfet datasheet, and F_S is switching frequency. Switching loss P_{SW} is frequency dependent.

Also MOSFET gate driver loss should be considered when choosing the proper power MOSFET. MOSFET gate driver loss is the loss generated by discharging the gate capacitor and is dissipated in driver circuits.It is proportional to frequency and is defined as:

$$P_{gate}=(Q_{HGATE}\times V_{HGS}+Q_{LGATE}\times V_{LGS})\times F_S \quad ...(17)$$

where Q_{HGATE} is the high side MOSFETs gate charge,Q_{LGATE} is the low side MOSFETs gate charge,V_{HGS} is the high side gate source voltage, and V_{LGS} is the low side gate source voltage.

This power dissipation should not exceed maximum power dissipation of the driver device.

Over Current Limit Protection

Over current protection is achieved by sensing current through the low side MOSFET. An internal current source of 40uA flows through an external resistor connected from OCP pin to SW node sets the over current protection threshold. When synchronous FET is on, the voltage at node SW is given as

$$V_{SW}=-I_L\times R_{DSON}$$

The voltage at pin OCP is given as

$$I_{OCP}\times R_{OCP}+V_{SW}$$

When the voltage is below zero, the over current occurs as shown in figure 18.

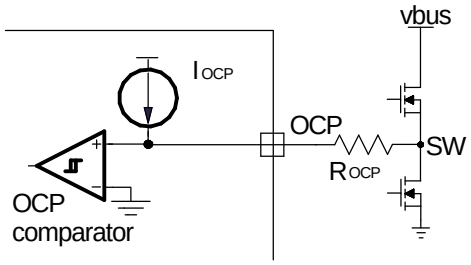


Figure 18 - Over Current Protection

The over current limit can be set by the following equation:

$$I_{SET}=\frac{I_{OCP}\times R_{OCP}}{K\times R_{DSON}}$$

If MOSFET R_{DSON}=6.5mΩ, the worst case thermal consideration K=1.5 and the current limit is set at 15A, then

$$R_{OCP}=\frac{I_{SET}\times K\times R_{DSON}}{I_{OCP}}=\frac{15A\times 1.5\times 6.5m\Omega}{40uA}=3.75k\Omega$$

Choose R_{OCP}=3.74kΩ.

Layout Considerations

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

There are two sets of components considered in the layout which are power components and small signal components. Power components usually consist of input capacitors, high-side MOSFET, low-side MOSFET, inductor and output capacitors. A noisy environment is generated by the power components due to the switching power. Small signal components are connected to sensitive pins or nodes. A multilayer layout which includes power plane, ground plane and signal plane is recommended .

Layout guidelines:

1. First put all the power components in the top layer connected by wide, copper filled areas. The input capacitor, inductor, output capacitor and the MOSFETs should be close to each other as possible. This helps to

reduce the EMI radiated by the power loop due to the high switching currents through them.

2. Low ESR capacitor which can handle input RMS ripple current and a high frequency decoupling ceramic cap which usually is 1uF need to be practically touching the drain pin of the upper MOSFET, a plane connection is a must.

3. The output capacitors should be placed as close as to the load as possible and plane connection is required.

4. Drain of the low-side MOSFET and source of the high-side MOSFET need to be connected thru a plane ans as close as possible. A snubber nedds to be placed as close to this junction as possible.

5. Source of the lower MOSFET needs to be connected to the GND plane with multiple vias. One is not enough. This is very important. The same applies to the output capacitors and input capacitors.

6. Hdrv and Ldrv pins should be as close to MOSFET gate as possible. The gate traces should be wide and short. A place for gate drv resistors is needed to fine tune noise if needed.

7. Vcc capacitor, BST capacitor or any other bypassing capacitor needs to be placed first around the IC and as close as possible. The capacitor on comp to GND or comp back to FB needs to be place as close to the pin as well as resistor divider.

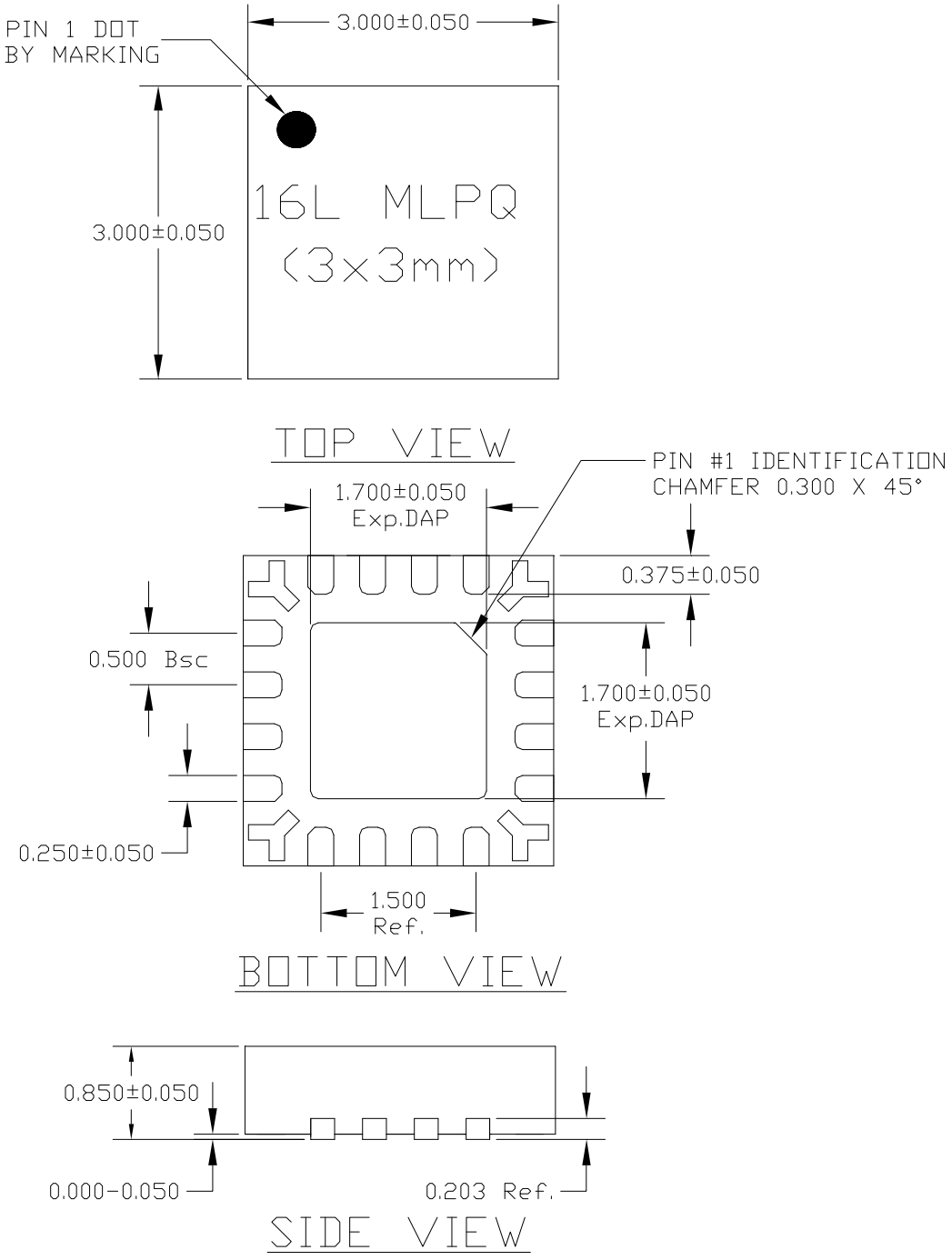
8. The output sense line which is sensing output back to the resistor divider should not go through high frequency signals.

9. All GNDs need to go directly thru via to GND plane.

10. The feedback part of the system should be kept away from the inductor and other noise sources, and be placed close to the IC.

11. In multilayer PCB, separate power ground and analog ground. These two grounds must be connected together on the PC board layout at a single point. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function.

MLPQ 16 PIN 3 x 3 PACKAGE OUTLINE DIMENSIONS



NOTE: ALL DIMENSIONS ARE DISPLAYED IN MILLIMETERS.

Microsemi
Analog Mixed Signal Group
11861 Western Avenue, Garden Grove, CA. 92841, 800-877-6458, 714-898-8121, Fax: 714-893-2570