19-1010; Rev 0; 10/07

EVALUATION KIT AVAILABLE

Low-Jitter, Precision Clock Generator with Three Outputs

General Description

The MAX3625 is a low-jitter precision clock generator optimized for networking applications. The device integrates a crystal oscillator and a phase-locked loop (PLL) clock multiplier to generate high-frequency clock outputs for Ethernet, 10G Fibre Channel, and other networking applications.

Maxim's proprietary PLL design features ultra-low jitter and excellent power-supply noise rejection, minimizing design risk for network equipment.

The MAX3625 has three LVPECL outputs. Selectable output dividers and a selectable feedback divider allow a range of output frequencies.

Features

- ♦ **Crystal Oscillator Interface: 24.8MHz to 27MHz**
- ♦ **CMOS Input: Up to 320MHz**
- ♦ **Output Frequencies**
  - **Ethernet: 125MHz, 156.25MHz, 312.5MHz**
  - **10G Fibre Channel: 159.375MHz, 318.75MHz**
- ♦ **Low Jitter**
  - **0.14ps$_{RMS}$ (1.875MHz to 20MHz)**
  - **0.38ps$_{RMS}$ (12kHz to 20MHz)**
- ♦ **Excellent Power-Supply Noise Rejection**
- ♦ **No External Loop Filter Capacitor Required**

Applications

Ethernet Networking Equipment

Fibre Channel Storage Area Network

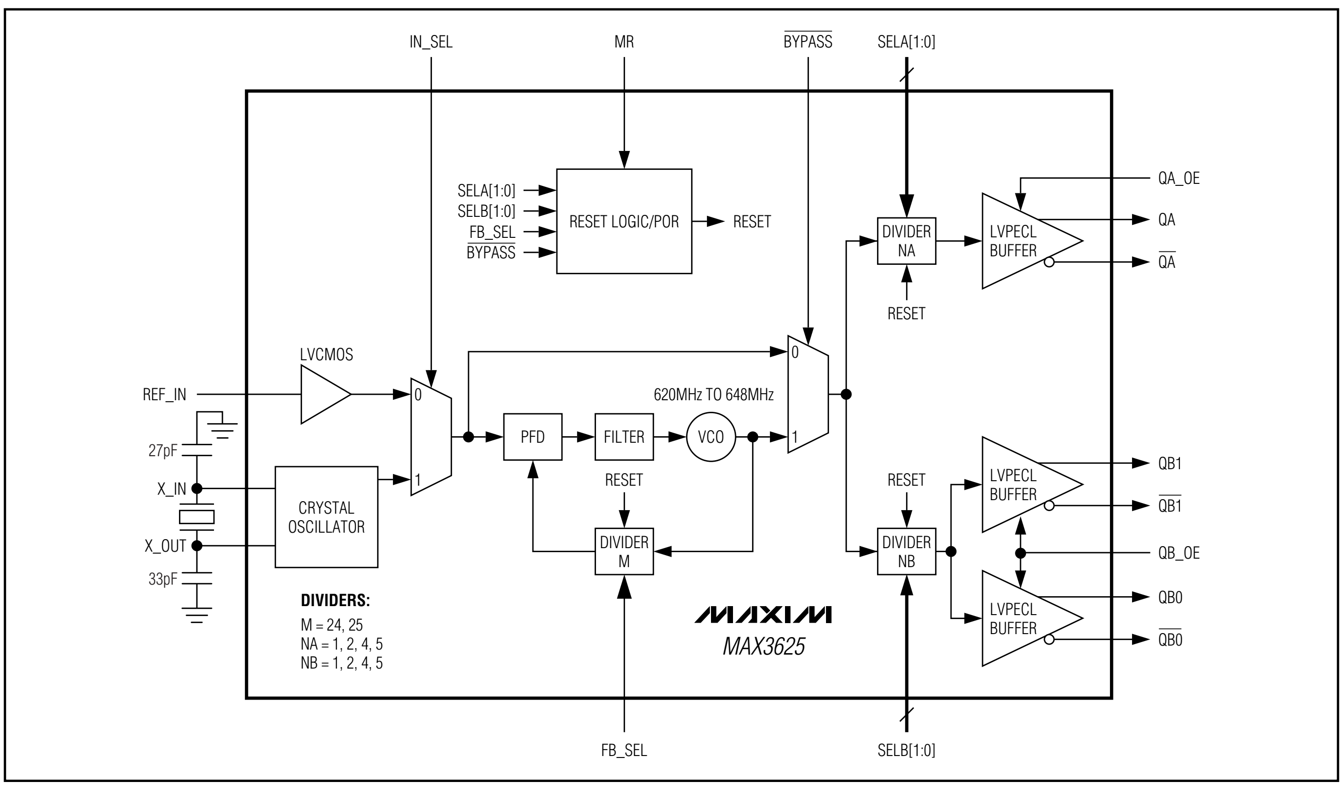
Pin Configuration and Typical Application Circuit appear at end of data sheet.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3625CUG+	0°C to +70°C	24 TSSOP	U24-1

+Denotes a lead-free package.

Block Diagram



Low-Jitter, Precision Clock Generator with Three Outputs

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range V_{CC}, V_{CCA},
V_{CCO_A}, V_{CCO_B} ....-0.3V to +4.0V
Voltage Range at REF_IN, IN_SEL,
FB_SEL, SELA[1:0], SELB[1:0],
QA_OE, QB_OE, MR, $\overline{\text{BYPASS}}$ ....-0.3V to (V_{CC} + 0.3V)
Voltage Range at X_IN Pin ....-0.3V to +1.2V
Voltage Range at X_OUT Pin ....-0.3V to (V_{CC} - 0.6V)
Current into QA, $\overline{\text{QA}}$, QB0, $\overline{\text{QB0}}$, QB1, $\overline{\text{QB1}}$ ....-56mA
Continuous Power Dissipation (T_A = +70°C)
24-Pin TSSOP (derate 13.9mW/°C above +70°C) 1111mW
Operating Junction Temperature Range...........-55°C to +150°C
Storage Temperature Range ....-65°C to +160°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Current (Note 3)	I_{CC}	IN_SEL = high		72	98	mA
		IN_SEL = low		74		
CONTROL INPUT CHARACTERISTICS (SELA[1:0], SELB[1:0], FB_SEL, IN_SEL, QA_OE, QB_OE, MR, $\overline{\text{BYPASS}}$ Pins)						
Input Capacitance	C_{IN}			2		pF
Input Pulldown Resistor	$R_{PULLDOWN}$	Pins MR, FB_SEL		75		kΩ
Input Logic Bias Resistor	R_{BIAS}	Pins SELA[1:0], SELB[1:0]		50		kΩ
Input Pullup Resistor	R_{PULLUP}	Pins QA_OE, QB_OE, IN_SEL, $\overline{\text{BYPASS}}$		75		kΩ
LVPECL OUTPUTS (QA, $\overline{\text{QA}}$, QB0, $\overline{\text{QB0}}$, QB1, $\overline{\text{QB1}}$ Pins)						
Output High Voltage	V_{OH}		V_{CC} - 1.13	V_{CC} - 0.98	V_{CC} - 0.83	V
Output Low Voltage	V_{OL}		V_{CC} - 1.85	V_{CC} - 1.7	V_{CC} - 1.55	V
Peak-to-Peak Output-Voltage Swing (Single-Ended)		(Note 2)	0.6	0.72	0.9	V_{P-P}
Clock Output Rise/Fall Time		20% to 80% (Note 2)	200	350	600	ps
Output Duty-Cycle Distortion		PLL enabled	48	50	52	%
		PLL bypassed (Note 4)	45	50	55	
LVCMOS/LVTTL INPUTS (SELA[1:0], SELB[1:0], FB_SEL, IN_SEL, QA_OE, QB_OE, MR, $\overline{\text{BYPASS}}$ Pins)						
Input-Voltage High	V_{IH}		2.0			V
Input-Voltage Low	V_{IL}				0.8	V
Input High Current	I_{IH}	V_{IN} = V_{CC}			80	µA
Input Low Current	I_{IL}	V_{IN} = 0V	-80			µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REF_IN SPECIFICATIONS (Input DC- or AC-Coupled)						
Reference Clock Frequency		PLL enabled	24.8		27.0	MHz
		PLL bypassed			320	
Input-Voltage High	V_{IH}		2.0			V
Input-Voltage Low	V_{IL}				0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{CC}$			240	µA
Input Low Current	I_{IL}	V_{IN} = 0V	-240			µA
Reference Clock Duty Cycle		PLL enabled	30		70	%
Input Capacitance				2.5		pF
CLOCK OUTPUT AC SPECIFICATIONS						
VCO Frequency Range			620		648	MHz
Random Jitter (Note 6)	RJ_{RMS}	12kHz to 20MHz		0.36	1.0	ps_{RMS}
		1.875MHz to 20MHz		0.14		
Deterministic Jitter Induced by Power-Supply Noise		(Notes 6, 7, and 8)		5.6		ps_{P-P}
Spurs Induced by Power-Supply Noise		(Notes 6, 8, and 9)		-54		dBc
Nonharmonic and Subharmonic Spurs				-70		dBc
Output Skew		Between any output pair		5		ps
Clock Output SSB Phase Noise at 125MHz (Note 10)		f = 1kHz		-124		dBc/Hz
		f = 10kHz		-127		
		f = 100kHz		-131		
		f = 1MHz		-145		
		f > 10MHz		-153		

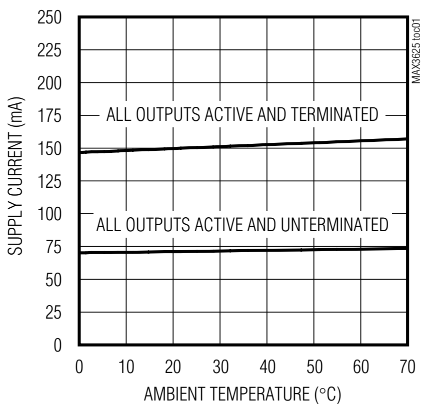
Note 1: A series resistor of up to 10.5Ω is allowed between V_{CC} and V_{CCA} for filtering supply noise when system power-supply tolerance is V_{CC} = 3.3V ±5%. See Figure 1.
Note 2: LVPECL outputs guaranteed up to 320MHz.
Note 3: All outputs enabled and unloaded.
Note 4: Measured with a crystal (see Table 4) or an AC-coupled, 50% duty-cycle signal on REF_IN.
Note 5: Measured using setup shown in Figure 1.
Note 6: Measured with crystal source, see Table 4.
Note 7: Measured with Agilent DSO81304A 40GS/s real-time oscilloscope.
Note 8: Measured with 40mV_{P-P}, 100kHz sinusoidal signal on the supply.
Note 9: Measured at 156.25MHz output.
Note 10: Measured with 25MHz crystal or 25MHz reference clock at REF_IN with a slew rate of 0.5V/ns or greater.

Low-Jitter, Precision Clock Generator with Three Outputs

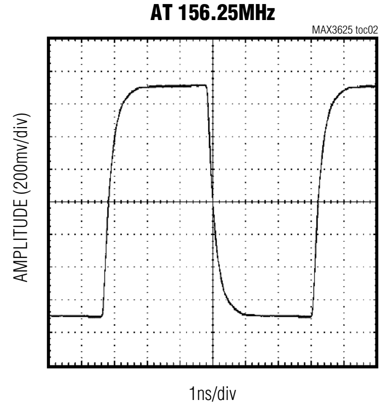
Typical Operating Characteristics

(Typical values are at V_{CC} = +3.3V, T_A = +25°C, crystal frequency = 25MHz.)

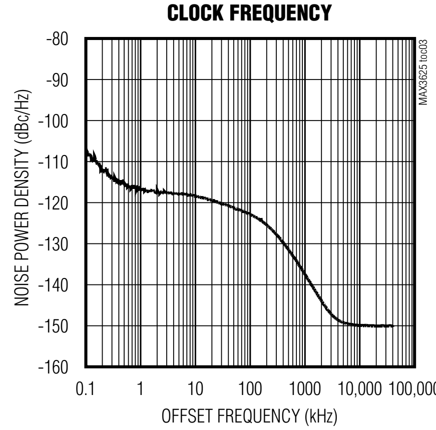
SUPPLY CURRENT vs. TEMPERATURE



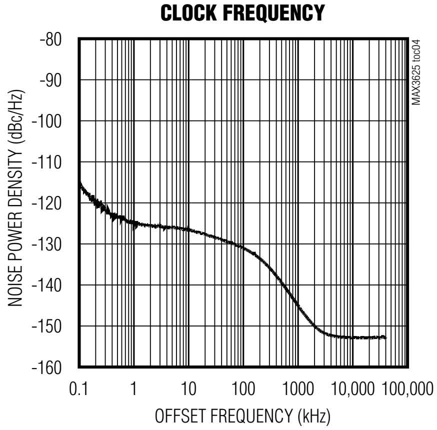
DIFFERENTIAL OUTPUT WAVEFORM AT 156.25MHz



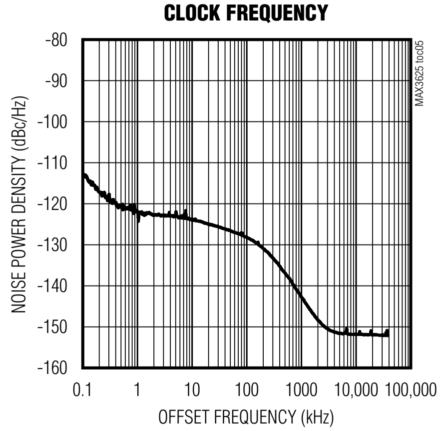
PHASE NOISE AT 312.5MHz CLOCK FREQUENCY



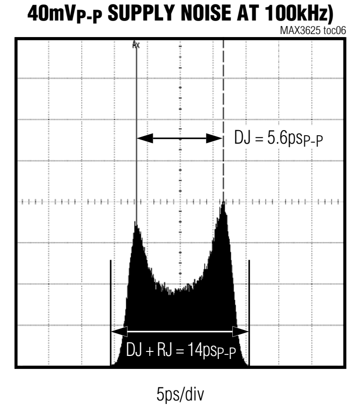
PHASE NOISE AT 125MHz CLOCK FREQUENCY



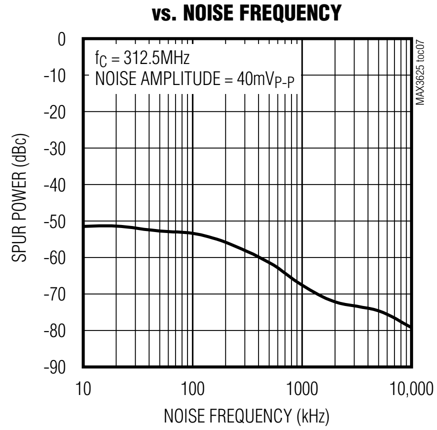
PHASE NOISE AT 156.25MHz CLOCK FREQUENCY



JITTER HISTOGRAM (312.5MHz OUTPUT, 40mV$_{P-P}$ SUPPLY NOISE AT 100kHz)



SPURS INDUCED BY POWER-SUPPLY NOISE vs. NOISE FREQUENCY



Pin Description

PIN	NAME	FUNCTION
1, 24	SELB0, SELB1	LVCMOS/LVTTL Inputs. Control NB divider setting. Has 50kΩ input impedance. See Table 2 for more information.
2	$\overline{\text{BYPASS}}$	LVCMOS/LVTTL Input (Active Low). Connect low to bypass the internal PLL. Connect high or leave open for normal operation. When in bypass mode the output dividers are set to divide by 1. Has internal 75kΩ pullup to V_{CC}.
3	MR	LVCMOS/LVTTL Input. Master reset input. Pulse high for > 1µs to reset all dividers. Has internal 75kΩ pulldown to GND. Not required for normal operation.
4	V_{CCO_A}	Power Supply for QA Clock Output. Connect to +3.3V.
5	QA	Noninverting Clock Output, LVPECL
6	$\overline{\text{QA}}$	Inverting Clock Output, LVPECL
7	QB_OE	LVCMOS/LVTTL Input. Enables/disables QB clock outputs. Connect pin high or leave open to enable LVPECL clock outputs QB0 and QB1. Connect low to set QB0 and QB1 to a logic 0. Has internal 75kΩ pullup to V_{CC}.
8	QA_OE	LVCMOS/LVTTL Input. Enables/disables the QA clock output. Connect this pin high or leave open to enable the LVPECL clock output QA. Connect low to set QA to a logic 0. Has internal 75kΩ pullup to V_{CC}.
9	FB_SEL	LVCMOS/LVTTL Input. Controls M divider setting. See Table 3 for more information. Has internal 75kΩ pulldown to GND.
10	V_{CCA}	Analog Power Supply for the VCO. Connect to +3.3V. For additional power-supply noise filtering, this pin can connect to V_{CC} through 10.5Ω as shown in Figure 1 (requires V_{CC} = 3.3V ±5%).
11	V_{CC}	Core Power Supply. Connect to +3.3V.
12, 13	SELA0, SELA1	LVCMOS/LVTTL Inputs. Control NA divider setting. See Table 2 for more information. 50kΩ input impedance.
14	GND	Supply Ground
15	X_OUT	Crystal Oscillator Output
16	X_IN	Crystal Oscillator Input
17	REF_IN	LVCMOS Reference Clock Input. Self-biased to allow AC- or DC-coupling.
18	IN_SEL	LVCMOS/LVTTL Input. Connect high or leave open to use a crystal. Connect low to use REF_IN. Has internal 75kΩ pullup to V_{CC}.
19	$\overline{\text{QB1}}$	LVPECL, Inverting Clock Output
20	QB1	LVPECL, Noninverting Clock Output
21	$\overline{\text{QB0}}$	LVPECL, Inverting Clock Output
22	QB0	LVPECL, Noninverting Clock Output
23	V_{CCO_B}	Power Supply for QB0 and QB1 Clock Output. Connect to +3.3V.

Detailed Description

The MAX3625 is a low-jitter clock generator designed to operate at Ethernet and Fibre Channel frequencies. It consists of an on-chip crystal oscillator, PLL, programmable dividers, and LVPECL output buffers. Using a low-frequency clock (crystal or CMOS input) as a reference, the internal PLL generates a high-frequency output clock with excellent jitter performance.

Crystal Oscillator

An integrated oscillator provides the low-frequency reference clock for the PLL. This oscillator requires an external crystal connected between X_IN and X_OUT. Crystal frequency is 24.8MHz to 27MHz.

REF_IN Buffer

An LVCMOS-compatible clock source can be connected to REF_IN to serve as the reference clock.

The LVCMOS REF_IN buffer is internally biased to the threshold voltage (1.4V typ) to allow AC- or DC-coupling, and is designed to operate up to 320MHz.

PLL

The PLL takes the signal from the crystal oscillator or reference clock input and synthesizes a low-jitter, high-frequency clock. The PLL contains a phase-frequency detector (PFD), a lowpass filter, and a voltage-controlled oscillator (VCO) with a 620MHz to 648MHz operating range. The VCO is connected to the PFD input through a feedback divider. See Table 3 for divider values. The PFD compares the reference frequency to the divided-down VCO output (f_{VCO}/M) and generates a control signal that keeps the VCO locked to the reference clock. The high-frequency VCO output clock is sent to the output dividers. To minimize noise-induced jitter, the VCO supply (V_{CCA}) is isolated from the core logic and output buffer supplies.

Output Dividers

The output dividers are programmable to allow a range of output frequencies. See Table 2 for the divider input settings. The output dividers are automatically set to divide by 1 when the MAX3625 is in bypass mode ($\overline{\text{BYPASS}}$ = 0).

LVPECL Drivers

The high-frequency outputs—QA, QB0, and QB1—are differential PECL buffers designed to drive transmission lines terminated with 50Ω to V_{CC} - 2.0V. The maximum operating frequency is specified up to 320MHz. The outputs can be disabled, if not used. The outputs go to a logic 0 when disabled.

Reset Logic/POR

During power-on, a power-on reset (POR) signal is generated to synchronize all dividers. An external master reset (MR) signal is not required.

Applications Information

Power-Supply Filtering

The MAX3625 is a mixed analog/digital IC. The PLL contains analog circuitry susceptible to random noise. In addition to excellent on-chip power-supply noise rejection, the MAX3625 provides a separate power-supply pin, V_{CCA}, for the VCO circuitry. Figure 1 illustrates the recommended power-supply filter network for V_{CCA}. The purpose of this design technique is to ensure a clean power supply to the VCO circuitry and to improve the overall immunity to power-supply noise. This network requires that the power supply is +3.3V ±5%. Decoupling capacitors should be used on all supply pins for best performance.

Output Divider Configuration

Table 2 shows the input settings required to set the output dividers. Note that when the MAX3625 is in bypass mode ($\overline{\text{BYPASS}}$ set low), the output dividers are automatically set to divide by 1.

PLL Divider Configuration

Table 3 shows the input settings required to set the PLL feedback divider.

Crystal Selection

The crystal oscillator is designed to drive a fundamental mode, AT-cut crystal resonator. See Table 4 for recommended crystal specifications. See Figure 3 for external capacitance connection.

Crystal Input Layout

The crystal, trace, and two external capacitors should be placed on the board as close as possible to the MAX3625's X_IN and X_OUT pins to reduce crosstalk of active signals into the oscillator. The example layout shown in Figure 3 gives approximately 3pF of trace plus footprint capacitance per side of the crystal. The dielectric material is FR-4 and dielectric thickness of the reference board is 15 mils. Using a 25MHz crystal and the capacitor values of C10 = 27pF and C9 = 33pF, the measured output frequency accuracy is -14ppm at +25°C ambient temperature.

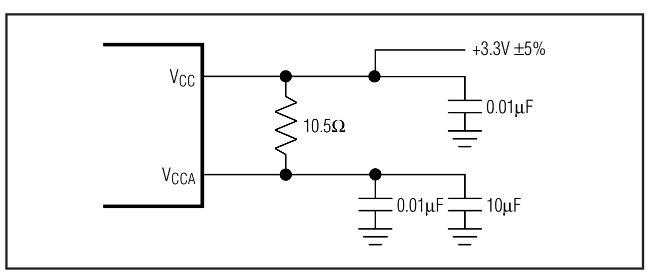


Figure 1. Analog Supply Filtering

Table 1. Output Frequency Determination Chart

CRYSTAL OR CMOS INPUT FREQUENCY (MHz)	FEEDBACK DIVIDER, M	VCO FREQUENCY (MHz)	OUTPUT DIVIDER, NA AND NB	OUTPUT FREQUENCY (MHz)	APPLICATIONS
25	25	625	2	312.5	Ethernet
			4	156.25	
			5	125	
25.78125	25	644.53125	4	161.132812	10Gbps Ethernet
26.04166	24	625	2	312.5	Ethernet
			4	156.25	
			5	125	
26.5625	24	637.5	2	318.75	10G Fibre Channel
			4	159.375	

Table 2. Output Divider Configuration Chart

INPUT		NA/NB DIVIDER
SELA1/SELB1	SELA0/SELB0	
0	0	/ 1*
0	1	/ 2*
1	0	/ 4
1	1	/ 5

*Maximum guaranteed output frequency is 320MHz.

Table 3. PLL Divider Configuration Chart

FB_SEL INPUT	M DIVIDER
0	/ 25
1	/ 24

Table 4. Crystal Selection Parameters

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Crystal Oscillation	f_{OSC}	24.8		27	MHz
Shunt Capacitance	C_O		2.0	7.0	pF
Load Capacitance	C_L		18		pF
Equivalent Series Resistance (ESR)	R_S			50	Ω
Maximum Crystal Drive Level				300	μW

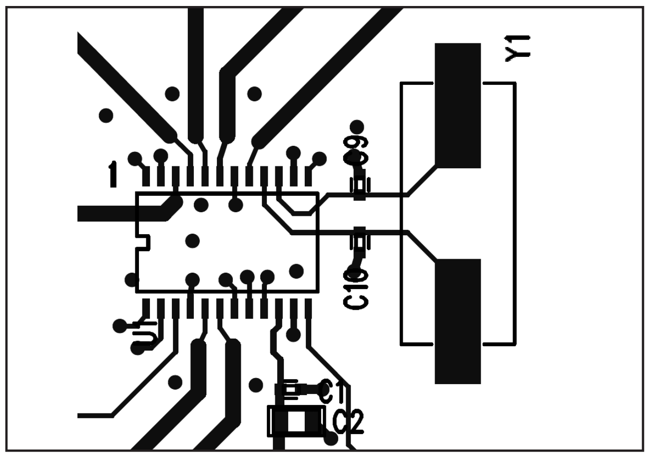


Figure 2. Crystal Layout

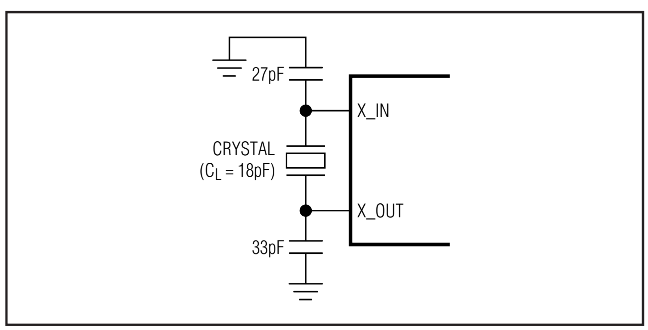


Figure 3. Crystal, Capacitors Connection

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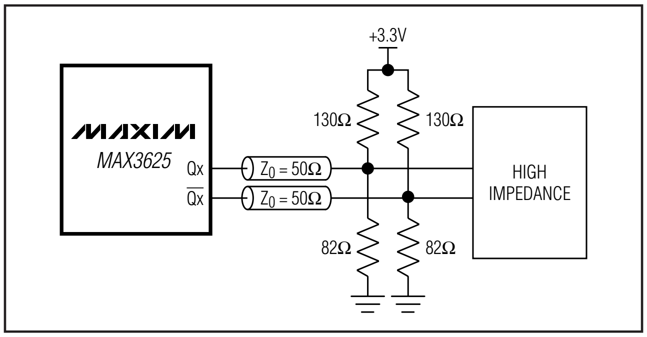


Figure 4. Thevenin Equivalent of Standard PECL Termination

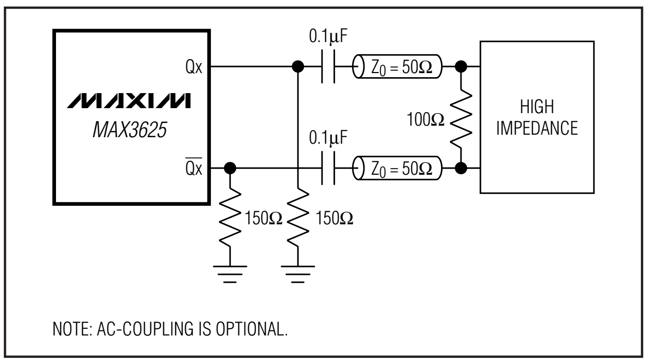


Figure 5. AC-Coupled PECL Termination

Interfacing with LVPECL Outputs

The equivalent LVPECL output circuit is given in Figure 7. These outputs are designed to drive a pair of 50Ω transmission lines terminated with 50Ω to $V_{TT} = V_{CC}$ - 2V. If a separate termination voltage (V_{TT}) is not available, other terminations methods can be used such as shown in Figures 4 and 5. Unused outputs should be disabled and may be left open. For more information on LVPECL terminations and how to interface with other logic families, refer to Maxim Application Note *HFAN-01.0: Introduction to LVDS, PECL, and CML*.

Interface Models

Figures 6 and 7 show examples of interface models.

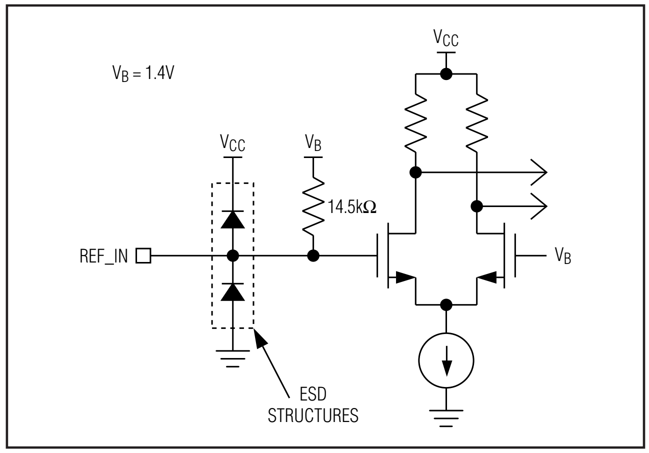


Figure 6. Simplified REF_IN Pin Circuit Schematic

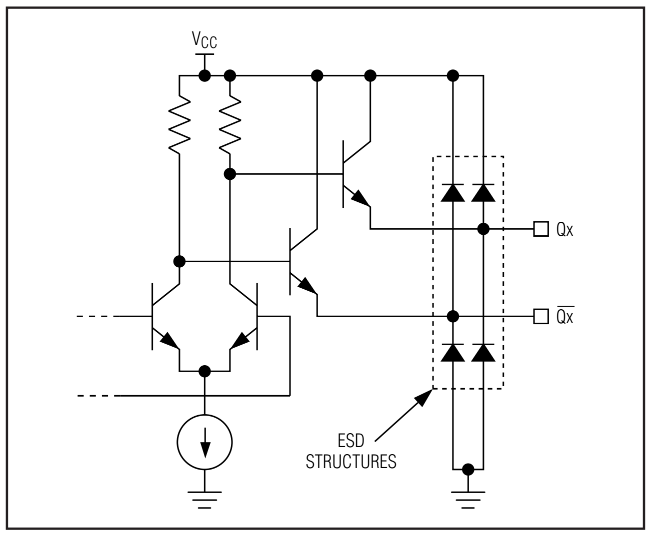


Figure 7. Simplified LVPECL Output Circuit Schematic

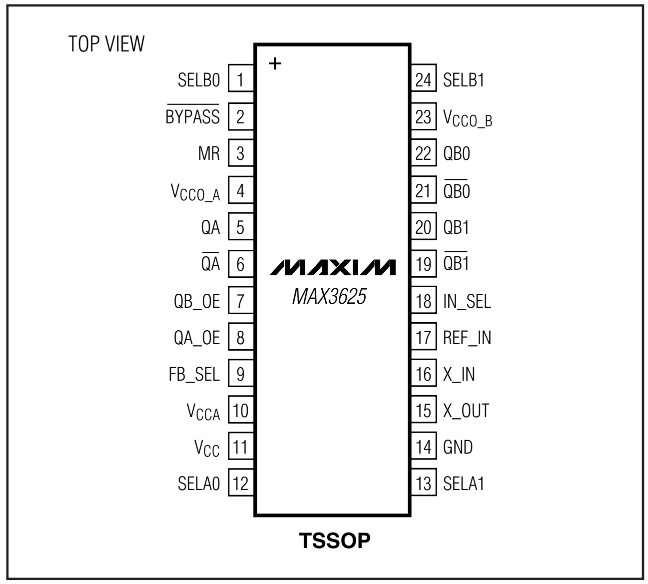
Layout Considerations

The inputs and outputs are critical paths for the MAX3625, and care should be taken to minimize discontinuities on these transmission lines. Here are some suggestions for maximizing the MAX3625's performance:

- An uninterrupted ground plane should be positioned beneath the clock I/Os.
- Supply and ground pin vias should be placed close to the IC and the input/output interfaces to allow a return current path to the MAX3625 and the receive devices.
- Supply decoupling capacitors should be placed close to the MAX3625 supply pins.
- Maintain 100Ω differential (or 50Ω single-ended) transmission line impedance out of the MAX3625.
- Use good high-frequency layout techniques and multilayer boards with an uninterrupted ground plane to minimize EMI and crosstalk.

Refer to the MAX3625 Evaluation Kit for more information.

Pin Configuration



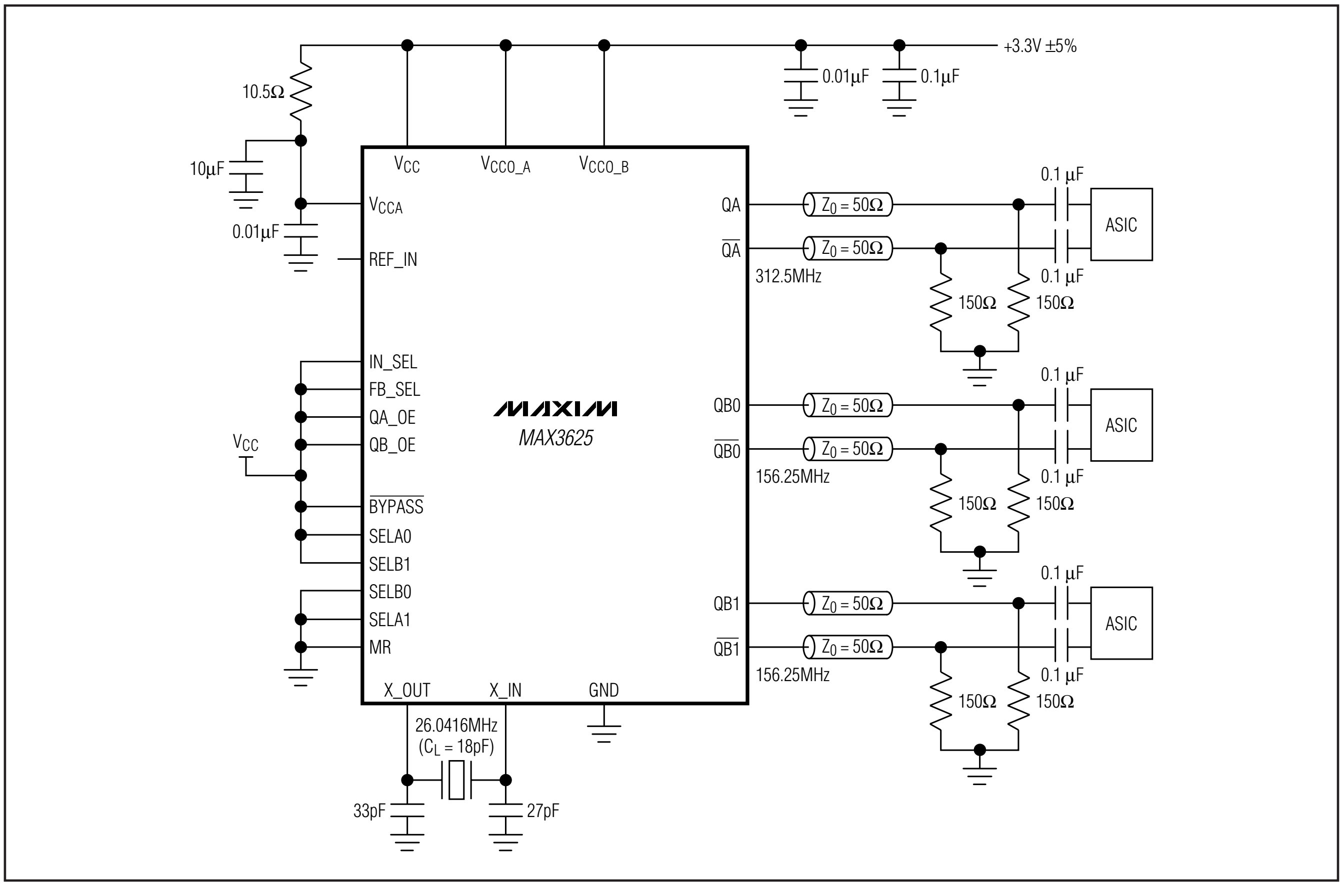
Chip Information

TRANSISTOR COUNT: 10,670

PROCESS: BiCMOS

Low-Jitter, Precision Clock Generator with Three Outputs

Typical Application Circuit



Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	DOCUMENT NO.
24 TSSOP	21-0066