
SmartFusion2 SoC FPGA Evaluation Kit

User Guide



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1 –Introduction

The SmartFusion[®]2 system-on-chip (SoC) field programmable gate array (FPGA) Evaluation Kit (M2S-EVAL-KIT) is restriction of hazardous substances (RoHS) compliant and enables the designer to develop applications that involve one or more of the following:

- Motor control
- System management
- Industrial automation
- High-speed serial I/O applications like peripheral component interconnect express (PCIe), serial gigabit media independent interface (SGMII), and user customizable serial interfaces

Kit Contents

Table 1 lists the contents of the M2S-EVAL-KIT.

Table 1 Kit Contents

Quantity	Description
1	SmartFusion2 SoC FPGA 25K LE M2S025T-1FGG484
1	12 V/2 A Wall-Mounted Power Supply
1	FlashPro4 JTAG programmer
1	USB 2.0 A-male to mini-B Y-cable for UART/power interface (up to 1 A) to PC
1	Quickstart Guide
1	Libero SoC Gold Software License
1	PCIe Control Plane Demo Design
<i>Note: The M2S-Eval-KIT is RoHS compliant.</i>	

SmartFusion2 SoC FPGA Evaluation Kit Web Resources

M2S-EVAL-KIT web resources are available at:

www.microsemi.com/products/fpga-soc/design-resources/dev-kits/SmartFusion2/smartfusion2-evaluation-kit#overview

Board Description

The M2S-EVAL-KIT Kit offers a full-featured Evaluation Board for SmartFusion2 SoC FPGAs. This kit inherently integrates the following on a single chip:

- Reliable flash-based FPGA fabric
- A 166 MHz ARM[®] Cortex[™]-M3 processor
- Advanced security processing accelerators
- Digital signal processing (DSP) blocks
- Static random-access memory (SRAM)
- Embedded nonvolatile memory (eNVM)
- Industry-required high-performance communication interfaces

The board has numerous interfaces including an RJ45 for 10/100/1000 Ethernet, one full-duplex serializer and deserializer (SERDES) lane through sub miniature version A (SMA) connectors, a 64-bit GPIO Header, and various connectors for serial peripheral interface (SPI) support.

The SmartFusion2 memory management system is supported by 512 Mb of on board mobile low-power double data rate (LPDDR) SDRAM memory and 64 Mb SPI flash. The SERDES block can be accessed through the PCIe edge connector or high-speed sense multiple access (SMA) connectors.

- The board supports the M2S025T device in an FGG484 package
- The board is eight layers PCB and manufactured with FR4 dielectric material.

Block Diagram

Figure 1 shows the M2S-EVAL-KIT block diagram:

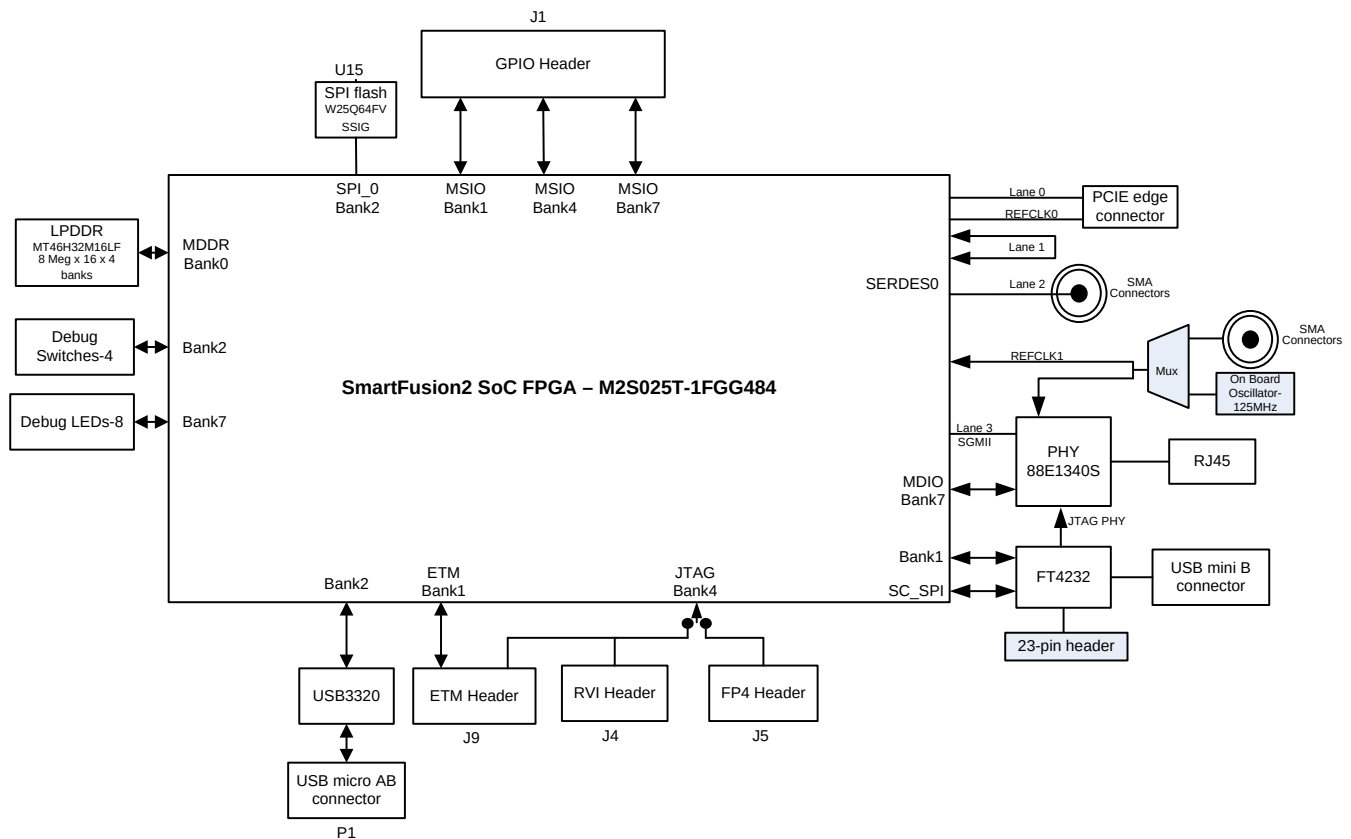


Figure 1 SmartFusion2 SoC FPGA Evaluation Kit Block Diagram

Board Overview

Figure 2 shows an overview of the M2S-EVAL-KIT features.

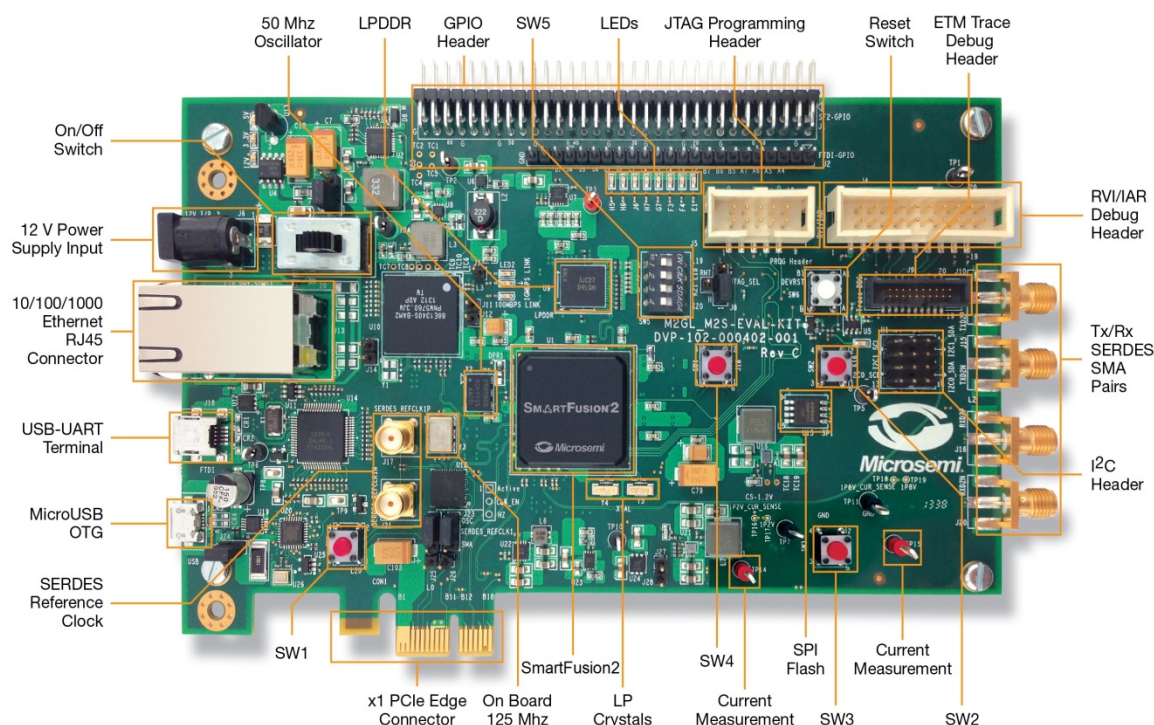


Figure 2 SmartFusion2 SoC FPGA Evaluation Kit Board Overview

Note: Microsemi® recommends SMA Male to SMA Male Precision Cable 12 Inch length using PE-SR405FLJ Coax, RoHS to use with SmartFusion2 Evaluation Kit. For more information, refer to www.pasternack.com/sma-male-sma-male-pe-sr405flj-cable-assembly-pe39429-12-p.aspx

I/O Voltage Rails

Table 2 lists the bank I/Os with voltage rails.

Table 2 I/O Voltage Rails

SmartFusion2 Bank	I/O Rail	Voltage
Bank0	VDDI0	1.8 V
Bank1	VDDI1	3.3 V
Bank2	VDDI2	3.3 V
Bank3	VDDI3	3.3 V
Bank4	VDDI4	3.3 V
Bank5	VDDI5	2.5 V
Bank6	VDDI6	2.5 V
Bank7	VDDI7	3.3 V

Table 3 describes the M2S -EVAL-KIT components.

Table 3 SmartFusion2 SoC FPGA Evaluation Kit Board Components

Name	Description
M2S025T-1FGG484	Microsemi SmartFusion2 SoC FPGA
Mobile Low-Power DDR SDRAM	512 Mb (MT46H32M16LF – 8 Meg x 16 x 4 banks) for storing the data bits.
SPI flash	64 Mb SPI flash Winbond electronics W25Q64FVSSIG connected to SPI port 0 of the SmartFusion2 FPGA high performance memory system (HPMS).
Ethernet	RJ45 connector (Ethernet jack with magnetic) interfacing with Marvell 10/100/1000 BASE-T PHY chip 88E1340S in serial gigabit media independent interface (SGMII) mode, interfacing with the Ethernet port of the SmartFusion2 FPGA (on-chip MAC and external PHY).
RVI header	RVI header for application programming and debugging from Keil ULINK or IAR J-Link.
FP4 header	FlashPro4 programming header for SmartFusion2 programming and debugging with Microsemi tools.
Future Technology Devices International (FTDI) programmer	FTDI programmer interface (J18) to program the external SPI flash.
Embedded trace macro (ETM) cell header	ETM header for debugging.
GPIO header	General purpose input/output(GPIO) header for multi standard I/O(MSIO) signals to be routed.
PCIe edge connector	PCI Express edge connector with one lane
Dual in-line package (DIP) switch	Debug switch for user application.
Light-emitting diodes (LEDs)	Eight active low LEDs that are connected to some of the user I/Os for debug. Three active high LEDs that are used for power supply indication.
Push–button reset	Push-button system reset for SmartFusion2 system.
Push–button switches	Four push-button switches for test and navigation.
USB interface	USB micro AB connector, interfacing with the high-speed USB2.0 ULPI transceiver chip USB3320, interfacing with FPGA pins of the SmartFusion2 HPMS.
OSC-125	125 MHz clock oscillator(differential output)
OSC-50	50 MHz clock oscillator
OSC-32	32.768 KHz low-power oscillator

2 – Installation and Settings

Software Installation

Download and install the latest release of Microsemi Libero[®] System-on-Chip (SoC) software v11.1 or later, from the Microsemi website and register for a free Gold license. For instructions on how to install Libero and SoftConsole, refer to the [Libero Installation and Licensing Guide](#) available on the Microsemi website.

Refer to the [Installing IP Cores and Drivers User Guide](#) to download and install Microsemi DirectCores, SGCores, and driver firmware cores. These must be localized on the PC where Microsemi Libero is installed while designing with Microsemi FPGAs.

Hardware Installation

The FlashPro4 programmer can be used to program the M2S-EVAL-KIT board.

Jumpers, Switches, LEDs, and DIP Switch Settings

The recommended default jumpers, switches, LEDs, and DIP switch settings are defined in [Table 4](#) through [Table 6](#).

- [Table 4.Jumper Settings](#)
- [Table 5.LEDs](#)
- [Table 6.Test Points](#)

Connect the jumpers using the default settings to enable the pre-programmed demonstration design to function correctly. [Table 4](#) shows the jumpers along with default settings.

Note: Location of all the jumpers and test points are searchable in [Figure 18 on page 40](#) of [5– Board Components Placement](#) section.

Table 4 Jumper Settings

Jumper	Function	Default Settings
J23	Jumper to select switch-side Mux inputs of A or B to the lineside.	–
	Pin 1-2 (Input A to the line side) that is on board 125 MHz differential clock oscillator output will be routed to line side.	Closed
	Pin 2-3 (Input B to the line side) that is external clock required to source through SMA connectors to the line side.	Open
J22	Jumper to select the output enables control for the line side outputs.	–
	Pin 1-2 (Line side output enabled)	Closed
	Pin 2-3 (Line side output disabled)	Open
J24	Jumper to provide the VBUS supply to USB when using in Host mode.	Open
J8	JTAG selection jumper to select between RVI header or FP4 header for application debug.	–
	Pin 1-2 FP4 for SoftConsole/FlashPro	Closed
	Pin 2-3 RVI for Keil ULINK [™] /IAR J-Link [®]	Open
	Pin 2-4 for Toggling JTAG_SEL signal remotely using GPIO capability of FT4232 chip.	Open
J3	Jumpers to select either SW2 input or signal ENABLE_FT4232 from FT4232H chip.	–

Jumper	Function	Default Settings
	Pin 1-2 for Manual power switching using SW7 switch.	Closed
	Pin 2-3 for Remote power switch using GPIO capability of FT4232 chip.	Open

Table 5 lists the power supply and Ethernet LEDs.

Table 5 LEDs

LED	Comment
DS1 - Green	Indicates the 5 V rail.
DS2 - Green	Indicates the 3.3 V rail.
DS3 - Green	Indicates the 12 V power source.
DS5 - Green	Connected to parallel LED output port 0 (P0_LED[0]) of Marvell PHY.
DS4 - Green	Connected to parallel LED output port 0 (P0_LED[2]) of Marvell PHY.
DS6 - Green	Connected to parallel LED output port 0 (P0_LED[3]) of Marvell PHY.

Table 6 lists the USB, ground, and other test points.

Table 6 Test Points

Test Point	Description
TP8	USB switch in/out for DP signal.
TP9	USB switch in/out for DM signal.
TP1,TP2,TP4,TP5,TP6,TP7,TP10,TP11	GND
TP3	Test point for DDR_VTT
TP12	Test point to measure the voltage at TP12 with reference to GND.
TP14	1.2 V current sensing test point
TP15	1.8 V current sensing test point
TP16, TP17	Test points across current sense resistor 0.05 Ohms for 1.2 V
TP18, TP19	Test points across current sense resistor 0.05 Ohms for 1.8 V

SmartFusion2 Power Sources

All the power supply devices used in the SmartFusion2 SoC FPGA Evaluation Kit are Microsemi devices. For more information on power supply devices refer to www.microsemi.com/product-directory/ics/853-power-management

Voltage rails (12 V, 5 V, 3.3 V, 2.5 V, 1.8 V, 1.5 V, and 1.0 V) provided on the board is shown in Figure 3.

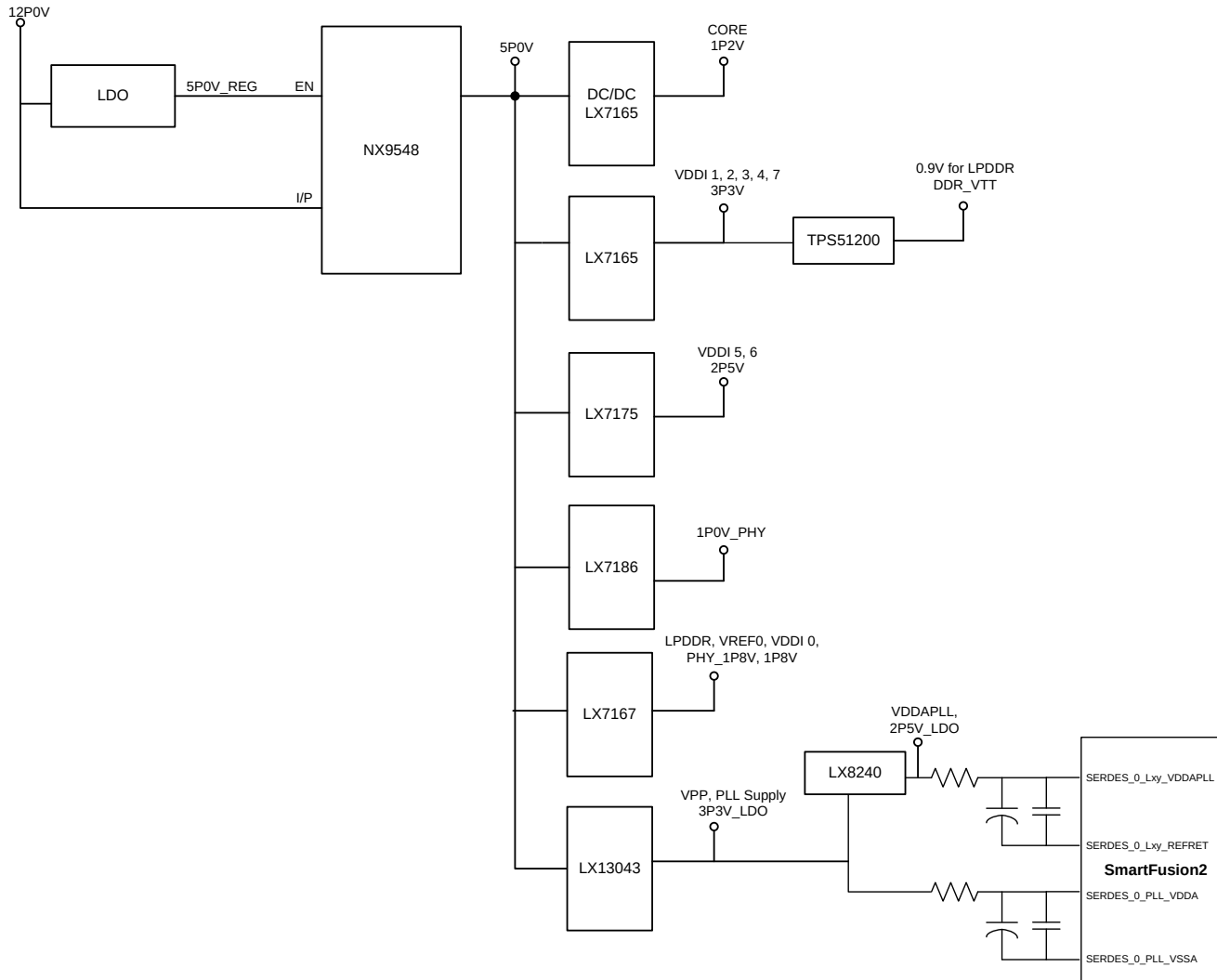


Figure 3 Voltage Rails in the SmartFusion2 SoC FPGA Evaluation Kit

Testing the Hardware

If the board is shipped directly from Microsemi, it contains a test program that determines whether or not the board works properly. If the board is found damaged, the [manufacturing test](#) can be rerun to verify the key interfaces of the board functionality.

Refer to www.microsemi.com/download/rsc/?f=%20M2S-EVAL-KIT-PP_Mfg_PF (to be released) for manufacturing test procedures.

Figure 5 shows the onboard core power measurement circuitry.

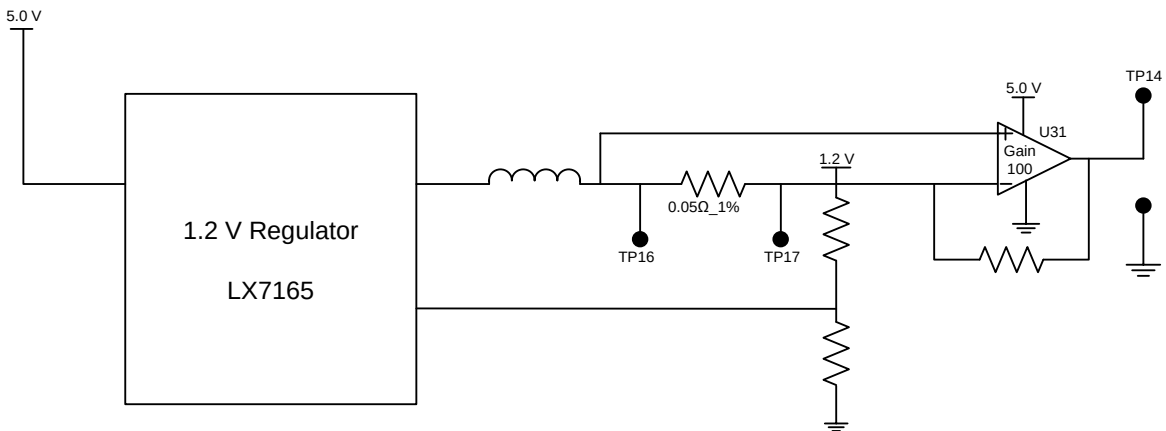


Figure 5 Core Power Measurement Circuitry

1.2 V Current Sensing for Flash*Freeze

The SmartFusion2 device consumes very low-power in Flash*Freeze mode. The voltage across the sense resistor (0.05 Ohms) needs to be measured directly using a precision digital multi-meter that can read sub milli-volts. Test points TP16 and TP17 can be used to directly measure voltage across the 1.2 V sense resistor.

To convert the voltage measured across sense resistor to power, use the following equation:

$$Power = \left(\frac{\text{voltage_measured_in_milli_volts}}{0.05} \right) * 1.2$$

1.8 V Current Sensing

For applications which require current measurement high precision Operational Amplifier circuitry (U32 with gain 100) is placed on the board to measure the output voltage at TP15 test point with reference to the ground.

1.8 V power can be measured by running the following steps:

1. Measure the output voltage (VOUT) at TP15.
2. $I = (VOUT/5)$
3. Power consumed $P = (1.8 \text{ V}) * I$

For example, when the voltage measured across TP15 as 0.5 V, then the consumed core power is 0.18 W.

Figure 6 shows the onboard 1.8 V power measurement circuitry.

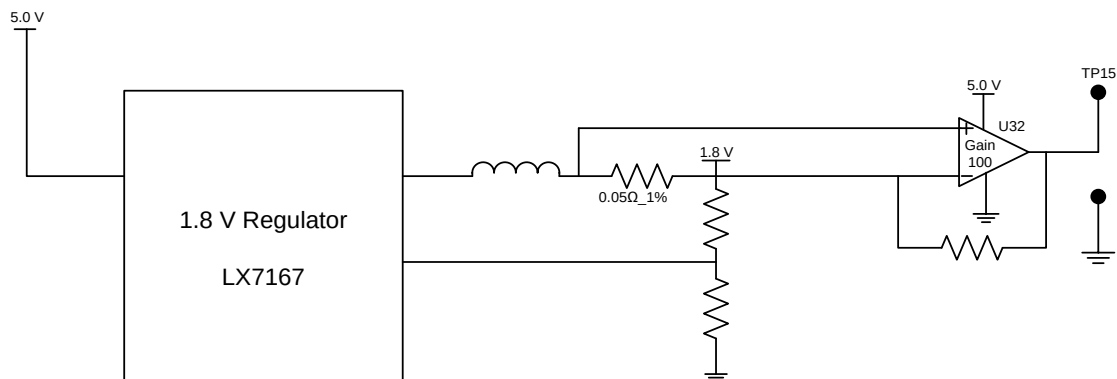


Figure 6 1.8 V Power Measurement Circuitry

Note: The measured accuracy is $\pm 10\%$.

Memory Interface

Dedicated I/Os are provided for HPMS DDR and fabric DDR for the SmartFusion2 device. Apart from the dedicated I/Os, regular I/Os can also be used to connect to other memory devices. Refer to [Figure 7](#).

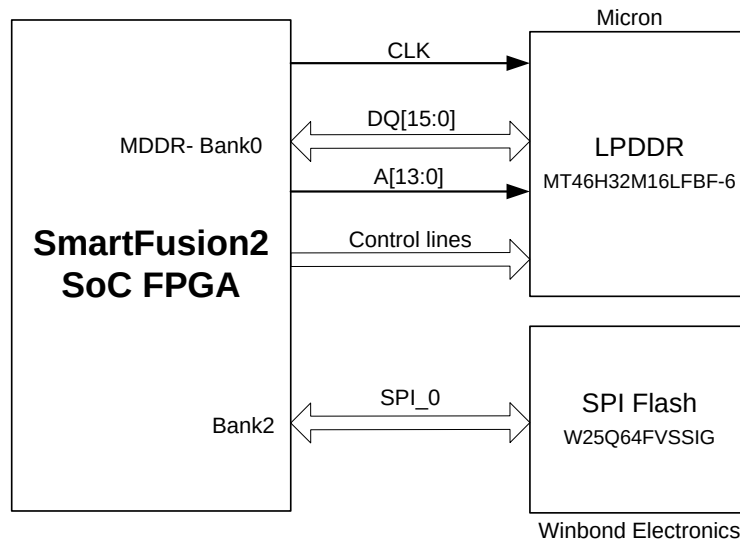


Figure 7 SmartFusion2 Memory Interface

Mobile LPDDR SDRAM

An individual chip, 512 Mb LPDDR SDRAM memory is provided as flexible volatile memory for user applications. The LPDDR interface is implemented in bank 0. The specifications of LPDDR SDRAM are listed below:

- MT46H32M16LF – 8 Meg x 16 x 4 banks
- Density: 512 Mb
- Data rate: LPDDR 16-bit at 400 Mbps = 6.4 Gbps

Note: For more information, refer to page 3 of Board Level Schematics document (provided separately).

SPI Serial Flash

The specifications of SPI Flash are listed below:

- Density: 64 Mb
- Voltage: 2.7 V - 3.6 V
- Frequency: 104 MHz
- Supports: SPI modes 0 and 3
- SmartFusion2 HPMS - SPI0 interfaced to SPI flash

Note: For more information, refer to page 8 of Board Level Schematics document (provided separately).

SERDES0 Interface

The SERDES0 is having four lanes connected as below:

1. Lane 0 is directly routed to the PCIe connector.
 - TX Pad → trace → AC Coupling→trace →via (to bottom layer)→ trace→PCIe connector pad
 - RX Pad→ trace → PCIe connector pad
2. Lane 1 is used for loopback testing. This path is routed between the Tx and Rx with a 6 inch trace and 2 vias.
 - TX Pad → via (to Bottom layer) → trace → AC Coupling→ trace → via (to top layer) → RX pad
3. Lane 2 routed to SMA connectors.
 - TX Pad → trace → AC Coupling→trace → SMA connector pad
 - RX Pad→trace→via (to bottom layer)→trace→via (to top layer)→ SMA connector Pad
4. Lane 3 is routed to Marvell PHY (88E1340S).
 - TX pad→trace→AC Coupling→trace→via→trace routed in (6th layer)→via (to top layer)→Marvel PHY pin
 - RX pad→via→trace routed in 6th layer→via (to top layer)→trace→AC Coupling→trace→Marvel PHY pin

SERDES0 reference clock 0 is routed directly from the PCIe connector to SmartFusion2 FPGA.

SERDES0 reference clock 1 is routed from the onboard 125 MHz clock oscillator and optionally routed from SMA connectors through LVDS Mux/Buffer chip.

Expected SERDES reference clock specifications:

- Voltage level: 3.3 (± 0.3)V
- Differential LVDS
 - Symmetry: 50% ($\pm 10\%$)
 - Rise/Fall Time: 1nsec Max @ 20% to 80% of supply (3.3V)
 - Output Voltage Levels: "0"=0.90 Minimum, 1.10 Typical
"1"=1.43 Typical, 1.60 Maximum
 - Differential Output Voltage: 247 mV Minimum, 454 mV Maximum

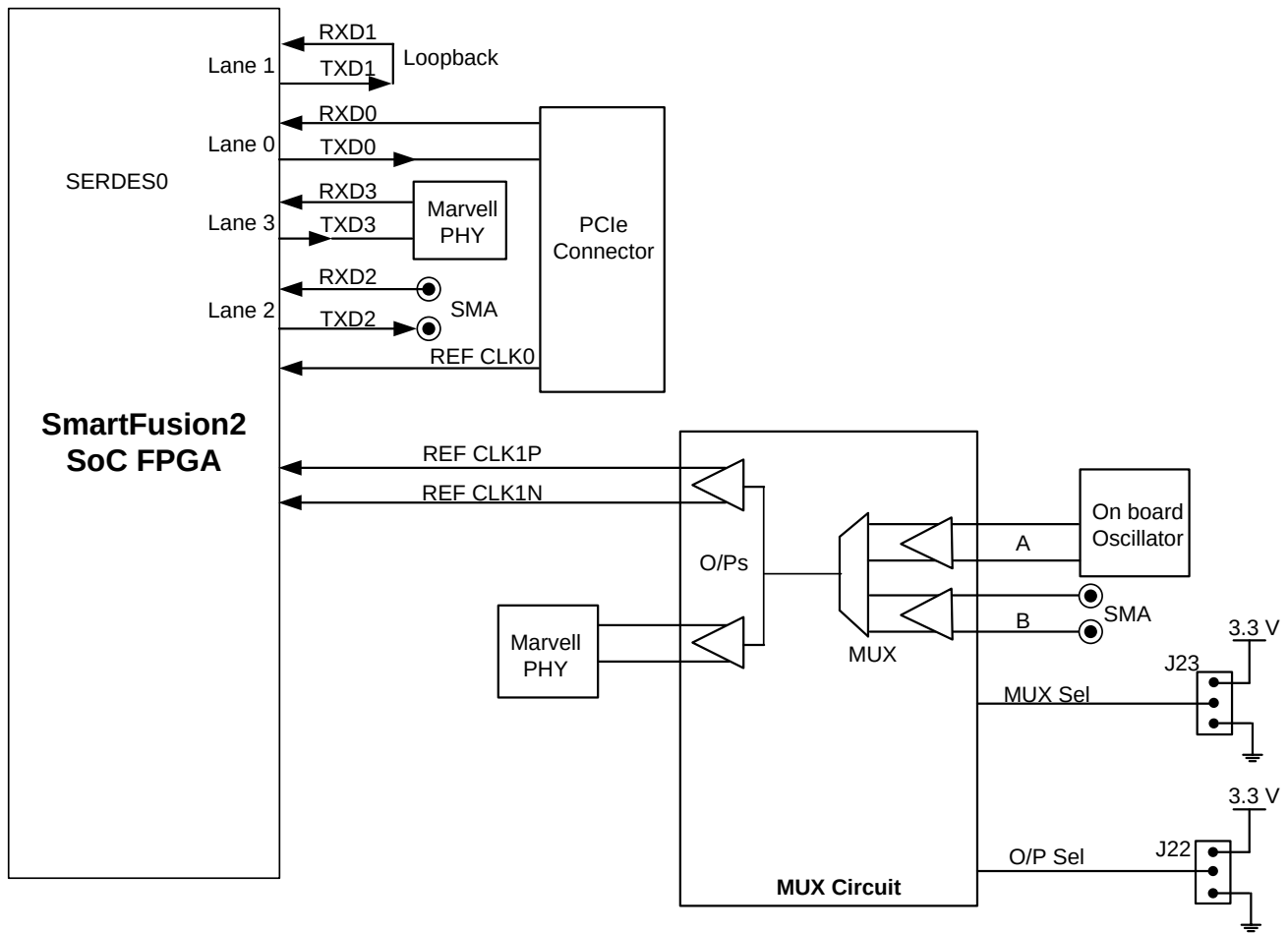


Figure 8 SERDES0 Interface

For more information on J22 and J23 jumpers, refer to [Table 4](#).

Note:

- SERDES0 TXD pairs are capacitively coupled to the SmartFusion2 device. Series AC coupling capacitors are used to provide common mode voltage independence.
- The AC coupling capacitors are not provided for SERDES 0 RXD signals. The mating board should have the AC coupling capacitors.
- For more information, refer to page 4 of Board Level Schematics document (provided separately).

USB Interface

The SMSC USB3320 is a high-speed USB 2.0 ULPI transceiver. It includes full support for the optional OTG protocol. CPEN: External 5 V supply enables. It controls the external VBUS power switch.

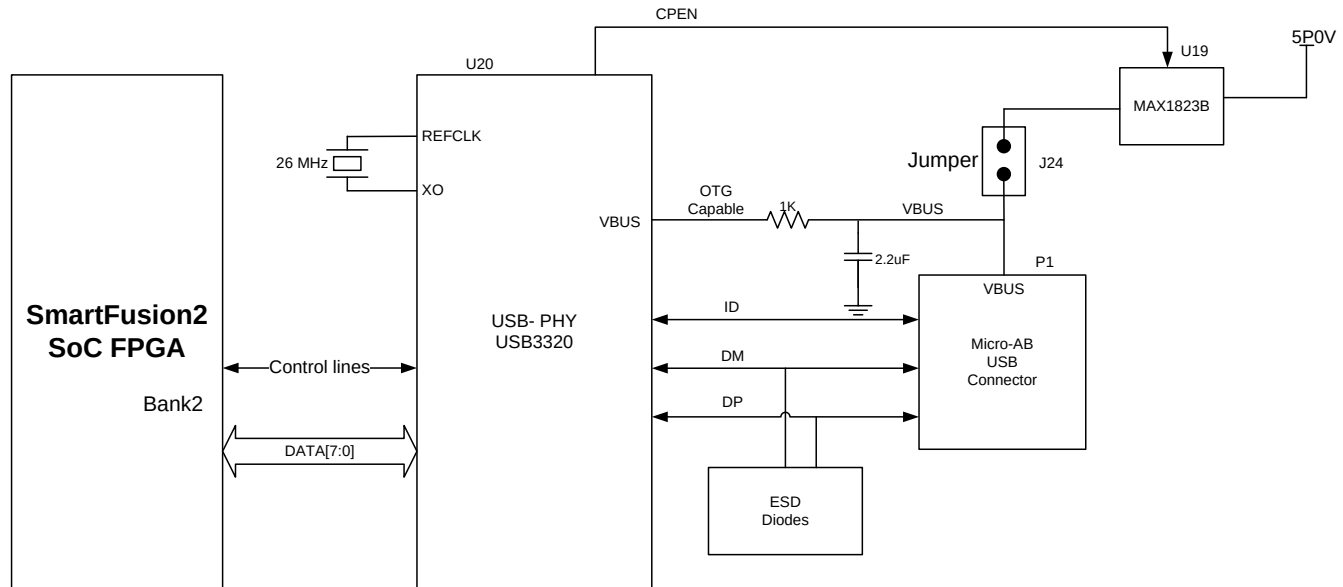


Figure 9 USB Interface

Note: For more information, refer to page 10 of Board Level Schematics document (provided separately).

Marvell PHY (88E1340S)

The SmartFusion2 Evaluation Kit utilizes the on board Marvell Alaska PHY device (88E1340S) for Ethernet communications at 100 or 1000 Mbps. 88E1340S has four independent gigabit Ethernet transceivers, but the board uses only one transceiver. Each transceiver performs all the physical layer functions for 100BASE-TX and 1000BASE-T full-duplex or half-duplex Ethernet on CAT5 twisted pair cable. The PHY connection to a user-provided Ethernet cable is through an RJ-45 connector with built-in magnetics.

The 88E1340S device supports the quad SGMII for direct connection to anSmartFusion2 chip. Refer to [Figure 10](#).

The 88E1340S is configured through the CONFIG [3:0] pins and CLK_SEL [1:0].

CLK_SEL [1:0] is used to select the reference clock input option. On board, the status of CLK_SEL0 is High and CLK_SEL1 is Low. REF_CLK is the 125 MHz reference differential clock input. It consists of LVDS differential inputs with a 100Ω differential internal termination resistor.

- RCLK – Gigabit recovered clock
- SCLK – 25 MHz synchronous input reference clock
- Expected reference clock (REF_CLK) specifications
 - Voltage level: 3.3 (± 0.3)V
 - Differential LVDS
 - Symmetry: 50% (± 10%)
 - Rise/Fall Time: 1nsec Max @ 20% to 80% of supply (3.3V)
 - Output Voltage Levels: 0: 0.90 Minimum, 1.10 Typical
1: 1.43 Typical, 1.60 Maximum
 - Differential Output Voltage: 247 mV Minimum, 454 mV Maximum

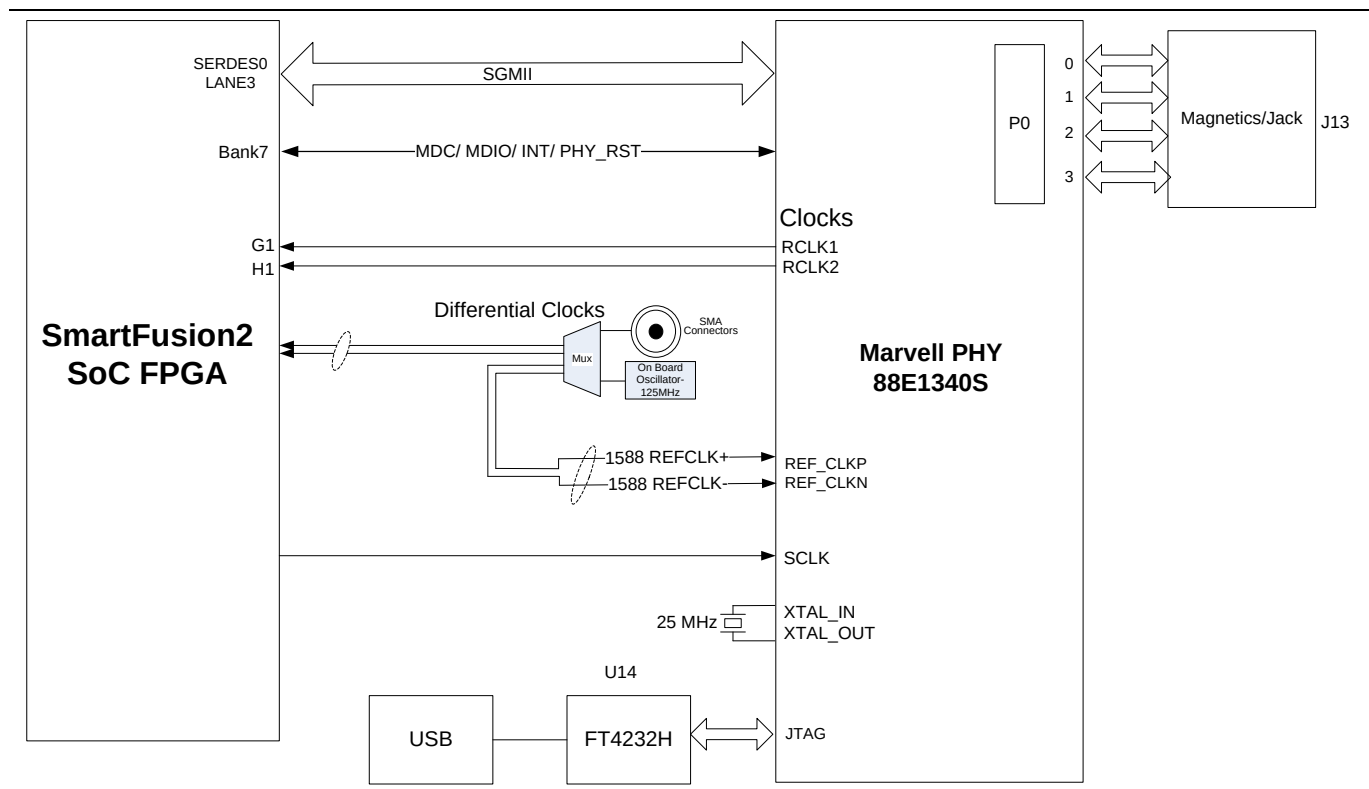


Figure 10 SmartFusion2 Marvell PHY Interface

Note: For more information, refer to page 11 and 12 of Board Level Schematics document (provided separately).

Programming

The SmartFusion2 device can be programmed through the JTAG interface. [Figure 11](#) shows various ways of SmartFusion2 programming.

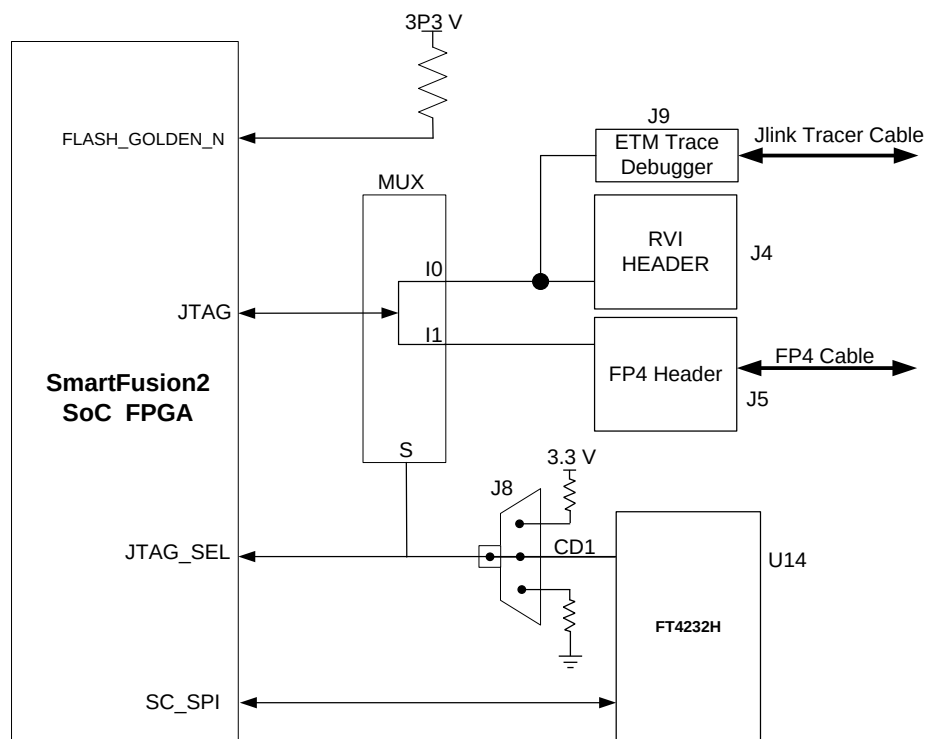


Figure 11 SmartFusion2 Programming Interface

JTAG_SEL: JTAG_SEL is used to switch between FP4 header (High) and RVI header or ETM header (Low).

For more information on J8 jumper, refer to [Table 4](#).

RVI Header

One 10X2 RVI header is provided on the board for debugging. This header allows plugging in the Keil ULINK debugger or IAR J-Link debugger.

FlashPro4 Programming Header

The SmartFusion2 device on the Evaluation Kit can be programmed using a FlashPro4 programmer. In addition, FlashPro4 is used for software debugging by SoftConsole.

Note:

- For more information, refer to page 13 of Board Level Schematics document (provided separately).
- For more details, refer to the [SmartFusion2 Programming User Guide](#).

FTDI Interface

Following are the FT4232H chip features:

- USB 2.0 high-speed (480 Mbps) to UART/MPSSE IC
- Single-chip USB to quad serial ports with a variety of configurations
- Entire USB protocol handled on the chip. USB specific firmware programming is not required
- USB 2.0 high-speed (480 Mbps) and full Speed (12 Mbps) compatible
- Two MPSSE on channel A and channel B, to simplify synchronous serial protocol (USB to JTAG, I2C, SPI, or bit-bang) design
- Fully assisted hardware or X-On/X-Off software handshaking
- +1.8 V (chip core) and +3.3 V I/O interfacing (+5 V tolerant)

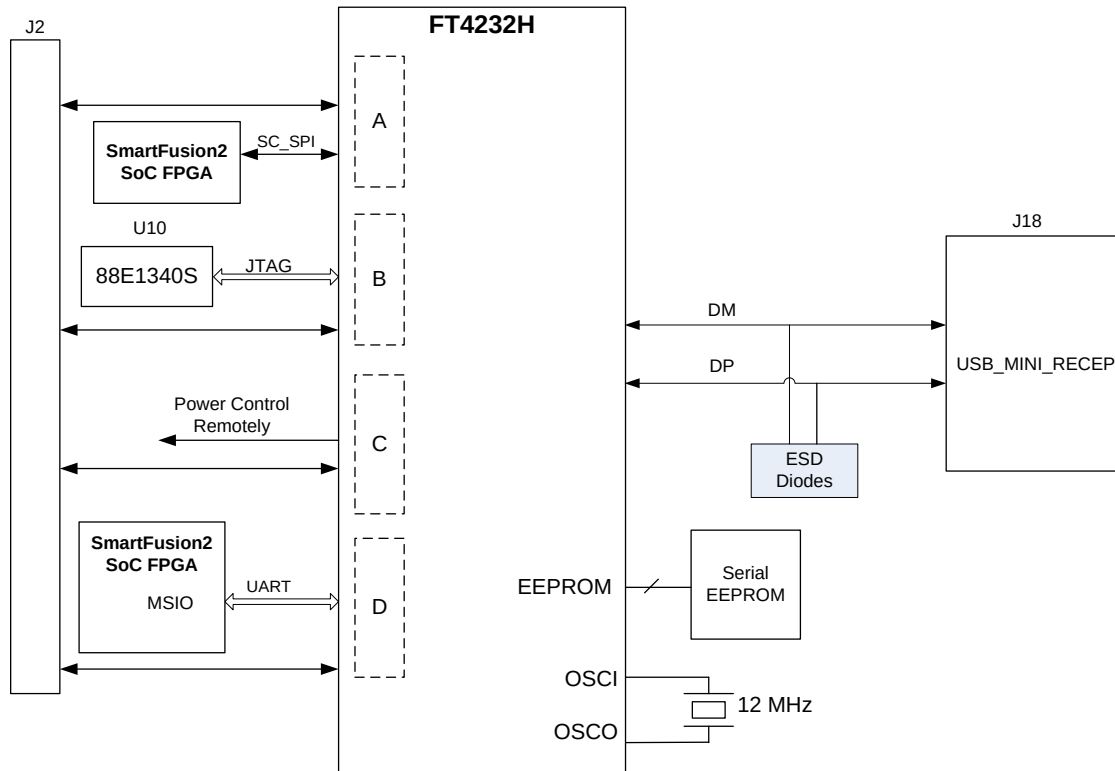


Figure 12 FTDI Interface

Note: For more information, refer to page 14 of Board Level Schematics document (provided separately).

I²C Port Header

Table 7 shows the two I²C ports routed to header – H1:

Table 7 I2C Port Header

Pin Number	SmartFusion2 Pin Name	Board Signal Name	Header - H1
G16	MSIO48NB1/I2C_0_SCL/GPIO_31_B	I2C0_SCL	10, 14
G17	MSIO48PB1/I2C_0_SDA/GPIO_30_B	I2C0_SDA	11, 15
R22	MSIO11NB3/CCC_NE1_CLKI0/I2C_1_SCL/ GPIO_1_A	I2C1_SCL	2, 6
P22	MSIO11PB3/CCC_NE0_CLKI0/I2C_1_SDA/ GPIO_0_A	I2C1_SDA	3, 7

Note: For more information, refer to page 8 of Board Level Schematics document (provided separately).

System Reset

The DEVRST_N signal (active low) is asserted, if the power supply level 3.3 V or 1.2 V fall below the threshold level or by pressing the SW6 (push-button switch). DEVRST_N is an input-only reset pad that allows assertion of a full reset to the chip at any time.

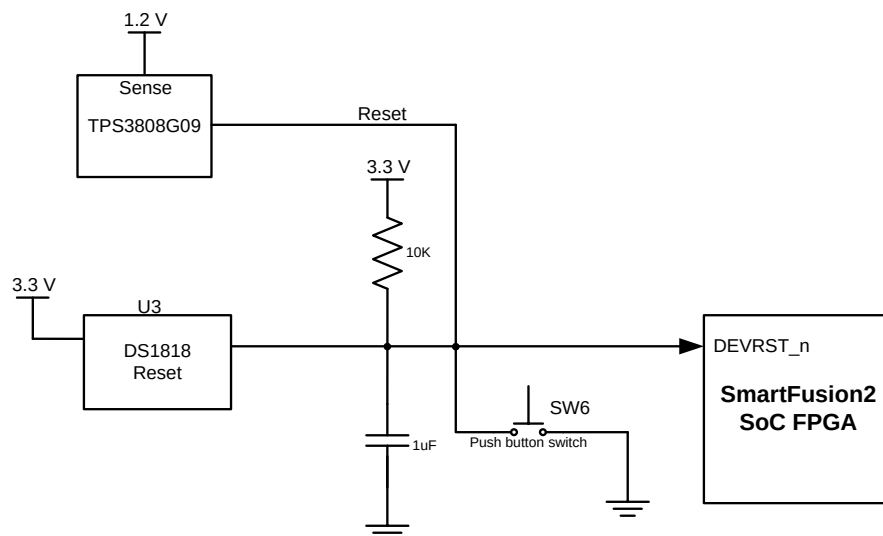


Figure 13 System Reset Interface

Note: For more information, refer to page13 of Board Level Schematics document (provided separately).

Clock Oscillator

50 MHz Clock Source

Figure 14 shows the 50 MHz clock oscillator with +/-50 ppm is available on the board. This clock oscillator is connected to the FPGA fabric to provide a system reference clock.

An on-chip SmartFusion2 PLL can be configured to generate a wide range of high precision clock frequencies.

Table 8 50 MHz Clock

SmartFusion2 Eval Kit	SmartFusion2- Pkg No	SmartFusion2 Pin Name
50MHZ_ SECLK_ WST_K1	K1	MSIOD121PB7/CCC_SW0_CLKI0

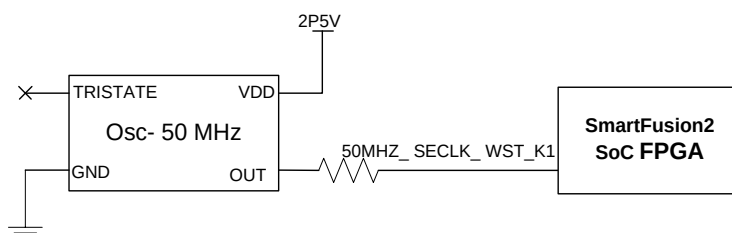


Figure 14 Clock Oscillator Interface

Note: For more information, refer to page 6 of Board Level Schematics document (provided separately).

Different Clock Sources

Following are the different clock sources used in M2S-EVAL-KIT:

- 125 MHz clock oscillator. For more information refer to [SERDES0 Interface](#).
- 32.768 KHz crystal oscillators for main and auxiliary oscillators of SmartFusion2 SoC FPGA.

Debugging

User LEDs

The board provides user access to eight active low LEDs, which are connected to the SmartFusion2 device for debugging applications. [Table 9](#). lists the onboard debugging LEDs.

Table 9 LEDs

SmartFusion2 Eval Kit	SmartFusion2- Pkg No	SmartFusion2 Pin Name
LED0 - Yellow	E1	MSIO105PB8
LED1 – Yellow	F4	MSIO106NB8
LED2 – Green	F3	MSIO106PB8
LED3 – Green	G7	MSIO107NB8
LED4 – Red	H7	MSIO107PB8
LED5 – Red	J6	MSIO108NB8
LED6 – Blue	H6	MSIO108PB8
LED7 - Blue	H5	MSIO109NB8

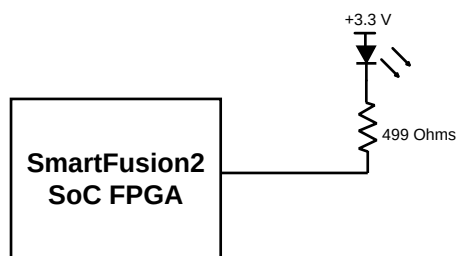


Figure 15 LEDs Interface

Note: For more information, refer to page 15 of Board Level Schematics document (provided separately).

Push-Button Switches

The SmartFusion2 Evaluation Kit comes with five push-button tactile switches that are connected to the SmartFusion2 device. [Table 10](#) lists the onboard push-button switches.

Table 10 Push-Button Switches

SmartFusion2 Eval Kit	SmartFusion2- Pkg No	SmartFusion2 Pin Name
SWITCH1	L20	MSIO17NB3
SWITCH2	K16	MSIO23NB3
SWITCH3	K18	MSIO24PB3
SWITCH4	J18	MSIO24NB3
SW6	R15	DEV_RST_N

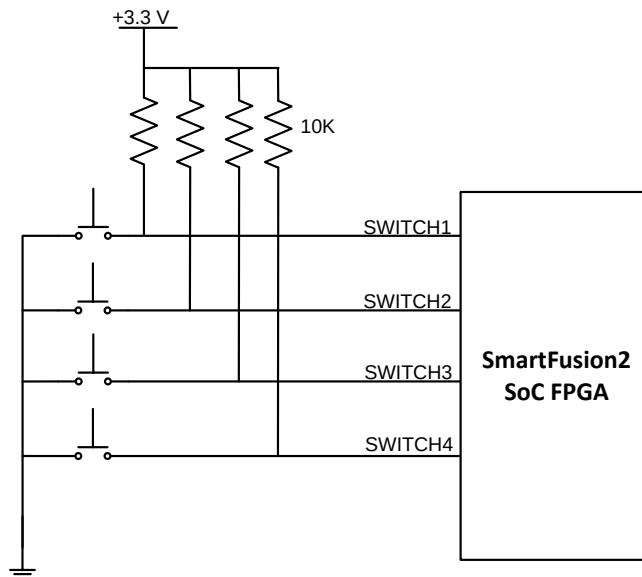


Figure 16 Switches Interface

Note: For more information, refer to page 15 of Board Level Schematics document (provided separately).

Slide Switches–DPDT

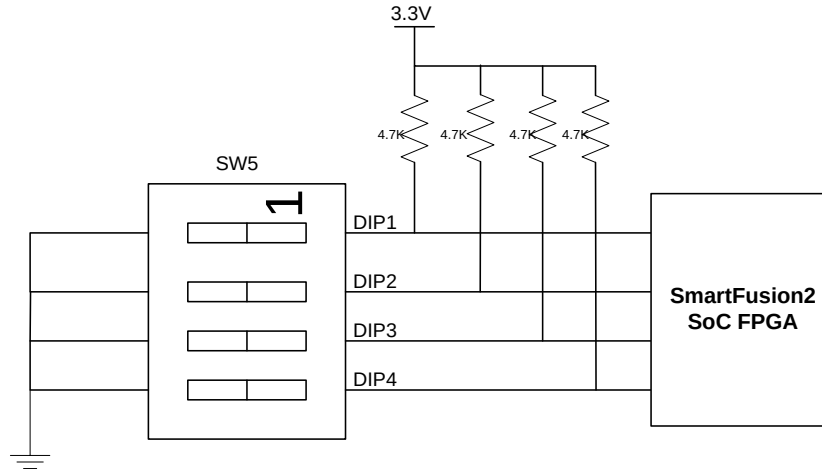
SW7–Power ON/OFF switch from external DC Jack, +12 V DC

DIP Switch- SPST

SW5–is a DIP switch that has four connections to the SmartFusion2 device. [Table 11.](#) lists the onboard DIP switches.

Table 11 DIP Switches

SmartFusion2 Eval Kit	SmartFusion2- Pkg No	SmartFusion2 Pin Name
DIP1	L19	MSIO18PB3
DIP2	L18	MSIO18NB3
DIP3	K21	MSIO19PB3
DIP4	K20	MSIO19NB3


Figure 17 SPST Interface

Note: For more information, refer to page 15 of Board Level Schematics document (provided separately).

GPIO Header Pin Out

Bank 4, bank 7, and bank 1 signals are routed to the GPIO header for user applications. [Table 12](#) lists the GPIO header pin out details.

Table 12 GPIO Header PinOut

SmartFusion2 – U1			SmartFusion2 – U1		
GPIO Header- J1			GPIO Header- J1		
Pin No	Pkg No	Pin Name	Pin No	Pkg No	Pin Name
1	AB15	DDRIO164PB5	2		3P3V
3	AA15	DDRIO164NB5	4		VSS
5		VSS	6	AA16	DDRIO167PB5
7	AB18	DDRIO177PB5	8	AA17	DDRIO167NB5
9	AB19	DDRIO177NB5	10		VSS
11		VSS	12	AB17	DDRIO174PB5
13	Y18	DDRIO181PB5	14	AA18	DDRIO174NB5
15	Y19	DDRIO181NB5	16		VSS
17		VSS	18	Y17	DDRIO182PB5
19	W16	DDRIO184PB5	20	W17	DDRIO182NB5
21	V16	DDRIO184NB5	22		VSS
23		VSS	24	U14	DDRIO176PB5
25	C22	MSIO47PB1	26	U15	DDRIO176NB5
27	B22	MSIO47NB1	28		VSS
29		VSS	30	V13	DDRIO171PB5
31	Y15	DDRIO172PB5	32	V14	DDRIO171NB5
33	W15	DDRIO172NB5	34		VSS

GPIO Header- J1			SmartFusion2 – U1		
Pin No	Pkg No	Pin Name	Pin No	Pkg No	Pin Name
35		VSS	36	G5	MSIO98PB8
37	F5	MSIO99PB8	38	G6	MSIO98NB8
39	F6	MSIO99NB8	40		VSS
41		VSS	42	E4	MSIO102PB8
43	C4	MSIO96PB8	44	E5	MSIO102NB8
45	D5	MSIO96NB8	46		VSS
47		VSS	48	C3	MSIO97PB8
49	B2	MSIO101PB8	50	B3	MSIO97NB8
51	A2	MSIO101NB8	52		VSS
53		VSS	54	C1	MSIO103PB8
55	D1	MSIO104PB8	56	B1	MSIO103NB8
57	D2	MSIO104NB8	58		VSS
59		VSS	60	D3	MSIO100PB8
61		3P3V	62	D4	MSIO100NB8
63		3P3V	64		VSS

4 – Pin List

Table 13 lists the pins for SmartFusion2 M2S025T-FGG484 devices.

Note: *D21- Pin cannot be used as a fabric output and it is only an Input.

Table 13 Pin List update with latest of M2S025T-FGG484

PKG.PIN	M2S025TS/M2S025T-FGG484 Pin Name
A1	VSS
A10	DDRIO57PB0/MDDR_DM_RDQS0
A11	DDRIO57NB0/MDDR_DQ4
A12	DDRIO54PB0/MDDR_DQ8
A13	DDRIO54NB0/MDDR_DQ9
A14	DDRIO50PB0/GB12/CCC_NE1_CLKI2/MDDR_DQ12
A15	DDRIO50NB0/MDDR_DQ13
A16	DDRIO45PB0/MDDR_CLK
A17	DDRIO45NB0/MDDR_CLK_N
A18	DDRIO44PB0/MDDR_BA0
A19	DDRIO44NB0/MDDR_BA1
A2	MSIO85NB7
A20	DDRIO40NB0/MDDR_ADDR6
A21	DDRIO37PB0/MDDR_ADDR10
A22	VSS
A3	DDRIO79NB0
A4	DDRIO79PB0
A5	DDRIO78NB0
A6	DDRIO65NB0/GB4/CCC_NW1_CLKI2
A7	DDRIO62PB0/MDDR_DQ_ECC1
A8	DDRIO62NB0/MDDR_DQ_ECC0
A9	DDRIO60NB0/MDDR_DQ1
AA1	VSS
AA10	MSIO122PB4
AA11	MSIO124PB4
AA12	MSIO127PB4
AA13	MSIO130PB4/VCCC_SE0_CLKI
AA14	VSS
AA15	MSIO134NB4
AA16	MSIO138PB4

PKG.PIN	M2S025TS/M2S025T-FGG484 Pin Name
AA17	MSIO138NB4
AA18	MSIO137NB4
AA19	VDDI4
AA2	SERDES_0_TXD0_N
AA20	XTLOSC_AUX_EXTAL
AA21	XTLOSC_MAIN_EXTAL
AA22	JTAGSEL
AA3	VSS
AA4	SERDES_0_TXD1_N
AA5	VSS
AA6	SERDES_0_TXD2_N
AA7	VSS
AA8	SERDES_0_TXD3_N
AA9	VSS
AB1	VSS
AB10	MSIO122NB4
AB11	MSIO124NB4
AB12	VDDI4
AB13	MSIO129PB4/CCC_SW1_CLKI3
AB14	MSIO129NB4
AB15	MSIO134PB4/VCCC_SE1_CLKI
AB16	VSS
AB17	MSIO137PB4
AB18	MSIO142PB4
AB19	MSIO142NB4
AB2	SERDES_0_TXD0_P
AB20	XTLOSC_AUX_XTAL
AB21	XTLOSC_MAIN_XTAL
AB22	VSS
AB3	VSS
AB4	SERDES_0_TXD1_P
AB5	VSS
AB6	SERDES_0_TXD2_P
AB7	VSS
AB8	SERDES_0_TXD3_P
AB9	VSS
B1	MSIO87NB7
B10	VSS
B11	DDRIO58PB0/MDDR_DQS0
B12	VDDI0
B13	DDRIO52PB0/GB8/CCC_NE0_CLKI3/MDDR_DQS1

PKG.PIN	M2S025TS/M2S025T-FGG484 Pin Name
B14	VSS
B15	DDRIO47PB0/MDDR_CKE
B16	VDDI0
B17	DDRIO43NB0/MDDR_ADDR0
B18	VSS
B19	DDRIO40PB0/MDDR_ADDR5
B2	MSIO85PB7
B20	VDDI0
B21	DDRIO37NB0/MDDR_ADDR11
B22	MSIO33NB1/MMUART_0_CLK/GPIO_29_B/USB_NXT_C
B3	MSIO81NB7
B4	VSS
B5	DDRIO78PB0
B6	DDRIO65PB0/GB0/CCC_NW0_CLKI3
B7	DDRIO64NB0/MDDR_DQS_ECC_N
B8	VDDI0
B9	DDRIO60PB0/MDDR_DQ0
C1	MSIO87PB7
C10	VDDI0
C11	DDRIO58NB0/MDDR_DQS0_N
C12	VSS
C13	DDRIO52NB0/MDDR_DQS1_N
C14	VDDI0
C15	DDRIO47NB0/MDDR_CS_N
C16	DDRIO43PB0/MDDR_BA2
C17	DDRIO41PB0/MDDR_ADDR3
C18	DDRIO41NB0/MDDR_ADDR4
C19	DDRIO39NB0/MDDR_ADDR7
C2	VDDI7
C20	DDRIO39PB0/MDDR_ODT
C21	VSS
C22	MSIO33PB1/MMUART_0_RXD/GPIO_28_B/USB_STP_C
C3	MSIO81PB7
C4	MSIO80PB7
C5	DDRIO77PB0
C6	VDDI0
C7	DDRIO64PB0/MDDR_DQS_ECC
C8	VSS
C9	DDRIO61NB0
D1	MSIO88PB7
D10	DDRIO56PB0/MDDR_DQ5
D11	DDRIO56NB0/MDDR_DQ6

PKG.PIN	M2S025TS/M2S025T-FGG484 Pin Name
D12	DDRIO53PB0/CCC_NE0_CLKI2/MDDR_DQ10
D13	DDRIO53NB0/MDDR_DQ11
D14	DDRIO49PB0/CCC_NE1_CLKI3/MDDR_DQ14
D15	VSS
D16	DDRIO42PB0/MDDR_ADDR1
D17	VDDI0
D18	DDRIO35PB0/MDDR_ADDR14
D19	VSS
D2	MSIO88NB7
D20	DDRIO36NB0/MDDR_ADDR13
D21	MSI32NB1 /MMUART_0_TXD/GPIO_27_B/USB_DIR_C
D22	FLASH_GOLDEN_N
D3	MSIO84PB7
D4	MSIO84NB7
D5	MSIO80NB7
D6	DDRIO77NB0
D7	MDDR_IMP_CALIB
D8	DDRIO63NB0/MDDR_DM_RDQS_ECC
D9	DDRIO61PB0/CCC_NW1_CLKI3
E1	MSIO89PB7
E10	DDRIO59NB0/MDDR_DQ3
E11	VDDI0
E12	DDRIO55PB0/MDDR_DQ7
E13	DDRIO49NB0/MDDR_DQ15
E14	VSS
E15	DDRIO46PB0/MDDR_RESET_N
E16	DDRIO42NB0/MDDR_ADDR2
E17	DDRIO38PB0/MDDR_ADDR8
E18	DDRIO35NB0/MDDR_ADDR15
E19	DDRIO36PB0/MDDR_ADDR12
E2	MSIO89NB7
E20	VDDI1
E21	MSIO31NB1/MMUART_0_DCD/GPIO_22_B
E22	MSIO31PB1/MMUART_0_RI/GPIO_21_B
E3	VSS
E4	MSIO86PB7
E5	MSIO86NB7
E6	VSS
E7	DDRIO66PB0/MDDR_TMATCH_ECC_OUT
E8	DDRIO63PB0/MDDR_TMATCH_ECC_IN
E9	VSS
F1	VDDI7

PKG.PIN	M2S025TS/M2S025T-FGG484 Pin Name
F10	DDRIO59PB0/MDDR_DQ2
F11	VSS
F12	DDRIO55NB0/MDDR_TMATCH_0_OUT
F13	VDDI0
F14	DDRIO48PB0/MDDR_RAS_N
F15	DDRIO46NB0/MDDR_CAS_N
F16	VSS
F17	DDRIO38NB0/MDDR_ADDR9
F18	MSIO30NB1/MMUART_0_DSR/GPIO_20_B
F19	MSIO30PB1/MMUART_0_CTS/GPIO_19_B/USB_DATA7_C
F2	MSIO94NB7
F20	MSIO29NB1/MMUART_0_DTR/GPIO_18_B/USB_DATA6_C
F21	MSIO29PB1/MMUART_0_RTS/GPIO_17_B/USB_DATA5_C
F22	VDDI1
F3	MSIO90PB7
F4	MSIO90NB7
F5	MSIO83PB7
F6	MSIO83NB7
F7	VDDI0
F8	DDRIO66NB0/CCC_NW0_CLKI2
F9	VDDI0
G1	MSIO96NB7
G10	VREF0
G11	VREF0
G12	DDRIO51PB0/MDDR_TMATCH_0_IN
G13	DDRIO51NB0/MDDR_DM_RDQS1
G14	DDRIO48NB0/MDDR_WE_N
G15	VREF0
G16	MSIO34NB1/I2C_0_SCL/GPIO_31_B/USB_DATA1_C
G17	MSIO34PB1/I2C_0_SDA/GPIO_30_B/USB_DATA0_C
G18	MSIO28NB1/MMUART_1_RXD/GPIO_26_B/USB_DATA3_C
G19	MSIO28PB1/GB14/VCCC_SE1_CLKI/MMUART_1_CLK/GPIO_25_B/USB_DATA4_C
G2	MSIO94PB7
G20	VSS
G21	MSIO26NB1/MMUART_1_DCD/GPIO_16_B
G22	MSIO26PB1/CCC_NE1_CLKI1/MMUART_1_RI/GPIO_15_B
G3	MSIO95NB7
G4	VDDI7
G5	MSIO82PB7
G6	MSIO82NB7
G7	MSIO91NB7
G8	CCC_NW1_PLL_VSSA

PKG.PIN	M2S025TS/M2S025T-FGG484 Pin Name
G9	CCC_NW1_PLL_VDDA
H1	MSIO96PB7/GB6/CCC_NW1_CLKI1
H10	VDD
H11	VSS
H12	VDDI0
H13	VSS
H14	VDDI0
H15	CCC_NE0_PLL_VDDA
H16	MSS_MDDR_PLL_VDDA
H17	MSS_MDDR_PLL_VSSA
H18	VDDI1
H19	MSIO27NB1/MMUART_1_TXD/GPIO_24_B/USB_DATA2_C
H2	VSS
H20	MSIO27PB1/GB10/VCCC_SE0_CLKI/USB_XCLK_C
H21	MSIO24NB1/MMUART_1_DTR/GPIO_12_B
H22	MSIO24PB1/MMUART_1_RTS/GPIO_11_B
H3	MSIO95PB7
H4	MSIO93PB7
H5	MSIO93NB7
H6	MSIO92PB7
H7	MSIO91PB7
H8	CCC_NW0_PLL_VDDA
H9	VSS
J1	MSIO98PB7/CCC_NW1_CLKI0
J10	VSS
J11	VDD
J12	VSS
J13	VDD
J14	VSS
J15	CCC_NE0_PLL_VSSA
J16	CCC_NE1_PLL_VSSA
J17	CCC_NE1_PLL_VDDA
J18	MSIO23NB2/SPI_1_SS3/GPIO_16_A
J19	MSIO25NB1/MMUART_1_DSR/GPIO_14_B
J2	MSIO98NB7
J20	MSIO25PB1/CCC_NE0_CLKI1/MMUART_1_CTS/GPIO_13_B
J21	VDDI1
J22	MSIO20NB2/GB13/VCCC_SE1_CLKI/GPIO_26_A
J3	MSIO97PB7/GB2/CCC_NW0_CLKI1
J4	MSIO97NB7
J5	VSS
J6	MSIO92NB7

PKG.PIN	M2S025TS/M2S025T-FGG484 Pin Name
J7	VDDI7
J8	CCC_NW0_PLL_VSSA
J9	VDD
K1	MSIOD103PB6/CCC_SW0_CLKI0
K10	VDD
K11	VSS
K12	VDD
K13	VSS
K14	VDD
K15	MSIO21NB2/SPI_0_SS2/GPIO_9_A/USB_DATA6_A
K16	MSIO22NB2/SPI_1_SS1/GPIO_14_A
K17	MSIO22PB2/SPI_0_SS3/GPIO_10_A/USB_DATA7_A
K18	MSIO23PB2/SPI_1_SS2/GPIO_15_A
K19	VSS
K2	MSIOD103NB6
K20	MSIO19NB2/SPI_1_SS7/GPIO_24_A
K21	MSIO19PB2/SPI_1_SS6/GPIO_23_A
K22	MSIO20PB2/GB9/VCCC_SE0_CLKI/GPIO_25_A
K3	VDDI6
K4	MSIOD100PB6/GB5/CCC_SW1_CLKI1
K5	MSIOD100NB6
K6	MSIO99PB7/CCC_NW0_CLKI0
K7	MSIO99NB7
K8	MSIOD101PB6/GB1/CCC_SW0_CLKI1
K9	VSS
L1	VSS
L10	VSS
L11	VDD
L12	VSS
L13	VDD
L14	VSS
L15	VPP
L16	MSIO21PB2/SPI_0_SS1/GPIO_8_A/USB_DATA5_A
L17	VDDI2
L18	MSIO18NB2/SPI_1_SS5/GPIO_18_A
L19	MSIO18PB2/SPI_1_SS4/GPIO_17_A
L2	MSIOD104PB6
L20	MSIO17NB2/SPI_1_SS0/GPIO_13_A
L21	MSIO17PB2/SPI_1_SDO/GPIO_12_A
L22	VSS
L3	MSIOD104NB6
L4	MSIOD105PB6

PKG.PIN	M2S025TS/M2S025T-FGG484 Pin Name
L5	MSIOD105NB6
L6	VDDI6
L7	MSIOD102NB6
L8	MSIOD101NB6
L9	VDD
M1	MSIOD110NB6
M10	VDD
M11	VSS
M12	VDD
M13	VSS
M14	VDD
M15	VPPNVM
M16	MSIO14PB2/SPI_0_SS4/GPIO_19_A
M17	MSIO14NB2/SPI_0_SS5/GPIO_20_A
M18	MSIO15PB2/SPI_0_SS6/GPIO_21_A
M19	MSIO15NB2/SPI_0_SS7/GPIO_22_A
M2	MSIOD108NB6
M20	VDDI2
M21	MSIO16PB2/SPI_1_CLK
M22	MSIO16NB2/SPI_1_SDI/GPIO_11_A
M3	MSIOD108PB6
M4	VSS
M5	MSIOD106PB6
M6	MSIOD106NB6
M7	MSIOD102PB6/CCC_SW1_CLKI0
M8	MSIOD113NB6
M9	VSS
N1	MSIOD110PB6
N10	VSS
N11	VDD
N12	VSS
N13	VDD
N14	VSS
N15	VSSNVM
N16	MSIO8PB2/CAN_RX/GPIO_3_A/USB_DATA1_A
N17	MSIO8NB2/CAN_TX_EN_N/GPIO_4_A/USB_DATA2_A
N18	VSS
N19	MSIO12PB2/SPI_0_CLK/USB_XCLK_A
N2	VDDI6
N20	MSIO12NB2/SPI_0_SDI/GPIO_5_A/USB_DIR_A
N21	MSIO13PB2/SPI_0_SDO/GPIO_6_A/USB_STP_A
N22	MSIO13NB2/SPI_0_SS0/GPIO_7_A/USB_NXT_A

PKG.PIN	M2S025TS/M2S025T-FGG484 Pin Name
N3	MSIOD109PB6
N4	MSIOD109NB6
N5	MSIOD107PB6
N6	MSIOD107NB6
N7	VSS
N8	MSIOD113PB6
N9	VDD
P1	MSIOD112PB6
P10	VDD
P11	VSS
P12	VDD
P13	VSS
P14	VDD
P15	VPP
P16	MSIO7NB2/CAN_TX/GPIO_2_A/USB_DATA0_A
P17	MSIO6PB2/USB_DATA6_B
P18	MSIO6NB2
P19	SC_SPI_SDO
P2	MSIOD112NB6
P20	SC_SPI_SS
P21	VSS
P22	MSIO11PB2/CCC_NE0_CLKI0/I2C_1_SDA/GPIO_0_A/USB_DATA3_A
P3	MSIOD111NB6
P4	MSIOD111PB6
P5	VDDI6
P6	MSIOD114PB6
P7	MSIOD114NB6
P8	SERDES_0_VDD
P9	VSS
R1	MSIOD115NB6
R10	VSS
R11	VDD
R12	VSS
R13	VDD
R14	VSS
R15	DEVRST_N
R16	MSIO7PB2
R17	MSIO1PB2/USB_XCLK_B
R18	MSIO1NB2/USB_DIR_B
R19	VDDI2
R2	MSIOD115PB6

PKG.PIN	M2S025TS/M2S025T-FGG484 Pin Name
R20	SC_SPI_CLK
R21	SC_SPI_SDI
R22	MSIO11NB2/CCC_NE1_CLKI0/I2C_1_SCL/GPIO_1_A/USB_DATA4_A
R3	MSIOD116PB6
R4	MSIOD116NB6
R5	VSS
R6	CCC_SW0_PLL_VSSA
R7	CCC_SW1_PLL_VDDA
R8	SERDES_0_L01_VDDAIO
R9	VSS
T1	MSIOD118NB5/SERDES_0_REFCLK0_N
T10	SERDES_0_L23_VDDAIO
T11	NC
T12	NC
T13	MSIO131NB4
T14	VDDI4
T15	VSS
T16	MSIO143NB4
T17	VSS
T18	MSIO2PB2/USB_STP_B
T19	MSIO2NB2/USB_NXT_B
T2	VSS
T20	MSIO5PB2/USB_DATA4_B
T21	MSIO5NB2/USB_DATA5_B
T22	VDDI2
T3	MSIOD117NB6
T4	MSIOD117PB6
T5	CCC_SW0_PLL_VDDA
T6	SERDES_0_PLL_VSSA
T7	CCC_SW1_PLL_VSSA
T8	SERDES_0_PLL_VDDA
T9	SERDES_0_VDD
U1	MSIOD118PB5/SERDES_0_REFCLK0_P
U10	MSIO123PB4
U11	MSIO123NB4
U12	VSS
U13	MSIO131PB4/GB11/VCCC_SE0_CLKI
U14	MSIO136PB4
U15	MSIO136NB4
U16	MSIO143PB4
U17	MSIO144NB4
U18	MSIO146NB4

PKG.PIN	M2S025TS/M2S025T-FGG484 Pin Name
U19	MSIO0PB2
U2	VDDI5
U20	VSS
U21	MSIO4NB2/USB_DATA3_B
U22	MSIO4PB2/USB_DATA2_B
U3	MSIOD119PB5/SERDES_0_REFCLK1_P
U4	MSIOD119NB5/SERDES_0_REFCLK1_N
U5	SERDES_0_L01_REXT
U6	SERDES_0_L01_REFRET
U7	SERDES_0_L01_VDDAPLL
U8	SERDES_0_L23_VDDAPLL
U9	VPP
V1	VSS
V10	VDDI4
V11	MSIO125PB4/GB3/CCC_SW0_CLKI3
V12	MSIO128NB4
V13	MSIO132PB4
V14	MSIO132NB4
V15	VSS
V16	MSIO139NB4
V17	MSIO144PB4
V18	MSIO146PB4
V19	MSIO0NB2/USB_DATA7_B
V2	VSS
V20	JTAG_TMS/M3_TMS/M3_SWDIO
V21	MSIO3NB2/USB_DATA1_B
V22	MSIO3PB2/USB_DATA0_B
V3	VSS
V4	VSS
V5	VSS
V6	VSS
V7	VSS
V8	SERDES_0_L23_REXT
V9	SERDES_0_L23_REFRET
W1	SERDES_0_RXD0_P
W10	MSIO121PB4/PROBE_A
W11	MSIO125NB4/GB7/CCC_SW1_CLKI2
W12	MSIO128PB4
W13	VDDI4
W14	MSIO133NB4
W15	MSIO135NB4
W16	MSIO139PB4

PKG.PIN	M2S025TS/M2S025T-FGG484 Pin Name
W17	MSIO140NB4
W18	VSS
W19	MSIO145NB4
W2	VSS
W20	JTAG_TCK/M3_TCK
W21	VDDI3
W22	JTAG_TDI/M3_TDI
W3	SERDES_0_RXD1_P
W4	VSS
W5	SERDES_0_RXD2_P
W6	VSS
W7	SERDES_0_RXD3_P
W8	VSS
W9	MSIO120PB4
Y1	SERDES_0_RXD0_N
Y10	MSIO121NB4/PROBE_B
Y11	VSS
Y12	MSIO127NB4
Y13	MSIO130NB4
Y14	MSIO133PB4/GB15/VCCC_SE1_CLKI
Y15	MSIO135PB4
Y16	VDDI4
Y17	MSIO140PB4
Y18	MSIO141PB4
Y19	MSIO141NB4
Y2	VSS
Y20	MSIO145PB4
Y21	JTAG_TDO/M3_TDO/M3_SWO
Y22	JTAG_TRSTB/M3_TRSTB
Y3	SERDES_0_RXD1_N
Y4	VSS
Y5	SERDES_0_RXD2_N
Y6	VSS
Y7	SERDES_0_RXD3_N
Y8	VSS
Y9	MSIO120NB4/CCC_SW0_CLKI2

5– Board Components Placement

The SmartFusion2 Evaluation Kit components placement on top and bottom sides, are shown in the following figures.



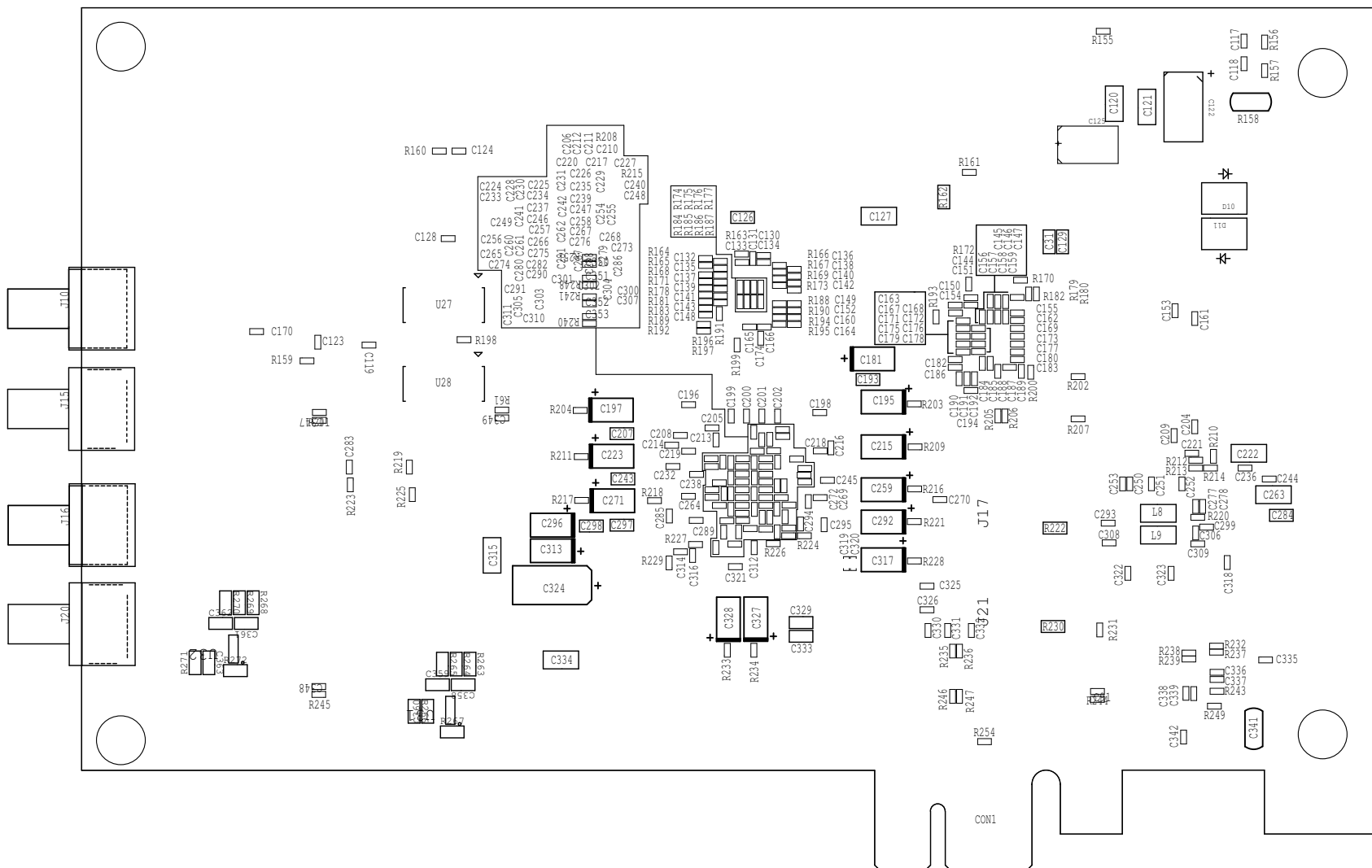


Figure 19. Silkscreen Bottom View

6 – Demo Design

M2S-EVAL-KIT Board Demo Design

The M2S-EVAL-KIT comes with a preloaded PCIe control plane demo design. This demo design demonstrates the key features of the SmartFusion2 device such as - PCIe, GPIOs, and fabric interface controller of the SmartFusion2 device. These features can be used for rapid prototyping and validation of user specific designs.

Note: For more details on running the demo designs, refer to the [SmartFusion2 FPGA Evaluation Kit PCIe Demo Guide](#) (to be released).

7– Manufacturing Test

M2S-EVAL-KIT Board Testing Procedures

M2S-EVAL-KIT contains a manufacturing test program that can be run to verify the functionality of the board. This program contains a list of options that can be run as diagnostics for the SERDES interface, LPDDR, SPI flash, I2C, SGMII, and debugging the LEDs and switches. From the list of provided menu options, either one or all of the tests can be selected to verify the functionality.

Setting Up the Board for Test

Jumper Settings

- Jumper J3 short pin 1-2
- Short Jumper J8 to 1-2 position.
- Short jumper J22,J23 to 1-2 Position
- Short jumper H1 pin 6-10 and pin 7-11 Position
- Short Jumper J24 to 1-2 position.

Requirements to Run EVAL KIT MTD Test

Power

- Connect 12 V power supply brick to J6 to power the board.
- Slide the main power switch SW7 to ON position.

Programming

- Connect the FP4 header to J5.
- Open the FlashPro Programming Software.
- Create a new programming project and select the **Single Device** when choosing programming mode.
- Click **Configure Device**. This will open the **Load Programming File** window.
- Browse the PC file system to find the SB1_top.stp programming file. Click **Open** to select the SB1_top.stp file.
- Click **Program** to program the M2S-EVAL-KIT device.

HyperTerminal communication

- Connect USB cable (mini USB to Type A USB cable) to J18 and other end connect it to USB port of test PC. This is required for HyperTerminal communication.

Note: Make sure test PC should have FTDI drivers installed. These are available at <http://www.ftdichip.com/Drivers/D2XX.htm>.

SGMII test

- Connect network Ethernet cable to J13 (RJ 45 connector).
- Other end of Ethernet cable should be connecting to network or Ethernet switch.

SERDES LOOPBACK Test

- Connect SMA Cable one end to J20 and other end to J15 of Eval kit.
- Connect SMA Cable one end to J16 and other end to J10 of Eval kit.

Before testing the SmartFusion2 Evaluation Kit:

- Download SB1_top.stp, SF2_SGMII_MDDR_top.stp, and PMA_SERDES_CONFIGURATOR.exe files from www.microsemi.com/soc/download/rsc/?f= SmartFusion2_EVAL_KIT_MTD.
- Download and install the drivers from: <http://www.ftdichip.com/Drivers/D2XX.htm>

Loopback Test on SERDES Lanes

Table 14 shows the list of tests performed on the four SERDES lanes in external physical coding sublayer (EPCS) mode.

Table 14 SERDES Lanes Loopback Tests

Lane	Tests Performed
Lane 0	Internal loopback
Lane 1	Internal and external loopback (Onboard 6 inches trace loopback)
Lane 2	Internal loopback, External Loopback using Loopback cables
Lane 3	Internal loopback

Internal Loopback Test on SERDES Lanes

1. Connect USB cable (mini USB to Type A USB cable) to J18 and other end of the cable to the USB port of test PC. This is required for SERDES and UART communication.
2. Switch **ON** the SW7 power supply switch.
3. Make sure that the board is programmed with SB1_top.stp file.
4. Double-click the PMA_SERDES_CONFIGURATOR.exe file to open the PMA SERDES analyzer to test the Evaluation Kit board. [Figure 20](#) shows the SERDES TEST APP window.

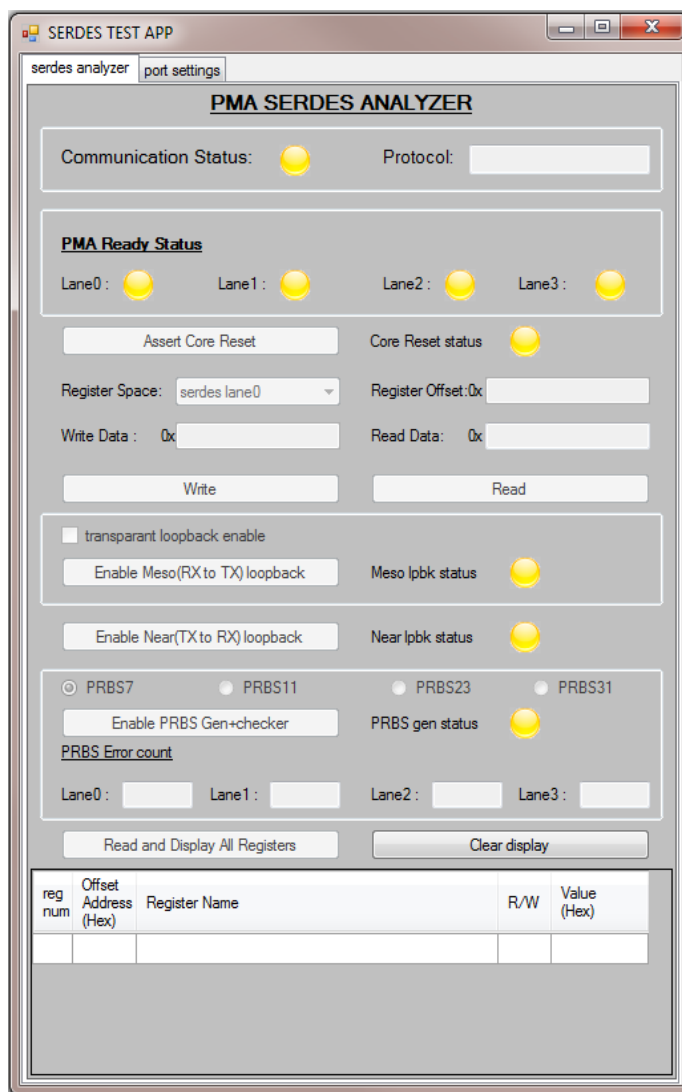


Figure 20 SERDES TEST APP Window

5. Click the **port settings** tab on the SERDES TEST APP window. [Figure 21](#) shows the **port settings** tab.

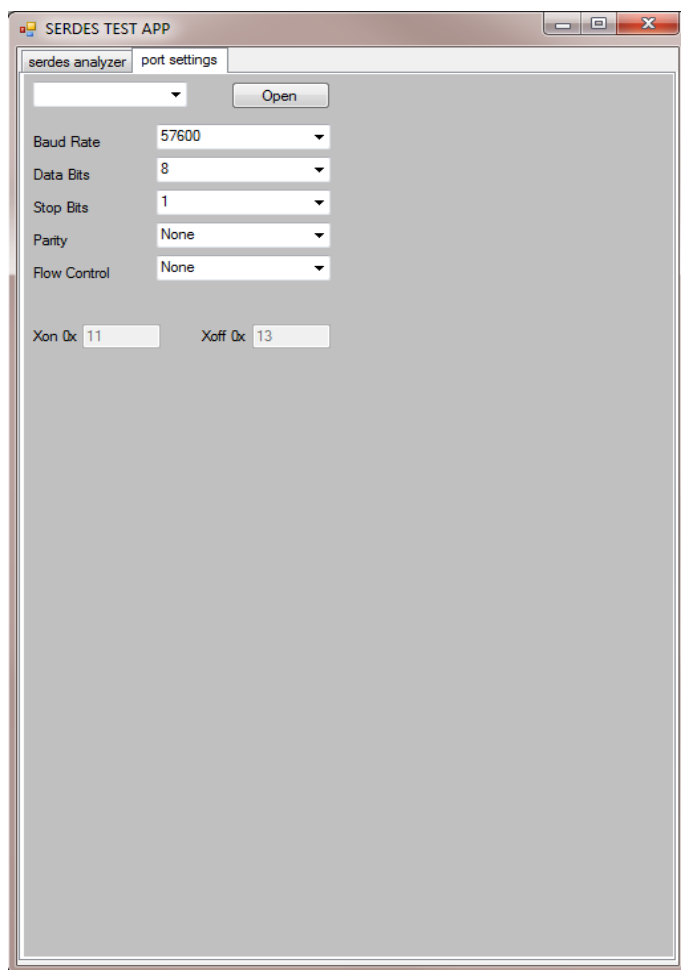


Figure 21 Port Settings Tab

6. Select the highest **COM port** from the drop-down list and click **Open** to establish the connection with the test PC.

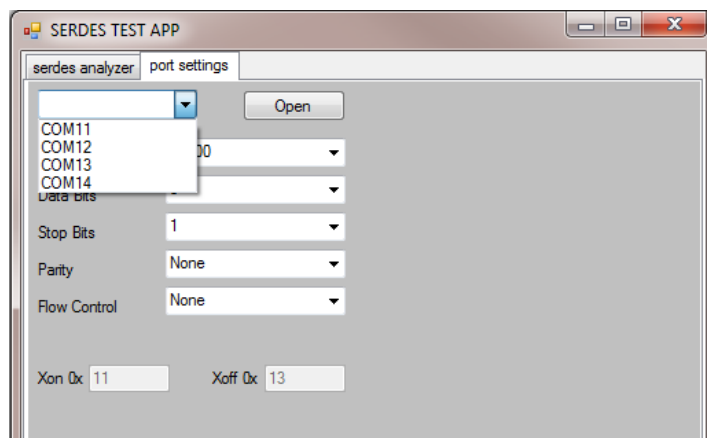


Figure 22 Selecting the COM Port

7. Click the **serdes analyzer** tab to verify the connection.

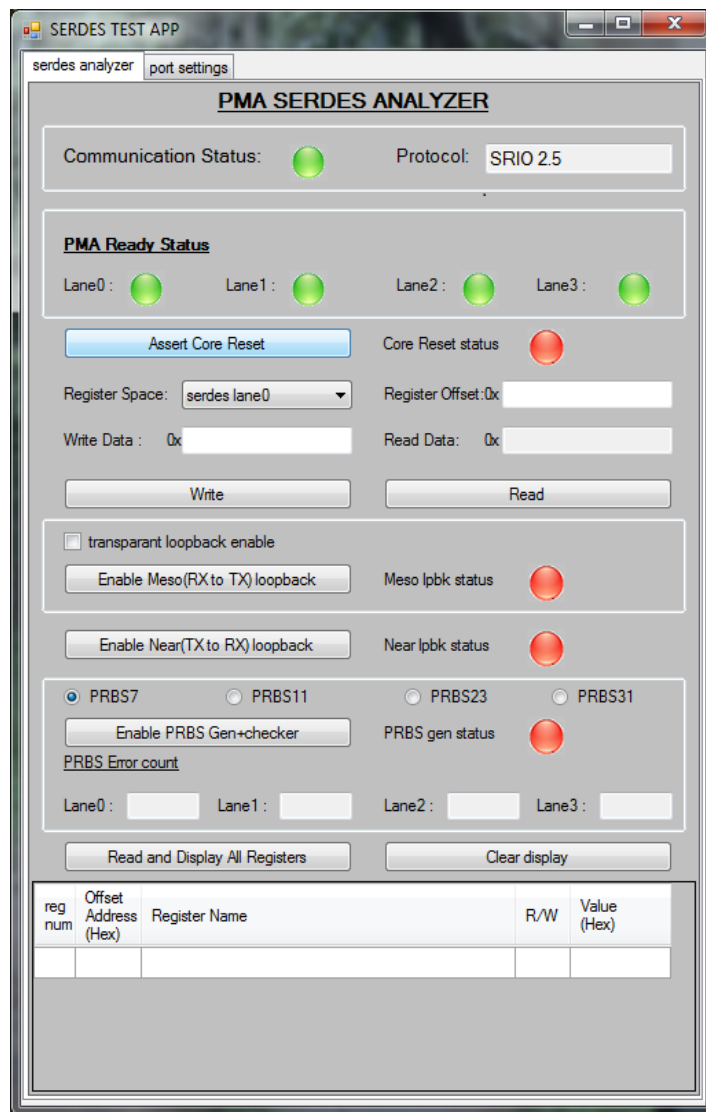


Figure 23 SERDES Analyzer Tab

Make sure that **Communication Status** indicator is in green. If the UART communication is not set up properly, Communication Status indicator will be in red.

Note: If the **Core Reset status** indicator is shown in green, click **Deassert Core Reset** to disable the core reset.

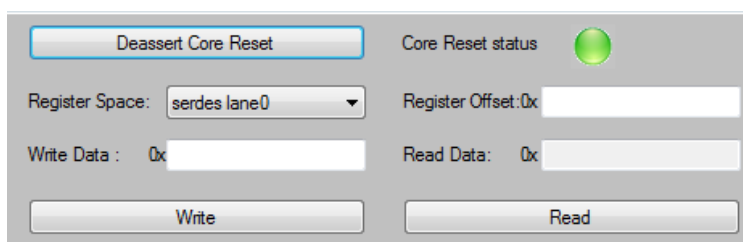


Figure 24 Deasserting Core Reset

8. Select **serdes lane0** from the **Register Space** drop-down list.

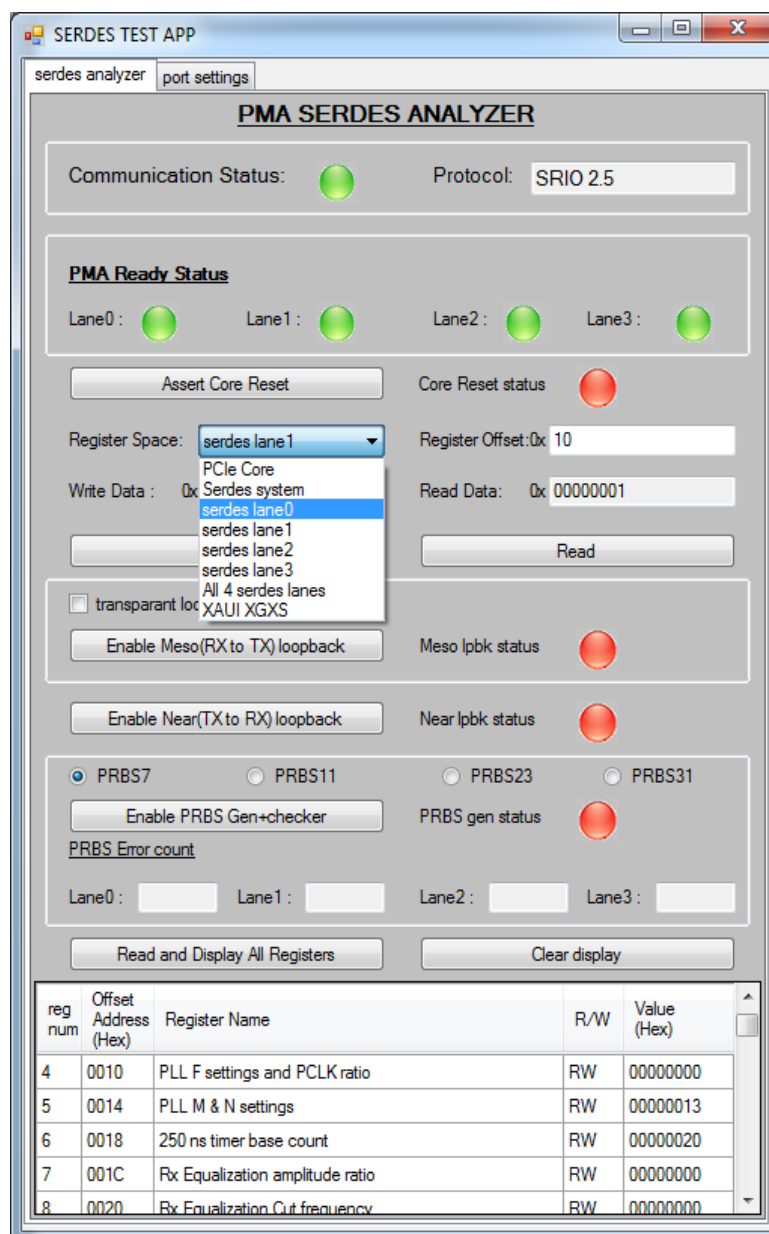


Figure 25 Selecting Register Space

9. In **serdes analyzer** tab, write **10** in **Register Offset** and write **1** in **Write Data** and click **Write**.

The screenshot shows the 'serdes analyzer' tab with the 'PMA SERDES ANALYZER' title. The 'Communication Status' is green and 'Protocol' is 'SRI0 2.5'. Under 'PMA Ready Status', all four lanes (Lane0, Lane1, Lane2, Lane3) are green. The 'Assert Core Reset' button is visible. The 'Register Space' is set to 'serdes lane0'. The 'Register Offset:0x' field is set to '10' and the 'Write Data : 0x' field is set to '1'. Both fields are highlighted with red boxes. The 'Write' button is also highlighted with a red box. The 'Read Data: 0x' field shows '00000001'. At the bottom, there is a checkbox for 'transparent loopback enable' and a button for 'Enable Meso(RX to TX) loopback'. The 'Core Reset status' and 'Meso lpbk status' are both red.

Figure 26 Entering values in Register Offset and Write Data

10. In **serdes analyzer** tab, write **14** in **Register Offset** and write **13** in **Write Data** and click **Write**.

This screenshot is a zoomed-in view of the 'PMA SERDES ANALYZER' interface. It shows the 'Register Space' set to 'serdes lane0'. The 'Register Offset:0x' field is set to '14' and the 'Write Data : 0x' field is set to '13'. Both fields are highlighted with red boxes. The 'Write' button is also highlighted with a red box. The 'Read Data: 0x' field is empty. The 'Core Reset status' and 'Meso lpbk status' are both red.

Figure 27 Entering values in Register Offset and Write Data

Note: By writing values on these register, we are setting up selected SEREDS lane to 5 GBPS mode. This exercise need to be done for every lane (that is, Lane 0, Lane 1, Lane 2, and Lane 3) to enable data rate of 5 GPBS on different lane.

10. Click **Enable Near(TX to RX) loopback** to enable the internal near end loopback on SERDES Lane0.

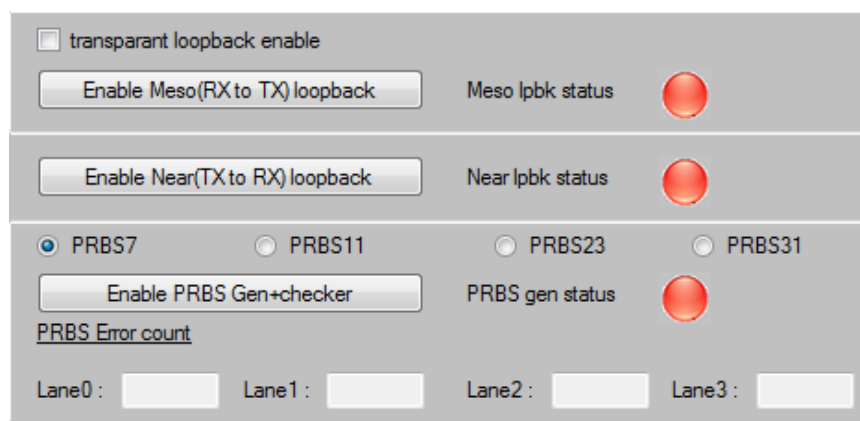


Figure 28 Enabling Internal Loopback

Figure 29 shows Near loopback (lpbk) status indicator in green after clicking **Enable Near(TX to RX) loopback**.

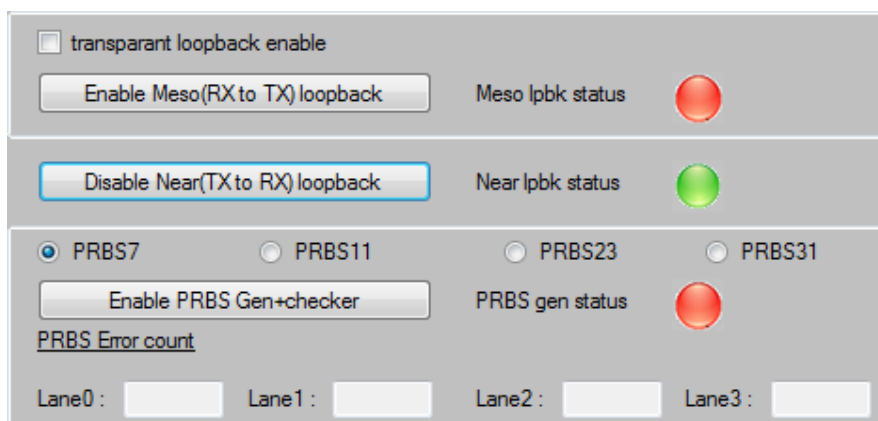


Figure 29 Enabled Internal Loopback

11. Click **Enable PRBS Gen+checker** to enable PRBS check.

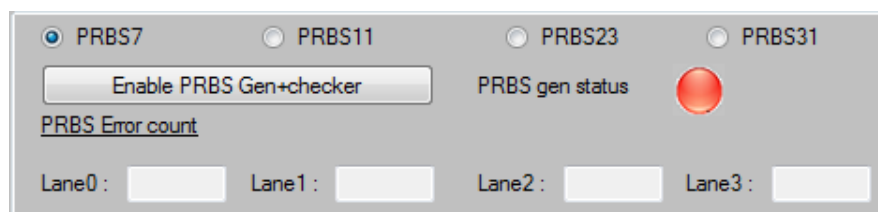


Figure 30 Enabling PRBS Generator

Figure 31 shows **PRBS gen status** indicator in green after clicking **Enable PRBS Gen+checker**.

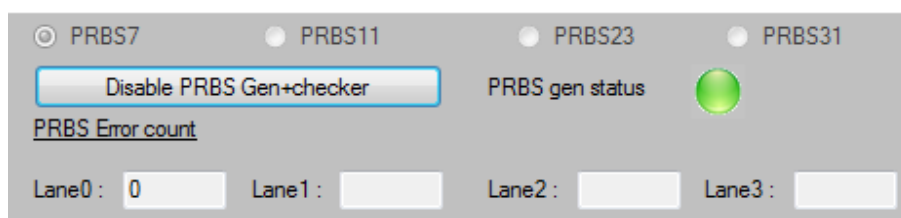


Figure 31 Enabling PRBS Pattern Generation

Once the **PRBS Gen+Checker** is enabled, observe the PRBS error count for Lane 0. It should be 0. 0 on PRBS error count shows that the internal loopback test is successful for SERDES lane 0. Value other than 0 indicated that the internal loopback test is not successful and it has the number of errors it shown.

12. Click **Disable PRBS Gen +checker** to stop the packet transmission and click **Disable Near (TX to RX) loopback** to disable the loopback. After clicking, **Near LPBK status** and **PRBS gen status** indicators change to red. Figure 32 shows Disabled Internal Loopback.

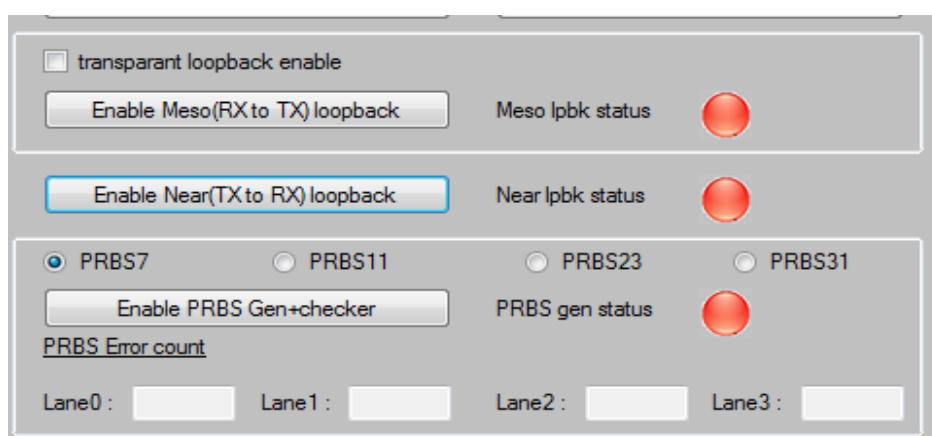


Figure 32 Disabling Internal Loopback

After testing internal loopback on SERDES Lane0, repeat the same test for other three SERDES lanes that is Lane 1, Lane 2, and Lane 3 by selecting the Lane from **Register Space** drop-down list.

Note: Make sure every time after selecting different lane on **Register Space** tab we need to update register values to enable 5GBPS data rates on different SERDES lanes as shown below.

External Loopback on SERDES Lane

External loopback can be performed on SERDES Lane 1 and Lane 2 only.

Note: Switch off the board and give the following connections and switch on the board:

- SMA connector J20 and J15 are shorted using SMA Cable.
 - SMA connector J16 and J10 are shorted using SMA Cable.
1. Select **serdes lane1** from the **Register Space** drop-down list.

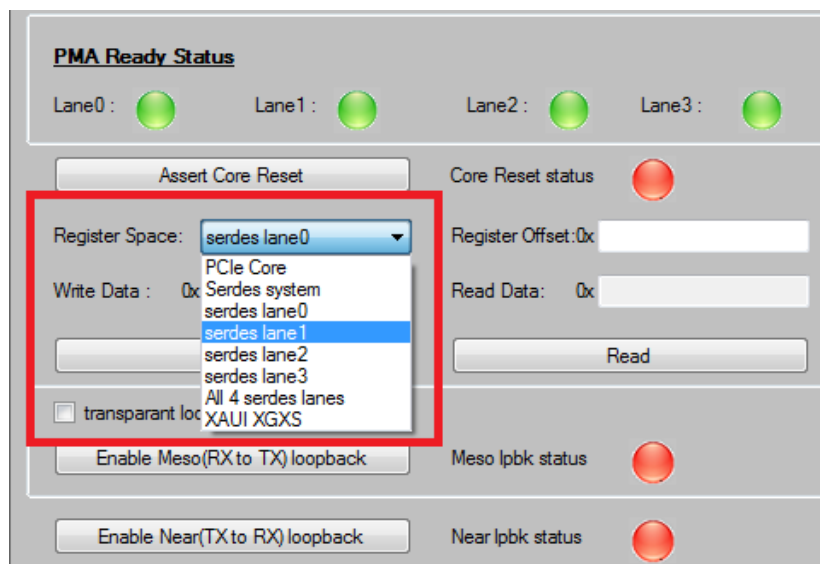


Figure 33 Selecting SERDES Lane 1

On **Register Offset** tab write **10** and on **Write Data** tab write **1** and click on **Write** tab.

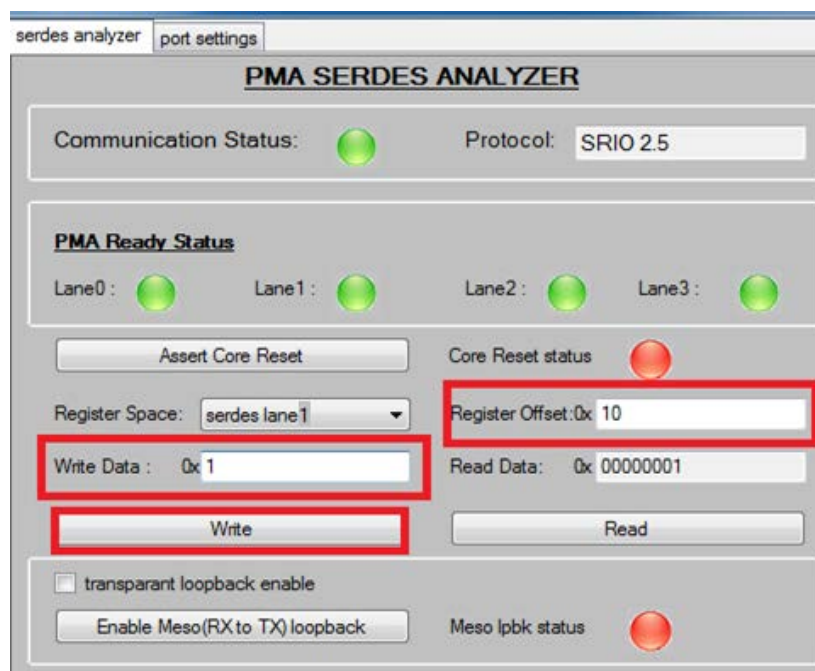


Figure 34 Writing Registers 1

Now On **Register Offset** tab write **14** and on **Write Data** tab write **13** and click on **Write** tab.



Figure 35 Writing Registers 2

2. Click **Enable PRBS Gen+checker** to check the error count.

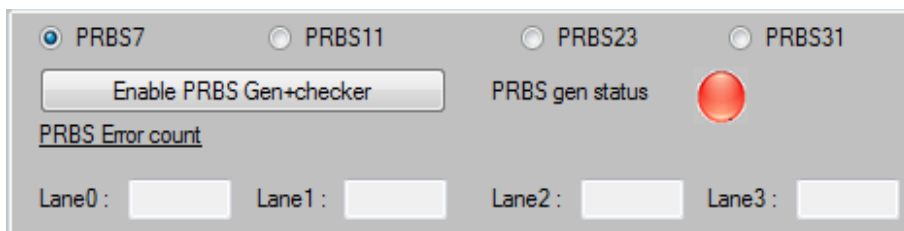


Figure 36 Enabling PRBS Generator

[Figure 37](#) shows **PRBS gen status** indicator in green after clicking **Enable PRBS Gen+checker**.

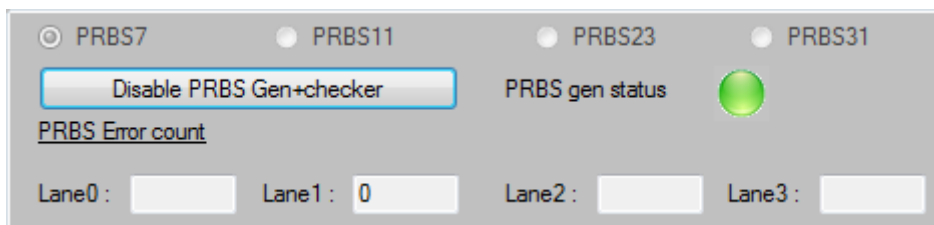


Figure 37 Enabling PRBS Pattern Generation

Once the **PRBS Gen+checker** is enabled, observe the PRBS error count for Lane1. It should be 0. If PRBS error count shows 0, the external loopback test is successful for SERDES Lane 1. Value other than 0 indicated that the external loopback test is not successful and it has the number of errors it shown. After testing interface loopback on SERDES Lane 1, repeat the same test for Lane 2 by selecting lane on register space tab. Repeat all steps as done for lane1 test.

3. Close **SERDES TEST APP** window once the test is completed.

Setting up the Test Terminal for MTD

Note: Make sure the GUI for SERDES test is closed before opening HyperTerminal application for MTD.

1. Open the Windows **start** menu. Click on **All Programs, Accessories, Communications**, and then select the **HyperTerminal** program. This will open HyperTerminal window.

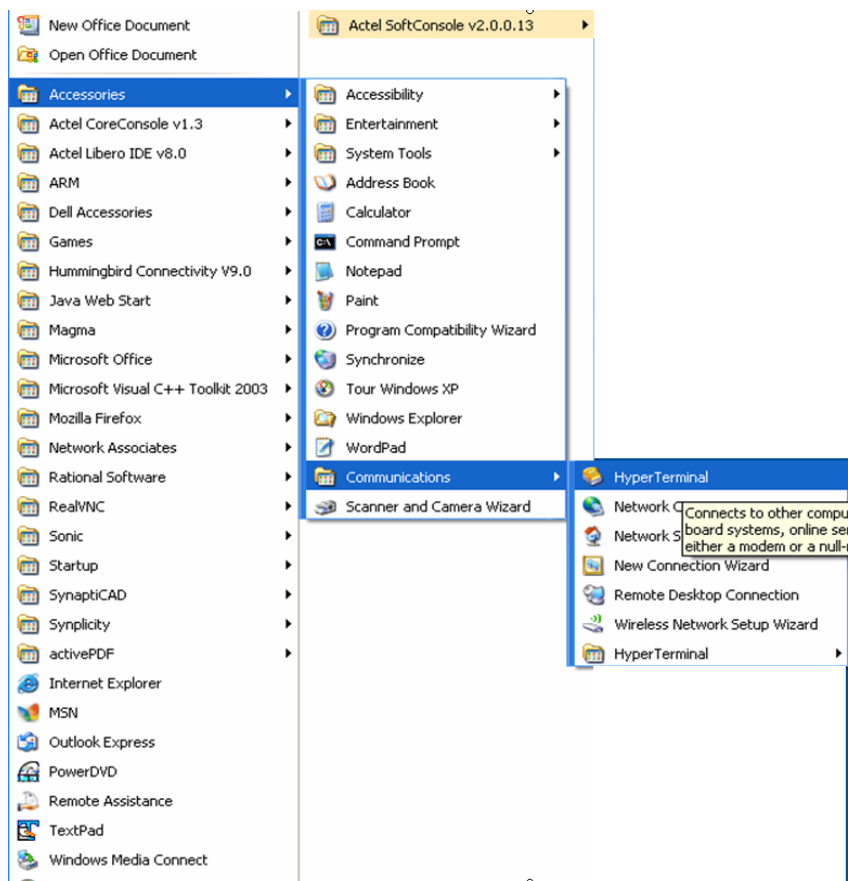


Figure 38 Opening HyperTerminal window

The **Connection Description** window will open. Type in **M2S-EVAL-KIT-MTD** as the name of the new HyperTerminal session and click **OK**.

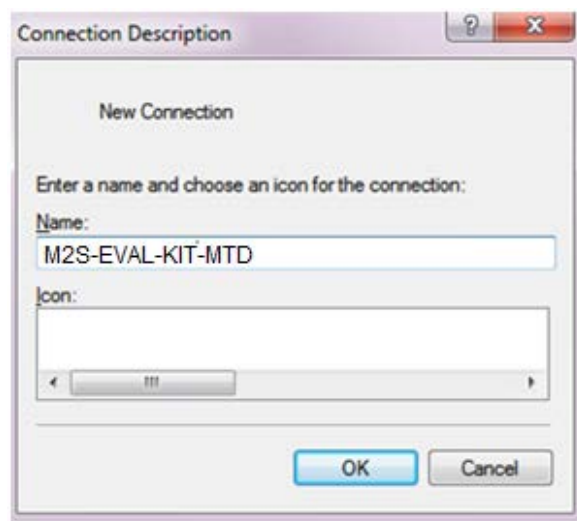


Figure 39 Connection Naming

2. The **Connect To** window will open. Select the **COM port** for serial connection.

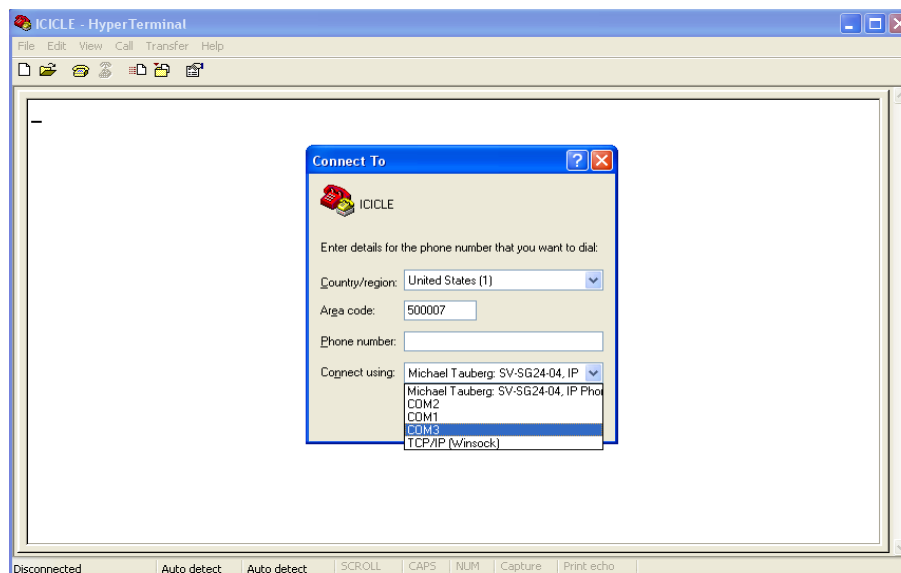


Figure 40 Selecting COM Port

Note:

- Selection of COM port may vary from PC to PC. When using USB cable for HyperTerminal communication, 4 COM port prompts on connection menu, select the last com port out of the 4 COM port appears, to establish connection with test PC.
- Make sure the GUI for SERDES test is closed before opening Hyperterminal application for MTD.

3. The **COM port Properties** window will appear. Select the following settings:
Bits per second = 57600 Data bits = 8, Parity = None, Stop bits = 1, Flow Control = None

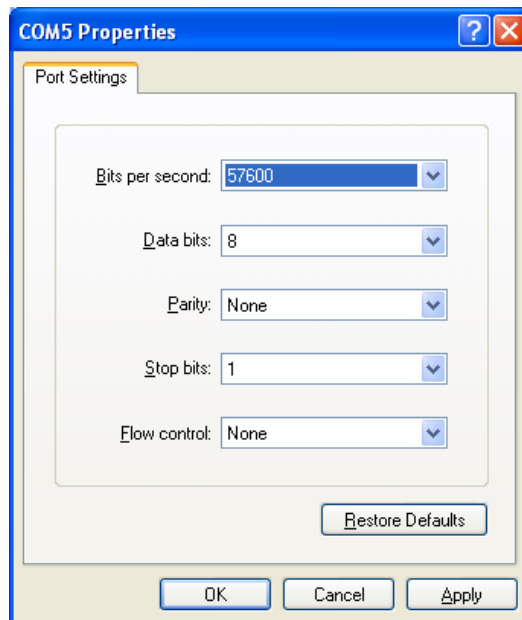


Figure 41 Port Setting

4. Click **OK** to keep the settings.
5. Select **File→ Properties** on the **HyperTerminal** window.
6. Click **ASCII Setup** in the **Settings** tab.

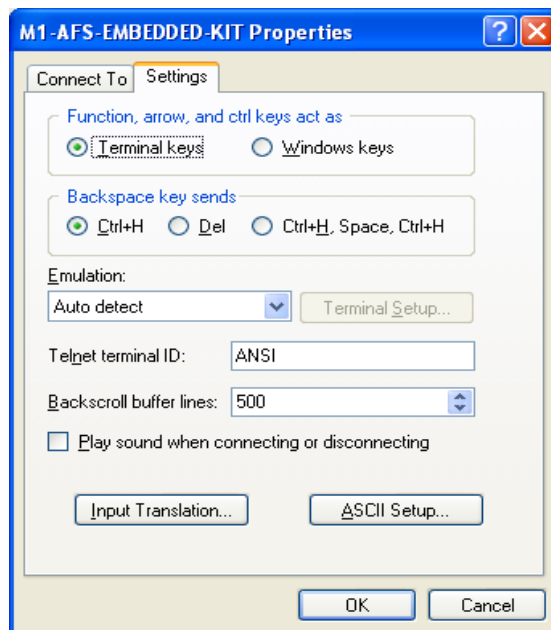


Figure 42 Setting Properties

7. Check the box labeled **Append line feeds to incoming line ends**.

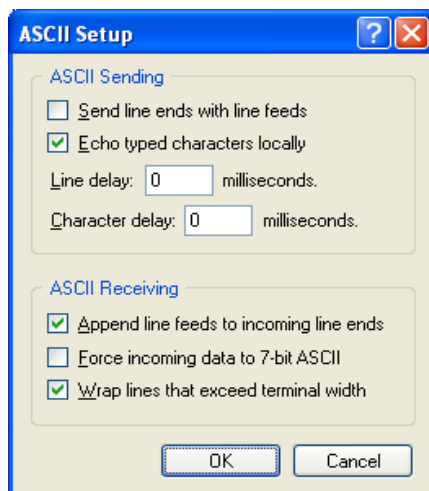


Figure 43 Enabling Local Echo

Running the MTD Test on M2S-EVAL-KIT

- Program the EVAL KIT with SF2_SGMII_MDDR_top.stp file using FlashPro 4 software.
- Make sure all the jumper set-up and jumper setting are placed as explained in the [Requirements to Run EVAL KIT MTD Test](#) section.
- Make sure network cable is connected to J13 (RJ 45 connector) and all the jumper are in place explained in the [SGMII test](#) section.

Test Procedure

Press the Reset Switch SW6 on the M2S-EVAL-KIT to reset the board and start the test program. Following menu will appear.

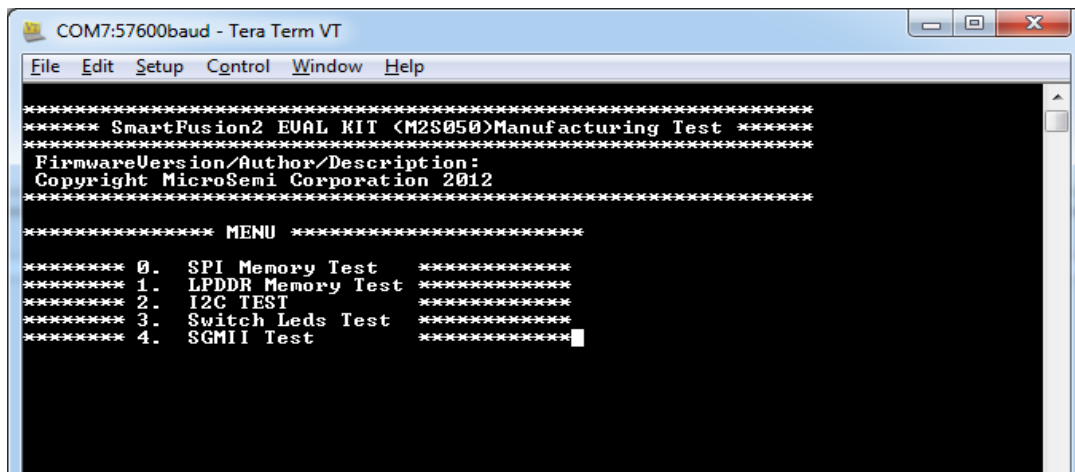


Figure 44 MTD Test Menu

Note: If this message does not appear, then try pressing button SW6 again. If the above message still does not appear, then check all the jumper setting and the hyper terminal has been setup correctly. Power cycles the board again.

Press 0 into the terminal to begin the SPI memory test. The following screen will appear.

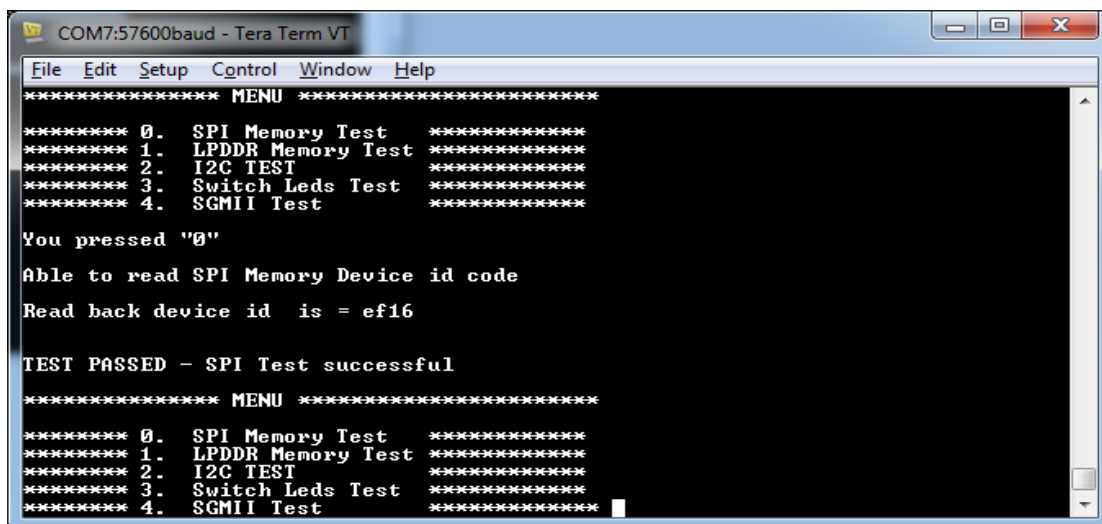
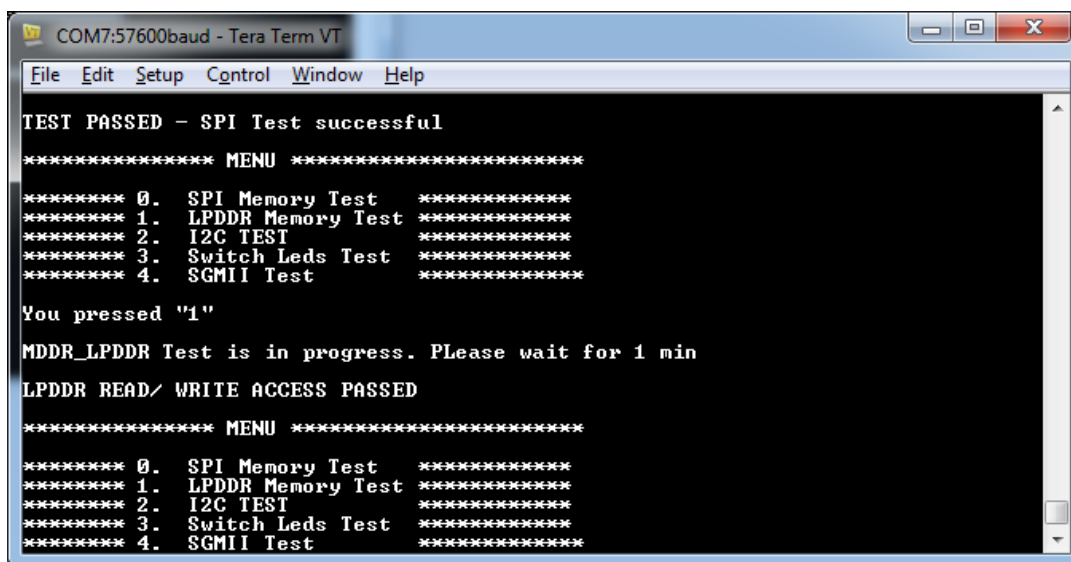


Figure 45 SPI Memory Test

Press 1 into the terminal to begin the LPDDR memory test. The following screen will appear.



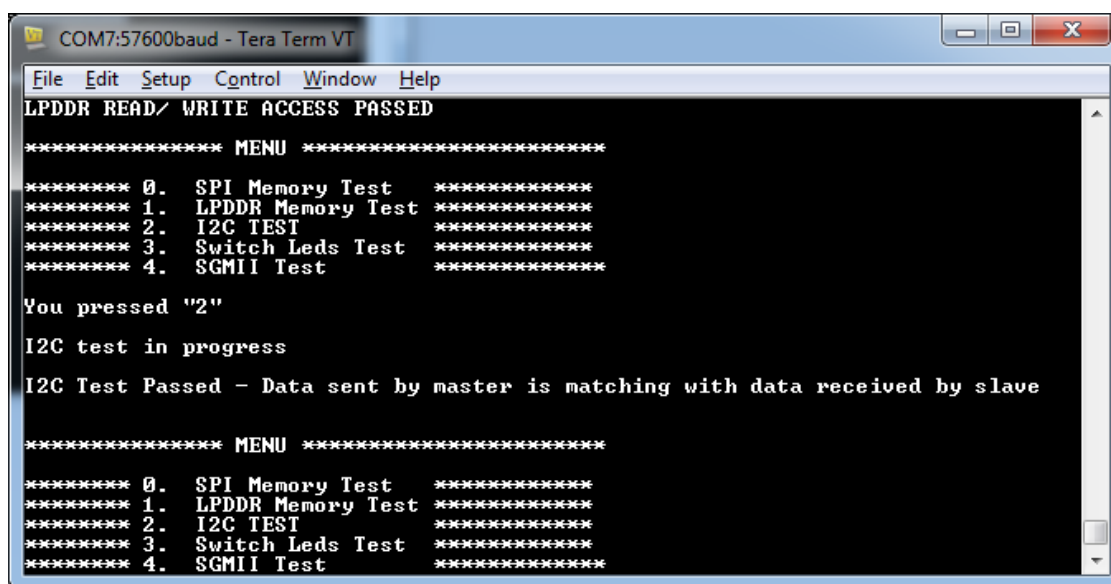
```

COM7:57600baud - Tera Term VT
File Edit Setup Control Window Help
TEST PASSED - SPI Test successful
***** MENU *****
***** 0. SPI Memory Test *****
***** 1. LPDDR Memory Test *****
***** 2. I2C TEST *****
***** 3. Switch Leds Test *****
***** 4. SGMII Test *****
You pressed "1"
MDDR_LPDDR Test is in progress. Please wait for 1 min
LPDDR READ/ WRITE ACCESS PASSED
***** MENU *****
***** 0. SPI Memory Test *****
***** 1. LPDDR Memory Test *****
***** 2. I2C TEST *****
***** 3. Switch Leds Test *****
***** 4. SGMII Test *****

```

Figure 46 LPDDR Memory Test Press 2

into the terminal to begin the I2C test. The following screen will appear.



```

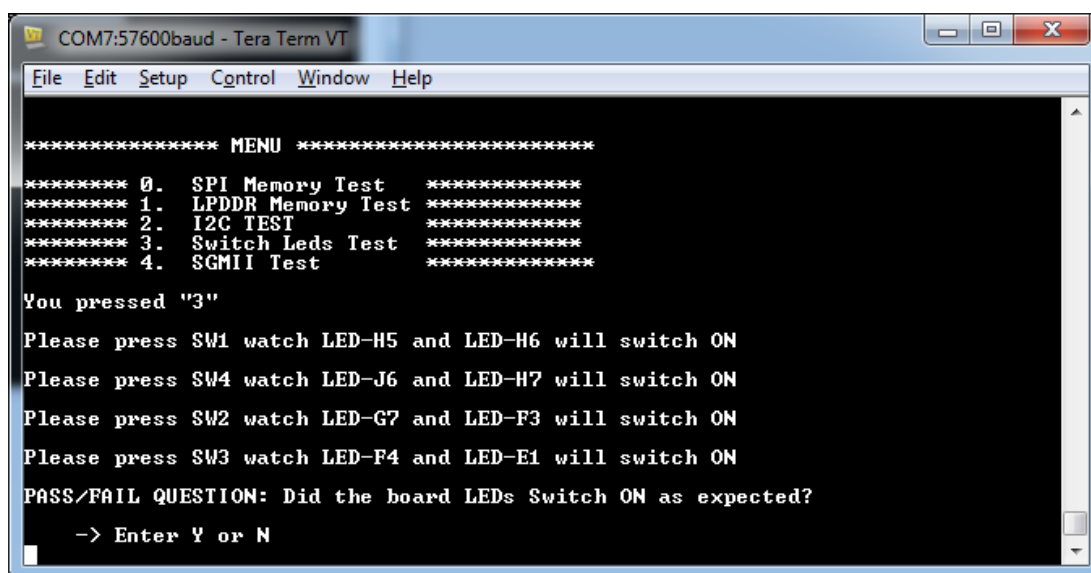
COM7:57600baud - Tera Term VT
File Edit Setup Control Window Help
LPDDR READ/ WRITE ACCESS PASSED
***** MENU *****
***** 0. SPI Memory Test *****
***** 1. LPDDR Memory Test *****
***** 2. I2C TEST *****
***** 3. Switch Leds Test *****
***** 4. SGMII Test *****
You pressed "2"
I2C test in progress
I2C Test Passed - Data sent by master is matching with data received by slave
***** MENU *****
***** 0. SPI Memory Test *****
***** 1. LPDDR Memory Test *****
***** 2. I2C TEST *****
***** 3. Switch Leds Test *****
***** 4. SGMII Test *****

```

Figure 47 I2C Test

Note: In case test failure message appears, please make sure jumper H1 pin 6-10 and pin 7-11 positions are shorted properly.

Press 3 into the terminal to begin the Switch LEDs test. The following screen will appear.



```

COM7:57600baud - Tera Term VT
File Edit Setup Control Window Help

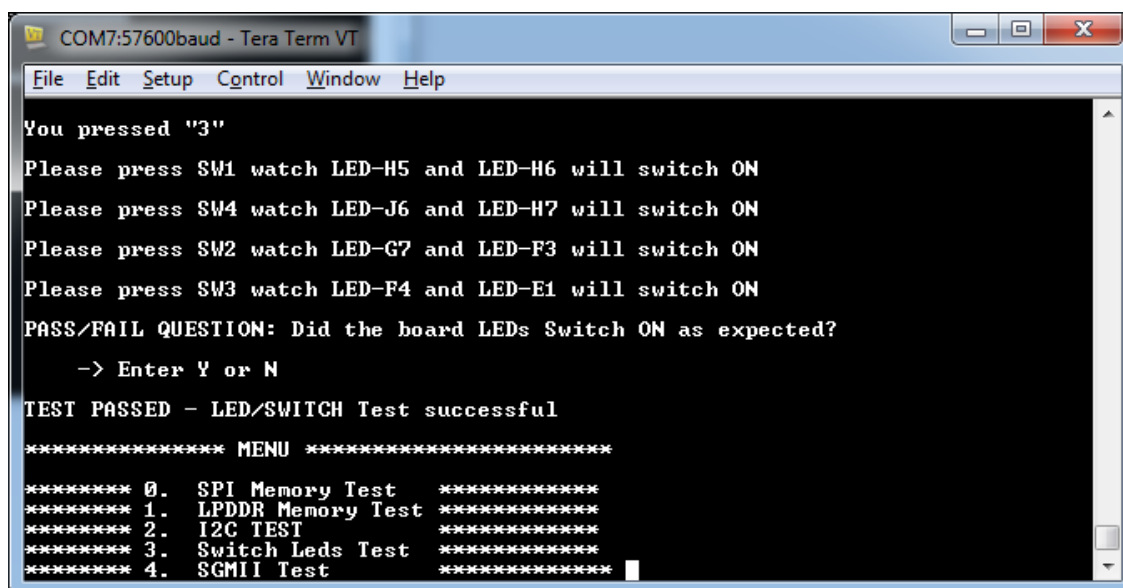
***** MENU *****
***** 0. SPI Memory Test *****
***** 1. LPDDR Memory Test *****
***** 2. I2C TEST *****
***** 3. Switch Leds Test *****
***** 4. SGMII Test *****

You pressed "3"

Please press SW1 watch LED-H5 and LED-H6 will switch ON
Please press SW4 watch LED-J6 and LED-H7 will switch ON
Please press SW2 watch LED-G7 and LED-F3 will switch ON
Please press SW3 watch LED-F4 and LED-E1 will switch ON
PASS/FAIL QUESTION: Did the board LEDs Switch ON as expected?
-> Enter Y or N
  
```

Figure 48 Switch LEDs Test - Step1

Press the switch as instructed and observed the behavior of LEDs. If you observed the same behavior as mentioned on terminal message, enter Y in the terminal window and following window will appear.



```

COM7:57600baud - Tera Term VT
File Edit Setup Control Window Help

You pressed "3"

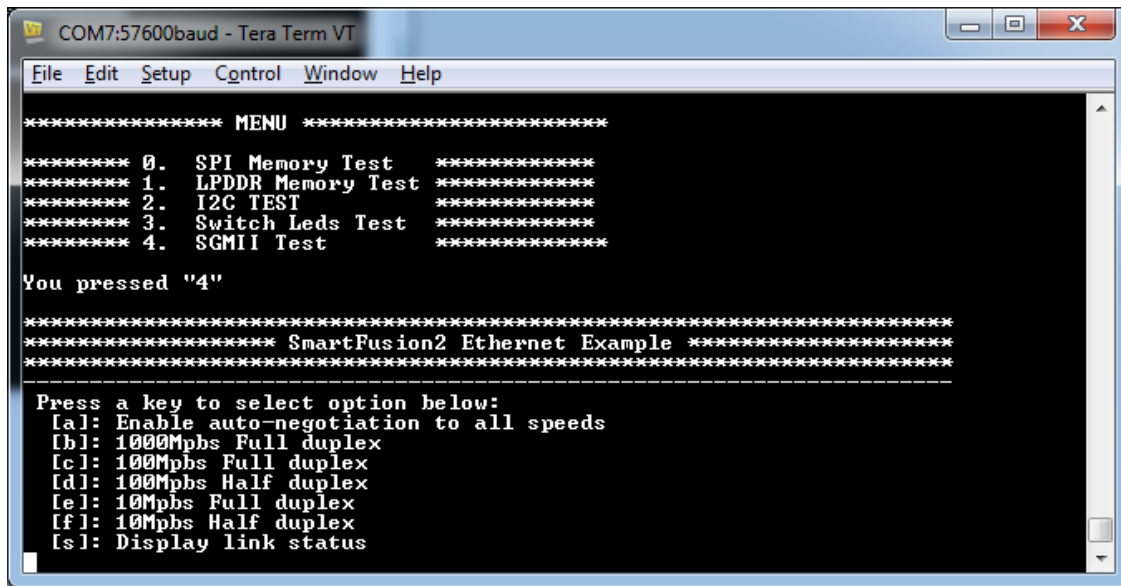
Please press SW1 watch LED-H5 and LED-H6 will switch ON
Please press SW4 watch LED-J6 and LED-H7 will switch ON
Please press SW2 watch LED-G7 and LED-F3 will switch ON
Please press SW3 watch LED-F4 and LED-E1 will switch ON
PASS/FAIL QUESTION: Did the board LEDs Switch ON as expected?
-> Enter Y or N

TEST PASSED - LED/SWITCH Test successful

***** MENU *****
***** 0. SPI Memory Test *****
***** 1. LPDDR Memory Test *****
***** 2. I2C TEST *****
***** 3. Switch Leds Test *****
***** 4. SGMII Test *****
  
```

Figure 49 Switch LEDs Test - Step2

Press 4 into the terminal to begin the SGMII test. After few seconds, the following message will display.

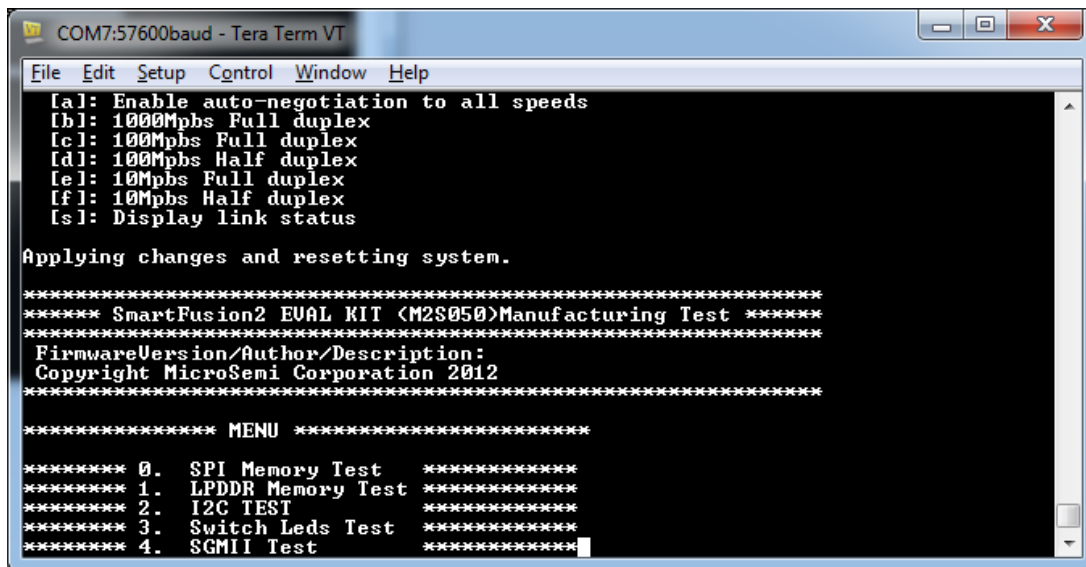


```

COM7:57600baud - Tera Term VT
File Edit Setup Control Window Help
***** MENU *****
***** 0. SPI Memory Test *****
***** 1. LPDDR Memory Test *****
***** 2. I2C TEST *****
***** 3. Switch Leds Test *****
***** 4. SGMII Test *****
You pressed "4"
***** SmartFusion2 Ethernet Example *****
-----
Press a key to select option below:
[a]: Enable auto-negotiation to all speeds
[b]: 1000Mbps Full duplex
[c]: 100Mbps Full duplex
[d]: 100Mbps Half duplex
[e]: 10Mbps Full duplex
[f]: 10Mbps Half duplex
[s]: Display link status
  
```

Figure 50 SGMII Test-Step1

Press **a** on terminal window. Following message will appear. Pressing **a** resets the terminal and the main menu reappears on terminal window as shown below.

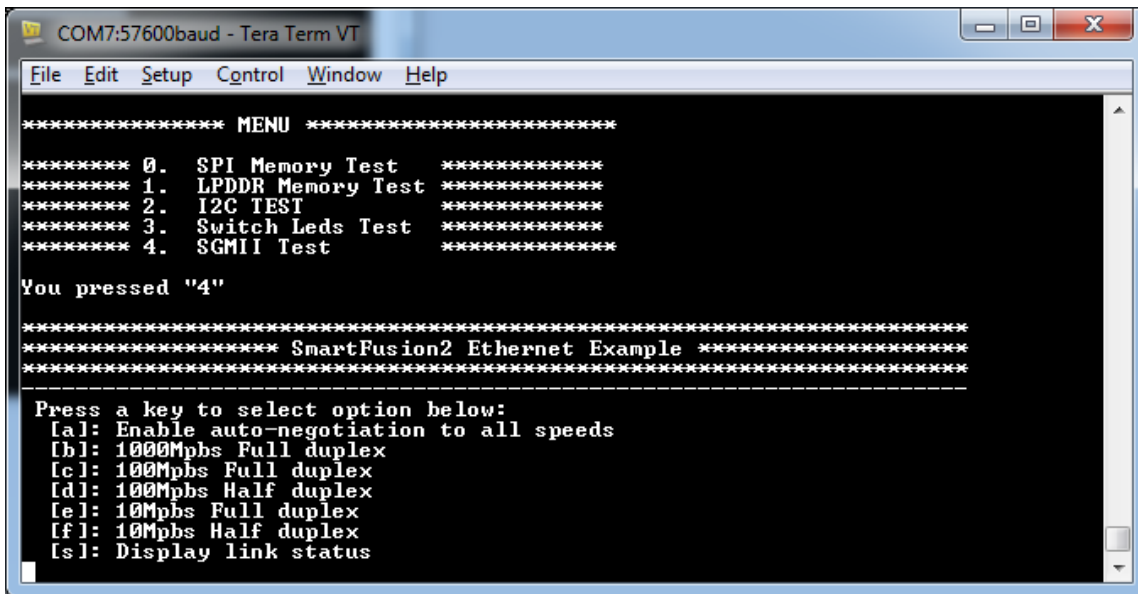


```

COM7:57600baud - Tera Term VT
File Edit Setup Control Window Help
[a]: Enable auto-negotiation to all speeds
[b]: 1000Mbps Full duplex
[c]: 100Mbps Full duplex
[d]: 100Mbps Half duplex
[e]: 10Mbps Full duplex
[f]: 10Mbps Half duplex
[s]: Display link status
Applying changes and resetting system.
***** SmartFusion2 EVAL KIT <M2S050>Manufacturing Test *****
***** FirmwareVersion/Author/Description: *****
***** Copyright MicroSemi Corporation 2012 *****
***** MENU *****
***** 0. SPI Memory Test *****
***** 1. LPDDR Memory Test *****
***** 2. I2C TEST *****
***** 3. Switch Leds Test *****
***** 4. SGMII Test *****
  
```

Figure 51 SGMII Test-Step2

Press 4 again on **terminal** window. Following message will appear.



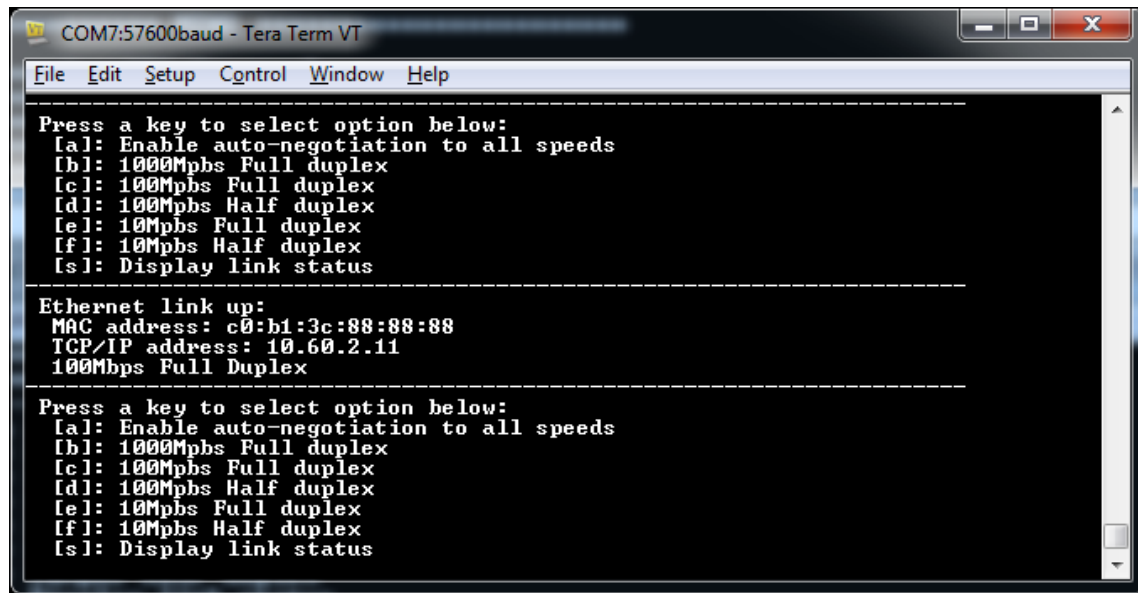
```

COM7:57600baud - Tera Term VT
File Edit Setup Control Window Help
***** MENU *****
***** 0. SPI Memory Test *****
***** 1. LPDDR Memory Test *****
***** 2. I2C TEST *****
***** 3. Switch Leds Test *****
***** 4. SGMII Test *****
You pressed "4"
***** SmartFusion2 Ethernet Example *****
*****
Press a key to select option below:
[a]: Enable auto-negotiation to all speeds
[b]: 1000Mbps Full duplex
[c]: 100Mbps Full duplex
[d]: 100Mbps Half duplex
[e]: 10Mbps Full duplex
[f]: 10Mbps Half duplex
[s]: Display link status
  
```

Figure 52 SGMII Test-Step3

Wait for few seconds (approx-5 Seconds) and the press **s** into the **terminal** window to get MAC and IP address.

[Figure 53](#) shows the message that appears on terminal window.



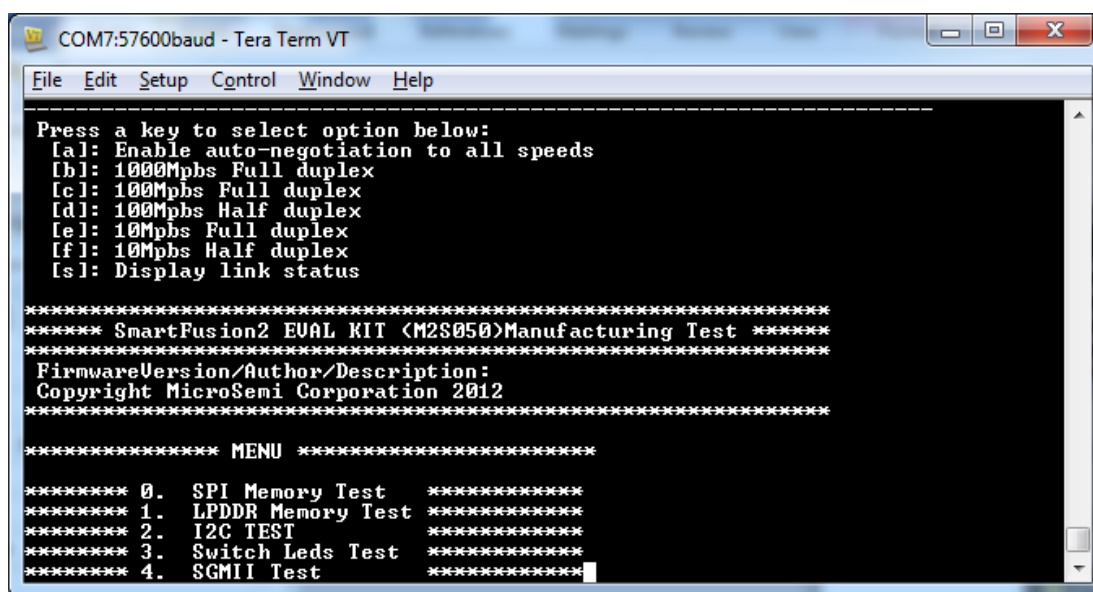
```

COM7:57600baud - Tera Term VT
File Edit Setup Control Window Help
-----
Press a key to select option below:
[a]: Enable auto-negotiation to all speeds
[b]: 1000Mbps Full duplex
[c]: 100Mbps Full duplex
[d]: 100Mbps Half duplex
[e]: 10Mbps Full duplex
[f]: 10Mbps Half duplex
[s]: Display link status
-----
Ethernet link up:
MAC address: c0:b1:3c:88:88:88
TCP/IP address: 10.60.2.11
100Mbps Full Duplex
-----
Press a key to select option below:
[a]: Enable auto-negotiation to all speeds
[b]: 1000Mbps Full duplex
[c]: 100Mbps Full duplex
[d]: 100Mbps Half duplex
[e]: 10Mbps Full duplex
[f]: 10Mbps Half duplex
[s]: Display link status
  
```

Figure 53 SGMII Test-Step4

Note: IP address may vary from PC to PC. It may not be the same as appears on the snapshot.

Press **Reset** (SW6) to switch to main menu. After pressing SW6, main test window will appear.



```

COM7:57600baud - Tera Term VT
File Edit Setup Control Window Help
-----
Press a key to select option below:
[a]: Enable auto-negotiation to all speeds
[b]: 1000Mbps Full duplex
[c]: 100Mbps Full duplex
[d]: 100Mbps Half duplex
[e]: 10Mbps Full duplex
[f]: 10Mbps Half duplex
[s]: Display link status

*****
***** SmartFusion2 EVAL KIT (M2S050)Manufacturing Test *****
*****
FirmwareVersion/Author/Description:
Copyright MicroSemi Corporation 2012
*****

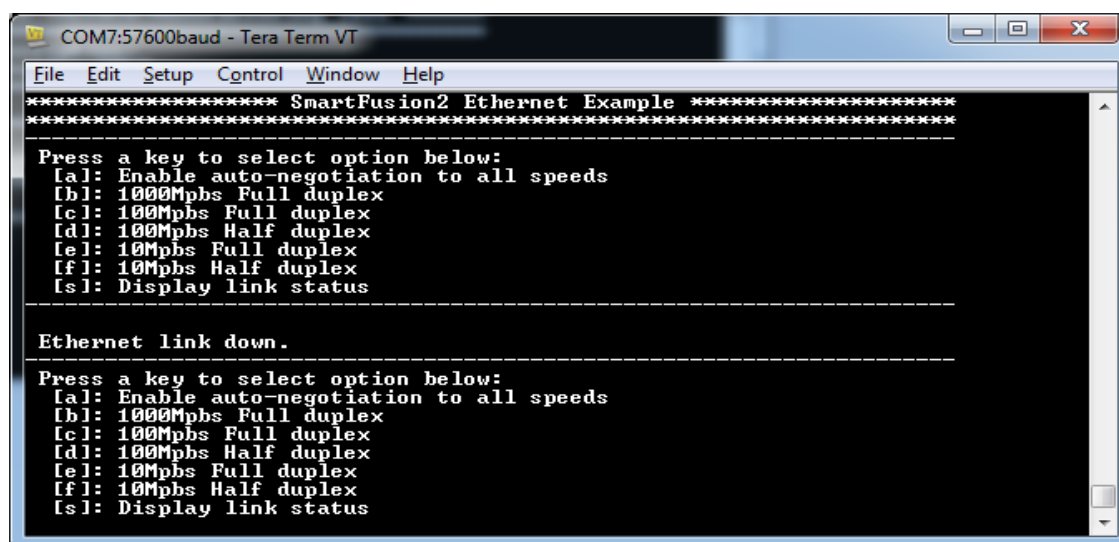
***** MENU *****

***** 0. SPI Memory Test *****
***** 1. LPDDR Memory Test *****
***** 2. I2C TEST *****
***** 3. Switch Leds Test *****
***** 4. SGMII Test *****

```

Figure 54 SGMII Test-Step5

Note: While running SGMII test, if the link-up is not proper below message will appear.



```

COM7:57600baud - Tera Term VT
File Edit Setup Control Window Help
-----
***** SmartFusion2 Ethernet Example *****
*****
Press a key to select option below:
[a]: Enable auto-negotiation to all speeds
[b]: 1000Mbps Full duplex
[c]: 100Mbps Full duplex
[d]: 100Mbps Half duplex
[e]: 10Mbps Full duplex
[f]: 10Mbps Half duplex
[s]: Display link status

-----
Ethernet link down.
-----
Press a key to select option below:
[a]: Enable auto-negotiation to all speeds
[b]: 1000Mbps Full duplex
[c]: 100Mbps Full duplex
[d]: 100Mbps Half duplex
[e]: 10Mbps Full duplex
[f]: 10Mbps Half duplex
[s]: Display link status

```

Figure 55 SGMII Test-Error Message

In case of this error make sure

- Ethernet cable is connected properly to J13.
- Jumper J22,J23 are shorted to **1-2** Position
- Rerun the SGMII test as explained above.

Switches and LED Tests

Use the following switches to test the corresponding LED:

- Press SW6, H5 LED must glow.
- Press SW7, H6 LED must glow.
- Press SW4, J6 LED must glow.
- Press SW3, H7 LED must glow.

Debugging the Board

If the board is not programmed successfully, check if all the required power supplies, clocks, and reset signals are within the accepted range or not.

Power Supply Validation

1. Check for all default jumper settings as per [Table 4 on page 9](#).
2. After power **ON**, power supplies with respect to the ground must be measured and the range must be as listed in [Table 15](#).

Table 15 Power Supply Range

Power Rail	Probing Point	Accepted Voltage Range. (in Volt)
1P2V	C95 Pin 2	1.15<VDD_REG<1.25
5P0V	C16 pin 2	4.75<5P0V<5.25
3P3V	C76 pin 2	3.15<3P3V<3.46
2P5V	C107 pin 2	2.375<2P5V<2.625
3P3V_LDO	C99 pin 1	3.135<3P3V_LDO<3.465
2P5V_LDO	C100 pin 1	2.375<2P5V_LDO<2.625
DDR_VTT	C22 pin 1	0.88<DDR3_VTT<.92
1P0V_PHY	C36 pin 1	0.95<1P0V_PHY<1.05
1P8V	C31 pin 1	1.78<1P8V<1.82

3. LEDs (top left of board) corresponding to their respective power rails must glow.
4. Ripples on power rails should be within $\pm 5\%$ of respective voltage rail.

Clock Measurement

Measure clock signal at Y2 pin 3 and ensure that the stable 50 MHz signal is available.

Reset Measurement

Measure reset signal at resistor R14 and ensure that this is 3.3 V and held High.

FPGA Programming

Check whether SmartFusion2 has been successfully programmed through the JTAG interface.

Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call **800.262.1060**

From the rest of the world, call **650.318.4460**

Fax, from anywhere in the world **408.643.6913**

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Microsemi SoC Products Group Customer Support website for more information and support (<http://www.microsemi.com/soc/support/search/default.aspx>). Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on website.

Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group [home page](http://www.microsemi.com/soc/), at <http://www.microsemi.com/soc/>.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the TechnicalSupport Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to [My Cases](#).

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. [Sales office listings](#) can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within [My Cases](#), select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the [ITAR](#) web page.



Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor solutions for: aerospace, defense and security; enterprise and communications; and industrial and alternative energy markets. Products include high-performance, high-reliability analog and RF devices, mixed signal and RF integrated circuits, customizable s, FPGAs, and complete subsystems. Microsemi is headquartered in Aliso Viejo, Calif. Learn more at www.microsemi.com.

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