

Six Output Programmable LED Current Sink

PRODUCTION DATA SHEET

DESCRIPTION

LED Display Driver: This six channel current sink driver is ideal for controlling brightness and hue of high quality dimmable LED displays. High accuracy, dual mode dimming, and controlled current switching time provides consistent color hue, at brightness ratios of up to 1000:1, and keeps electro magnetic emissions in check.

Its wide compliance voltage range combined with 43 volt breakdown capability make the LX1991 ideal for automotive in-dash displays.

Precision current control: Precision current mirror circuitry sets all channels to the same current with a single programming input. Sinking current value can be programmed up to 30 mA per channel with a single resistor or potentiometer from I_{SET+} to I_{SET-}. Channel to channel matching is typically within ±1 percent of channel mean at the rated output current.

Dual Mode Dimming: Display dimming can be achieved by controlling either current amplitude or duty cycle, and both methods can be employed at the same time.

1000:1 Dimming Range: The DIG DIM input accepts a TTL or CMOS logic signal that controls duty cycle of the output currents.

Independent Channels: The six channels feature independent regulation with respect to output voltage, so one does not affect the others. Any one or more outputs can be left unloaded without affecting current regulation of the other channels. Multiple channels can also be connected together to sink more current in a single load.

EMI Control: Rise and fall time of sink currents are precisely controlled by placing a capacitor on the SLOPE C pin. Special control circuitry maintains symmetrical rise and fall times, preserving the LX1991's ability to provide accurate output current response to very narrow input pulses on the DIG DIM pin.

Power Handling: The LX1991 is supplied in a 4x4 MLPQ package capable of 1.5 watts dissipation. Logic Enable: A separate input puts the LX1991 to sleep at less than 1 uA IDD.

KEY FEATURES

LX1991

- Six precision independent current sink channels
- Simultaneous Analog and **Digital Dimming Modes**
- Precision programming of current rise & fall times
- 1% band gap reference
- 40 volt rated output stages
- 3V / 5V logic input compatible
- 1.5 watt power dissipation
- On-chip thermal shutdown
- 16 Pin 4 x 4 MLPQ Package

BENEFITS

- Consistent LED color hue results from high current accuracy
- 1000:1 dimming ratio with digital dimming
- Lowered emissions with current slope programming
- Reduced component count for compact designs
- Drive up to 108 colored LED's per IC (6 x 18 @ 2.1 volts)
- Drive up to 60 white or blue LED's per IC (6 x 10 @ 3.8 volts)

IMPORTANT: For the most current data, consult MICROSEMI's website: http://www.microsemi.com



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	ABLE SLOPP ET+	
	16 15 14 13 DIG DIM 1 12 NC	
		٢-
	SINK 1 3 10 SINI	< 6
	SINK 2 4 9 GNE)
	GND SINK SINK	
	(Top View)	
n		
	0	
	MSC	
	1991	
	××××	
	XXXX	

LQ PACKAGE MARKING xxxx Denotes Date Code / Lot Code

RoHS / Pb-free 100% Matte Tin Lead Finish

ABSOLUTE	MAXIMUM	RATINGS

Supply Voltage (VDD)	-0.3v to 6V
Analog Output Voltage (SINK ₁ to SINK ₆)	-0.3V to 43V
Analog Inputs (I _{SET})	-0.3V to VDD +0.5V
Digital Inputs (ENABLE, DIG_DIM)	-0.3V to VDD +0.5V
Operating Temperature Range	-40°C – 85°C
Storage Temperature Range	-65°C – 150°C
Maximum Junction Temperature	150°C
Peak Package Solder Reflow Temp. (40 seconds max. exposure)	

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

THERMAL DATA				
LQ Plastic 4x4 MLPQ 16-Pin				
THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JC}	2.2°C/W			
THERMAL RESISTANCE-JUNCTION TO AMBIENT. θ_{10}	36°C/W			

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$. The θ_{JA} numbers are guidelines for the thermal performance of the device/ 4 layer pcboard system. All of the above assume no ambient airflow. The θ_{JA} numbers are to MIL-STD-883D Method 1012.1

FUNCTIONAL PIN DESCRIPTION

	DESCRIPTION
GND	Ground
V _{DD}	Voltage Input, 4.5 to 5.5V input range. V_{DD} is internally switched (see ENABLE) to remove power from chip.
SINK ₁ – SINK ₆	Current sink channels one through six. Each output sinks the programmed current from the V_{LED} supply to ground. Compliance voltage is from 1 volt minimum to the V_{LED} supply maximum.
DIG_DIM	A logic input that duty cycle modulates the output currents. All output currents are turned on at the programmed current value when DIG_DIM is high and turned off when it is low. Compatible with both 3V and 5V logic.
ENABLE	Chip Enable Input. If logic high, all functions are enabled. If logic low, internal power is disconnected from the V_{DD} pin, disabling all functions. Logic threshold is 1.6 ± 0.8V maximum over supply and temperature range. Maximum current into VDD when ENABLE < 0.4V is 1 μ A.
I _{SET+} I _{SET-}	Current programming resistor pins. Output current in each channel is 24 times the current that flows from I_{SET+} to I_{SET-} I_{SET} current is 1.26V / R_{SET-} Connect resistor between I_{SET+} and I_{SET-}
C _{SLOPE}	Current rise and fall time programming capacitor. Rise and fall times increase in direct proportion to capacitor value. C = $450\mu A * T_R$ or T_F in microseconds, C in picofarads.

PACKAGE DATA



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RECOMMENDED OPERATING CONDITIONS

Parameter		LX1991			
Falameter	Min	Тур	Max	Units	
Supply Voltage (V _{DD})	4.5		5.5	V	
ENABLE Input Voltage	0		V _{DD}	V	
DIG_DIM Input Voltage	0		V _{DD}	V	
C _{SLOPE} Capacitance Range					
I _{SET} Voltage	0		1.26	V	
R _{SET} Current Programming Resistor Range	1		40	ΚΩ	
SINK ₁ To SINK ₆ Output Voltage Range	0.5	3	40*	V	
SINK1 To SINK6 Maximum Output Current			30	mA	

*At output voltages greater than 5V total power dissipation when using all six outputs at maximum current will exceed power rating of package and ambient of 85°C.







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D	0			LX1991		Τ.
Parameter	Symbol	Test Conditions	Min	Typ Max		Ur
POWER					•	_
Power Supply Input Voltage	V _{DD}		4.5	5	5.5	
Quiescent current	I _{DD ON}	VDD = 5V, ENABLE ≥ 2.4V; DIG_DIM ≥ 2.4V		10	16	T
Quiescent current	I _{DD OFF}	VDD = 5V, ENABLE ≥ 2.4V; DIG_DIM ≤ 0.8V		3.6	6	T
Sleep Current ¹	IDD SLEEP	VDD = 5V, V_{OUT} = 40V, ENABLE $\leq 0.4V$		0.08	1	Ť
						_
ENABLE Logic Threshold	V _{TH EN}		0.8	1.6	2.4	Т
Input Current				4.0	10	Ť
Input Current		$V_{\text{ENABLE}} = 0V$		0.4	1	+
OUTPUT CURRENT			1		1	_
SINK x 30mA	SINK 30	$VDD = 5V SINK_{X} = 3V B_{SET} = 1.02KO$	28.4	30	31.6	Т
SINK v 20mA	SINK 20	$VDD = 5V SINK_{x} = 3V R_{SET} = 1.54KO$	19	20	21	t
SINK × 10mA		VDD = 5V SINK = 3V Root = 3.09KO	С	10	11	╈
SINK × 5mA		VDD = 5V, SINK _X = 3V, R _{SET} = 6.19KO	4	5	6	+
SINK - Current Matching ²		$VDD = 5V. SINK_{X} = 1V \text{ to } 5V. R_{SET} = 1.54K\Omega$		±1	±2.5	t
I _{SET} to SINK x Current Ratio		VDD = 5V, SINK _x /I _{SET}		24.5		t
Output Current I _{SET} = 0µA	SINK _{SET0}	$I_{SET} = 0\mu A$		10	100	Ť
Output Current DIG_DIM ≤ 0.8V	SINK _{DIG_DIM0}	R _{SET} = 1.02KΩ; DIG_DIM ≤ 0.8V		10	100	Ť
Dropout Voltage ³	VDROPOUT	SINK _x = 10mA		200	800	
Dropout Voltage ³	VDROPOUT	SINK _x = 30mA		600	1000	
Maximum Output Current, I _{SET} Shorted To Gnd. Each Output	SINK ISETSC	V_{ISET} = Zero Volts; VDD=5V; SINK _X = 5V		50		1
Output Off State Current	SINK X OFF	$ENA \le 0.4V, V_{OUT} = 40V$		1	3	
DIG_DIM INPUT						
DIG_DIM Logic Threshold	V _{TH_DD}		0.8	1.6	2.4	
Input Current, high state	I _{IH DIG_DIM}	$V_{DIG_DINM} = V_{DD}$		50	Ì	Ť
Input Current, low state	I _{IL DIG DIM}	V _{DIG DIM} = 0V		0.1		T
DIG DIM to SINK x Pulse Response		C _{SLOPE} ≤ 20pF		340		Ť
DIG_DIM to SINK x Pulse Response	T _{D(OFF)}	C _{SLOPE} ≤ 20pF		230		Ť
Minimum SINK x Pulse Width	SINK X PWMMIN	$C_{SLOPE} \le 20pF, DIG_DIM \le 5uS$		5		Τ
CURRENT ON / OFF SLOPE						
Current On rise time	T _{RISE}	C _{SLOPE} = 10 nF	15	22	29	
Current On fall time	T _{FALL}	C _{SLOPE} = 10 nF	15	24	29	
Current on / off delay time	T _{delay}	C_{SLOPE} = 10 nF, T_A = 25°C		50		
RSET PIN		•				
Voltage at Pin R _{SET}	V _{RSET}	R _{SET+} = 1.50K to I _{SET-}	1.24	1.26	1.28	Τ
Pin Rost Max Source Current			1	4 5	1	t

² SINK x current matching is greatest percentage delta between output currents with respect to the mean, with $V_{SINK x}$ both at 1V

and 5V and $R_{SET} = 1.54 K\Omega$.

 3 Dropout is defined as the SINK_x to GND voltage at which the output current sink drops 10% from the nominal value.



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THEORY OF OPERATION / APPLICATION NOTE

FUNCTIONAL DESCRIPTION

The LX1991 is designed to drive LED's used in display illumination and signaling applications such as cellular telephones, PDA's automotive dashboard lighting, panel illumination etc. With a single 5V supply, the six independently regulated constant current outputs can drive 6 white LED's ($V_F < 4.0V$), or 12 green or amber LED's ($V_F < 2.0V$ each) arranged as 6 parallel x 2 in series. With a separate high voltage LED supply (up to 40V) a large matrix of LED's (>100) can be driven.

The LX1991 features resistor settable output current. Connecting a resistor between I_{SET+} and I_{SET-} pins generates a current that is mirrored into each of the outputs with a gain ratio of about 24. This ratio remains linear for output currents from 3 to 30mA, at output current less than 3mA the ratio increases somewhat. Output current can be varied in an analog fashion by varying R_{SET} resistor, typically this resistor shall be chosen in the range of 1K to 40K.

Duty cycle dimming with a fixed current amplitude is accomplished by driving the DIG_DIM input. The switching frequency can exceed 100 KHz, making it practical to use a PWM output channel from popular micro controllers. The upper limit on frequency correlates to the minimum DIG_DIM sink pulse width which is typically about 5μ S.

To use the LX1991 at the maximum usable frequency, or minimum pulse width the CSLOPE pin must be open. The CSLOPE pin allows precise control of the sink current rise and fall time. As the value of the CSLOPE capacitor is increased the slope of the rise and fall time will change correspondingly along with some delay to output. Special control circuitry maintains symmetrical rise and fall times, preserving the LX1991's ability to provide accurate output current response to very narrow input pulses on the DIG_DIM pin.

The ENABLE input is TTL compatible with a turn on threshold of about 1.6V with about 150mV of hysteresis. Below 0.8V the chip is disabled and the sink outputs are off. However ENABLE must be driven below 0.4 volts to insure the minimum sleep current from V_{DD} and output off current.

All inputs and outputs are ESD and short circuit protected making the LX1991 an exceptionally robust component. The device also includes thermal shutdown however it is not recommended to short the I_{SET+} and I_{SET-} inputs together while shorting the outputs to 40V as the power dissipation under these conditions is the greatest.

APPLICATION NOTES

POWER CONSIDERATIONS

Each output has an independent current sink, however each must be held above about 600-800mV (typically) to perform properly and maintain the specified current regulation accuracy. The device is designed however to allow one or more of the outputs to be unused (open) without affecting the other channels Or conversely if more than 30mA is needed the outputs can be combined for higher total currents.

Package power dissipation can be calculated from the following equation:

$P_{\rm D} = (n \times I_{\rm OUT})$	$(V_l) \times (V_l)$	$LOAD - V_{LED}$)
n	=	Number of outputs used
I _{OUT}	=	Current from each output
V _{LOAD}	=	Output Supply Voltage
V _{LED}	=	Minimum LED forward voltage
P _D	=	Power Dissipated in mW

Care should be exercised not to exceed the power dissipation of the package or the maximum junction temperature of the die. Proper mounting of the package with thermal vias (see PCB Land Guidelines and Thermal Pad Design section) enhances power dissipation capability. As an example to drive 24 white LED's, 4 per channel from a 18V V_{LED} supply @ 25mA per LED string, we will assume the minimum LED forward voltage to be 3.5V with an maximum operating ambient of 50°C.

 $P_D = (6 \times 25 \text{ mA}) \times (18 \text{ V} - (4 \times 3.5 \text{ V})) = 15 \times 4 \text{ V} = 0.6 \text{ W}$

This represents a 21.6°C temperature rise ($36^{\circ}C/W * 0.6W$) for a die temperature of about 72°C, ignoring device drain current power dissipation that only represents about a 3°C rise worst case. This is well under the die junction temperature maximum rating of 150°C, and within the 85°C electrical specifications.

DIMMING

Dimming can be accomplished both with current amplitude control (changing the R_{SET} resistor value) with a PWM signal (toggling the DIG_DIM input) or both. Current between the I_{SET+} and I_{SET-} pins may be varied for current amplitude dimming. If a mechanical input is needed, a rheostat in series with a resistor connected from I_{SET+} to I_{SET-} can be used.:

 I_{OUT} =Current Ratio× I_{SET}

APPLICATIONS



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APPLICATION NOTE - CONTINUED

The range of the R_{SET} resistor can vary between 1K and 40K Ohms. The resistor in series with the rheostat will set the maximum current and should be a least 1K Ω in value. If a fixed sink current is desired its easy to find the RSET resistor value. As an example, suppose the desired output current is 25mA per sink channel. The R_{SET} resistor can be calculated as follows:

 $R_{SET(K\Omega)} = Current ratio / Output current(mA) \times VR_{SET}$

$$R_{SFT(K\Omega)} = 24.5 / 25 \times 1.26 = 1.23 K\Omega$$

Once the maximum sink current is set the rheostat will increase the RSET value thus dimming the LED by reducing the sinking current.

Wide range dimming can be accomplished by using the DIG_DIM input pin to pulse the output sink current. The DIG_DIM pin may be driven with a TTL compatible logic PWM signal to dim the LED's. The recommended PWM frequency for dimming is between 100 Hz and 100 KHz. Below 100 Hz flicker may be observed. Above 100 KHz duty cycle accuracy and minimum pulse width is reduced due to delay times and the current slew rate. To obtain the maximum dim range and still make use of the slope control function (see CSLOPE pin below) it is advisable to use a lower frequency on the DIG_DIM input.

If PWM dimming is used, use of separate power and ground lines directly from the power source point will help to prevent noise generated from the LED current transients from entering video or audio subsystems on the same supply rails. Additional power supply filtering may be needed in PWM dimming applications. Care should be exercised in the PCB layout to prevent coupling from the SINK outputs to the DIG DIM pin.

CSLOPE PIN

The CSLOPE pin is available to control the rise and fall times of the SINK outputs during pulse dimming. With the CSLOPE pin open a minimum rise and fall time of about 120 to 200nS will be present on the output waveforms along with a delay time (DIG_DIM to SINKx) of about 200nS. As the CSLOPE capacitor is increases in value so will the corresponding rise and fall times and delay to output. The calculation for the CSLOPE value is approximately 450 μ A * T_R or T_F in microseconds, C in picofarads. So for a 5uS rise and fall time 0.00045 * 5 = 2250pF or about a typical .0022uF capacitor value. For typical slope rise and fall times see the follow chart



Typical CSLOPE vs Slope Times



The chart below illustrates the correlation between the IC's drain current and the total sink output current. The drain current will also increase slightly if one or more the SINKx pins are left floating or when the SINK outputs are near dropout, however in both of these circumstances the increased drain current will be small and controlled and is a feature of the design.

LX1991 Typical Drain Current Vs Sink Current





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CHARTS



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MECHANICAL DRAWING

16-Pin MLPQ Plastic (4x4mm EP)



Dim	MILLIMETERS		INCHES	
DIIII	MIN	MAX	MIN	MAX
А	0.80	1.00	0.031	0.039
A1	0	0.05	0	0.002
A3	0.18	0.30	0.007	0.012
b	0.23	0.38	0.009	0.015
D	4.00 BSC		0.157 BSC	
Е	4.00	4.00 BSC		BSC
е	0.65	BSC	0.026	BSC
D2	2.55	2.80	0.100	0.110
E2	2.55	2.80	0.100	0.110
K	0.20	-	0.008	
L	0.30	0.50	0.012	0.020

Note:

 Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.

LO

16-Pin PCB Land Guidelines and Thermal Pad Design



The typical land pattern shown includes thermal vias in the exposed die attach pad for improved thermal performance. Vias should be about 0.3mm in diameter, with the via plated to about 1.0 ounce copper. Vias should be plugged to prevent voids being formed due to capillary action. This can be avoided by tenting the via during the solder mask process. In addition, to reduce solder paste volume on the thermal land, it is recommended that an array of small apertures in the solder mask be used instead of one large aperture, with the goal of 50 - 80% solder paste coverage. Please review IPC / EIA J-Std-001C Section 9.2.6.4 "Bottom Only Termination" for solder joint requirements.



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NOTES

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