LX1562/1563

SECOND-GENERATION POWER FACTOR CONTROLLER

PRODUCTION DATA SHEET

THE INFINITE POWER OF INNOVATION

DESCRIPTION

The LX1562 is a second-generation family of power factor correction controllers using a discontinuous mode of operation. They are optimized for electronic ballast applications. Many improvements have been made over the original SG3561A controller introduced by Silicon General Semiconductor in 1992.

New features include the addition of an internal start-up circuit eliminating bulky external components while allowing independent boost converter operation. Addition of internal current sense blanking eliminating the need for an external R/C filter network. Internal clamping of the error amplifier and multiplier outputs improves turn on overshoot characteristics and current limiting.

Special circuitry has also been added to prevent no load runaway conditions. And finally, output drive clamps limiting power MOSEFT gate drive independent of supply voltage greatly enhance the products practical application.

Although the IC design has been optimized for electronic ballast applications, it can also be used for power factor correction in lower power (typical < 300W) AC-DC converters. One unique feature of the device is encompassed by the addition of internal logic circuitry to detect zero crossing of the inductor current thus maintaining the discontinuous current mode of operation. This feature prevents large current gaps from appearing thereby minimizing distortion and enhancing power factor correction.

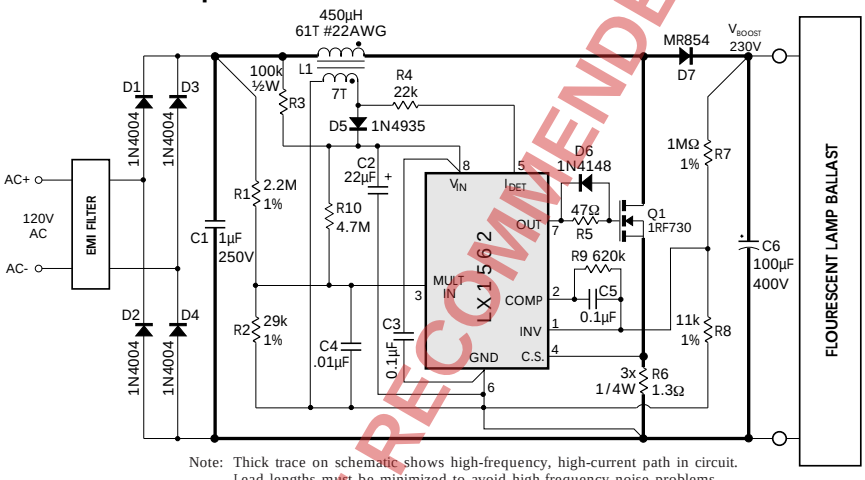
IMPORTANT: For the most current data, consult *MICROSEMI*'s website: **http://www.microsemi.com**

KEY FEATURES

- Internal Start-Up Circuit
- Internal Current Sense Blanking
- Improved MicroPower Start-Up Current (300µA maximum)
- Clamped E.A. Output For Lower Turn-On Overshoot
- Multiplier Clamp Limits Maximum Input Current
- Internal Over Voltage Protection Replaces Built-In C.S. Offset
- PWM Output Clamp Limits MOSFET Gate Drive Voltage
- Increased UVLO Hysteresis Reduces Start-Up Timing (LX1562 Only)
- Low Operating Current Consumption
- Internal 1.5% Reference
- Totem Pole Output Stage
- Automatic Current Limiting of Boost Stage
- Discontinuous Mode of Operation With No Current Gaps
- No Slope Compensation Required

PRODUCT HIGHLIGHT

Typical Application Of The LX1562 In An 80W Fluorescent Lamp Ballast With Active Power Factor Control



Note: Thick trace on schematic shows high-frequency, high-current path in circuit. Lead lengths must be minimized to avoid high-frequency noise problems.

KEY FEATURES

- Electronic Ballast
- Switching Power Supplies

Available Options Per Part #

Part #	Start-Up Voltage	Hysteresis Voltage
LX1562	13.1V	5.2V
LX1563	9.8V	2.1V

PACKAGE ORDER INFO

T_A (°C)	M Plastic DIP 8-Pin RoHS Compliant / Pb-free Transition D/C: 0503	DM Plastic SOIC 8-Pin RoHS Compliant / Pb-free Transition D/C: 0440
0 to 100	LX1562IM LX1563IM	LX1562IDM LX1563IDM

Note: Available in Tape & Reel. Append the letters "TR" to the part number (i.e. LX5241CDB-TR).

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LINFINITY MICROELECTRONICS INC.
11861 WESTERN AVENUE, GARDEN GROVE, CA. 92841, 714-898-8121, FAX: 714-893-2570

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V_{IN}) ..... -0.3V to 28V
Peak Driver Output Current (Note 3) ..... ±500mA
Driver Output Clamping Diodes
$V_O > V_{CC}$ or $V_O < -0.3V$ ..... ±10mA
Detector Clamping Diodes
$V_{DET} > 6V$ or $V_{DET} < 0.9V$ ..... ±10mA
Error Amp, Multiplier, and Comparator Input Voltages ..... -0.3V to 6V
Detector Input Voltage (Note 2) ..... -0.3 to 6V
Operating Junction Temperature
Plastic (M and DM Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C
Pb-free / RoHS Peak Package Solder Reflow Temp (40 second max. exposure).....260°C (+0, -5)

Note 1. Values beyond which damage may occur. All voltages are specified with respect to ground, and all currents are positive into the specified terminal.
Note 2. With no limiting resistor.
Note 3. Current duty cycle is chosen such that T_J is below 150°C.

THERMAL DATA

M PACKAGE:

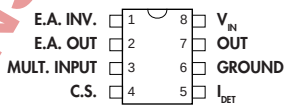
THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	95°C/W

DM PACKAGE:

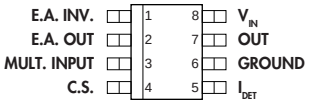
THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	165°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system.
All of the above assume no ambient airflow

PACKAGE PIN OUTS



M PACKAGE
(Top View)



DM PACKAGE
(Top View)
RoHS / Pb-free 100% Matte Tin Lead Finish

RECOMMENDED OPERATING CONDITIONS (Note 4)

Parameter	Symbol	Recommended Operating Conditions			Units
		Min.	Typ.	Max.	
Supply Voltage Range		11		25	V
Peak Driver Output Current			±200		mA
Operating Ambient Temperature Range:					
LX1562/1563		0		100	°C

Note 4. Range over which the device is functional.

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for the LX1562/1563 with 0°C≤ T_A ≤ 100°C; V_{IN}=12V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Symbol	Test Conditions	LX1562I/1563I			Units
			Min.	Typ.	Max.	
Under-Voltage Lockout Section						
Start Threshold Voltage	V_{ST}	LX1562 Only	12	13.1	14	V
		LX1563 Only	9.2	9.8	10.6	V
UV Lockout Hysteresis	ΔV_H	LX1562 Only	4	5.2	6	V
		LX1563 Only	1.7	2.1	2.5	V
Supply Current Section						
Start-Up Supply Current	I_{ST}	$V_{IN} < V_{TH}$		200	300	µA
Operating Supply Current	I_Q	V_{IN} = 12V, Output Not Switching		5	8	mA
Dynamic Operating Supply Current	I_{OP}	V_{IN} = 12V, 50kHz, CGS = 1000pF		6	10	mA
Reference Section (Note 5)						
Initial Accuracy (Note 8)	V_R	I_{REF} = 0mA, T_A = 25°C	2.465	2.50	2.535	V
		I_{REF} = 0mA	2.44		2.56	V
Line Regulation	ΔV_I	12V < V_{IN} < 25V		0.1		mV
Load Regulation	ΔV_L	0 < I_{REF} < 2mA		1.3		mV
Temperature Stability	ΔV_T			20		mV
Error Amplifier Section						
Input Bias Current	I_B		-500	50	500	nA
Large Signal Open Loop Voltage Gain	A_{VOL}	(Note 5)	60	80		dB
Slew Rate	S			0.63		V/µsec
Power Supply Rejection Ratio (Note 5)	PSRR	11 to 25V	60	80		dB
Output Source Current	I_{SR}	V_{OH} = 3V	-2	-4.5		mA
Output Sink Current	I_{SK}	V_{OL} = 2V	3	4.5		mA
Output Voltage Range (Note 7)	$E.A._O$	No Load on E.A. Output	1.2		3.8	V
Unity Gain Bandwidth	f_B			1.7		MHz
Phase Margin	ϕ_B			49		°
Multiplier Section						
Mult. Input Voltage Range	V_{M1}		0		2	V
M2 Input Voltage Range	V_{M2}		V_{REF}		V_{REF} + 1	V
Mult. Input Bias Current (M1)	I_{MB}			-0.24		µA
Multiplier Gain (Note 5 & 6)	K	V_{M1} = 1V, ΔV_{EA0} = 2.7V to 3.3V	0.55	0.68	0.8	V/V²
		ΔV_{M1} = 0.5V to 1.5V, V_{EA0} = V_{REF} + 1V	0.55	0.61	0.75	V/V²
Multiplier Gain Temperature Stability	ΔK_T			-0.2		%/°C
Maximum Multiplier Output Voltage	V_{CLMP}	V_{M1} = 2V, V_{PIN1} = 0V	1.1	1.24	1.45	V

(Electrical Characteristics continue next page.)

ELECTRICAL CHARACTERISTICS (Con't.)

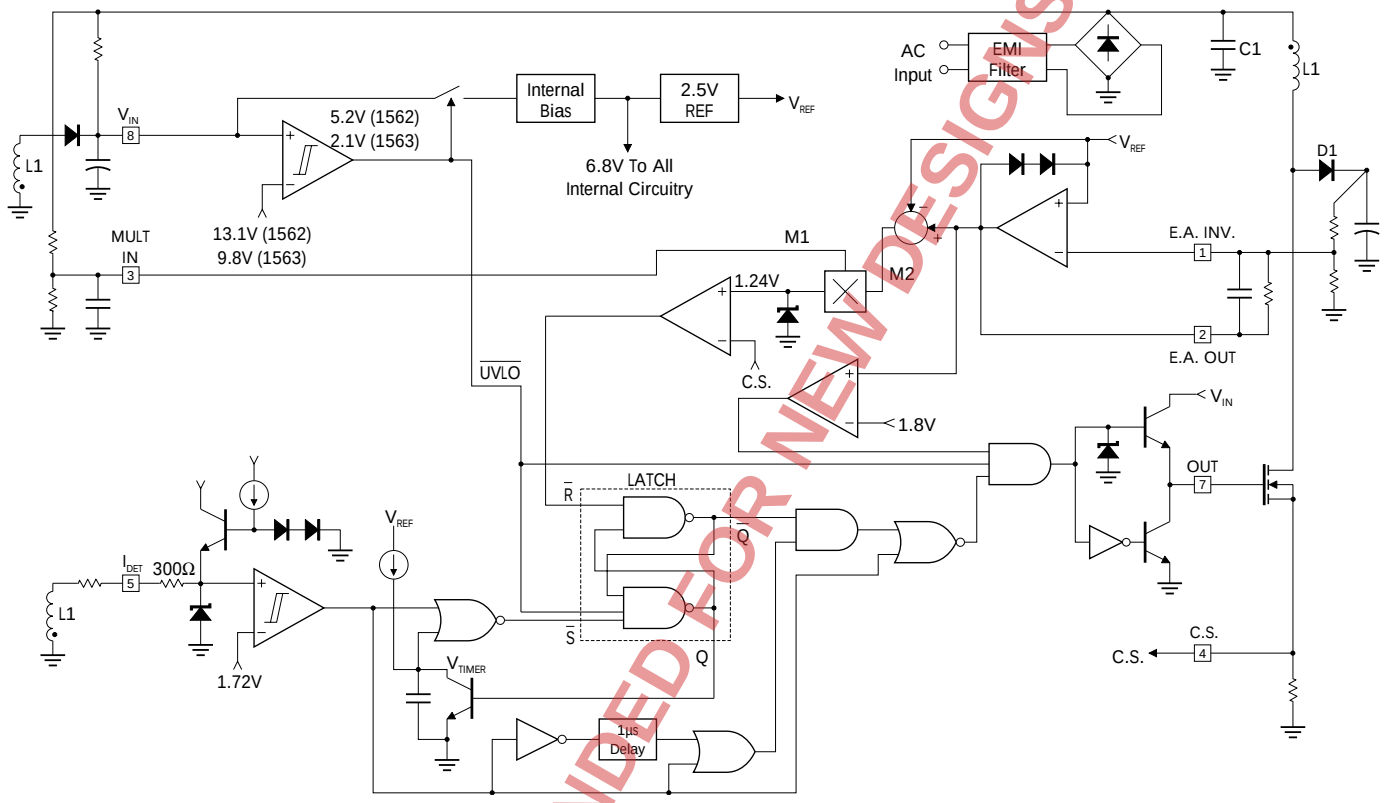
Parameter	Symbol	Test Conditions	LX1562I/1563I			Units
			Min.	Typ.	Max.	
Current Sense Comparator Section						
Input Bias Current	I_{CSB}	$0V \le V_{CS} \le 1.7V$	-1	-0.3	1	µA
Current Sense Delay to Output	t_d	$E.A._{OUT} = 3.7V$, $V_{CS} = 0$ to $1.2V$, $V_{M1} = 1V$		280	500	ns
C.S. Blanking Time	t_{BLK}		0.4	0.9	1.2	µs
C.S. Input Offset Voltage	V_{OFF}	$V_{EA0} = 2.2V$, $V_{M1} = 0V$, $I_{DETC} = 0V$	-20	3	20	mV
Detect Section						
Input Voltage Threshold - High	V_{HI}		1.6	1.72	1.9	V
Hysteresis	H_D		180	240	300	mV
Input LO Clamp Voltage	V_{DL}	$I_{DET} = 100µA$	0.4	0.62	0.85	V
Input HI Clamp Voltage	V_{DZ}	$I_{DET} = 3mA$	7.0	7.8	8.6	V
Input Current	I_{DB}	$1V \le V_{DET} \le 6V$	-1	-0.2	1	µA
Input HI/LO Clamp Diode Current	I_{DMX}	$V_{DET} < 0.9V$, $V_{DET} > 6V$			±3	mA
Restart Timer Section						
Restart Time	t_{RST}			300		µsec
Output Driver Section						
Output High Voltage	V_{PRH}	$I_L = -10mA$, $V_{IN} = 12V$	8.5	9		V
Output Low Voltage	V_{PRL}	$I_L = 10mA$, $V_{IN} = 12V$		0.8	1	V
Output Rise Time	t_R	$C_L = 1000pF$		130	200	ns
Output Fall Time	t_f	$C_L = 1000pF$		50	120	ns
Maximum Output Voltage	V_{DRMX}	$V_{IN} = 20V$	13	13.8	15	V

Notes: 5. Because the reference is not brought out externally, these specifications are tested at probe only, and cannot be tested on the packaged part. They are guaranteed by design, and shown for illustrative purposes only.

6. $$K = \frac{\Delta V_{C.S.}}{(\Delta V_{M1}) \times (V_{EA0} - V_{REF})} \approx \frac{\Delta V_{C.S.}}{(V_{M1})(\Delta V_{EA0})}$$

7. This parameter, although guaranteed, is not tested in production.
8. Initial accuracy includes input offset voltage of error amplifier.

BLOCK DIAGRAM / PIN DESCRIPTIONS



FUNCTIONAL DESCRIPTION

Pin	#	Description
V_{IN}	8	Input supply voltage.
GND	6	Input supply voltage return. Must always be the lowest potential of all the pins.
INV	1	Inverting input of the Error Amplifier. The output of the Boost converter should be resistively divided to 2.5V and connected to this pin.
E.A. OUT	2	The output of the Error Amplifier. A feedback compensation network is placed between this pin and the INV pin.
MULT IN	3	Input to the multiplier stage. The full-wave rectified AC is divided to less than 2V and is connected to this pin.
C.S.	4	Input to the PWM comparator. Current is sensed in the Boost stage MOSFET by a resistor in the source lead, and is fed to this pin. An internal blanking circuit eliminates the RC low pass filter that otherwise is required to eliminate leading edge spike.
I_{DET}	5	A current driven logic input with internal clamp. A second winding on the Boost inductor senses the flyback voltage associated with the zero crossing of the inductor current and feeds it to the I_{DET} pin through a limiting resistor. Low on this pin causes V_O (pin 7) to go high.
OUT	7	PWM output pin. A totem-pole output stage specially designed for direct driving the MOSFET.

GRAPH / CURVE INDEX

Characteristic Curves

FIGURE INDEX

IC Description

Application Information

Typical Applications

CHARACTERISTIC CURVES

FIGURE 1. — E.A. OUTPUT VOLTAGE vs. C.S. THRESHOLD

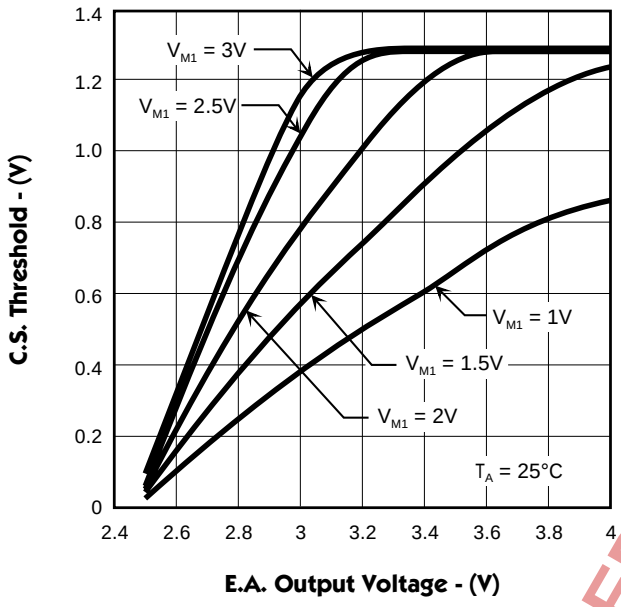


FIGURE 2. — MULTIPLIER INPUT VOLTAGE vs. C.S. THRESHOLD

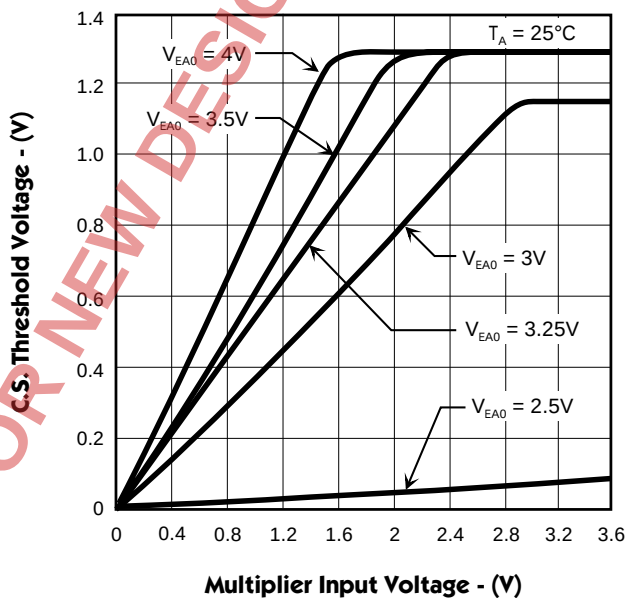


FIGURE 3. — MULTIPLIER GAIN (V_{M1}=1V, V_{EA0}=3.5V) vs. TEMPERATURE

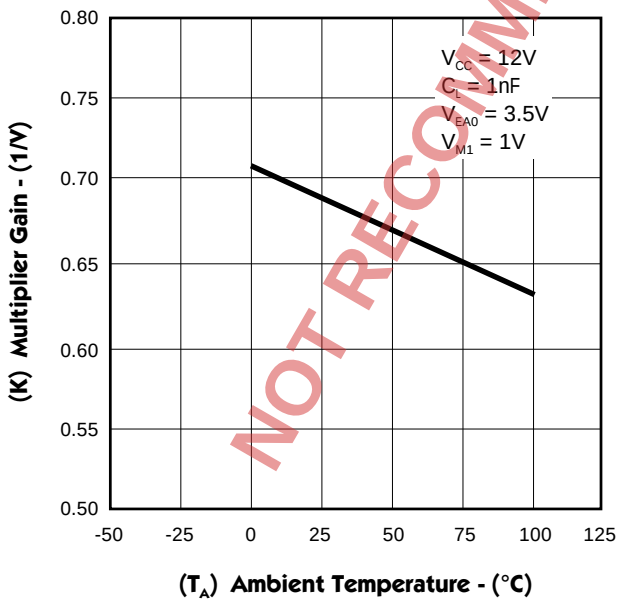
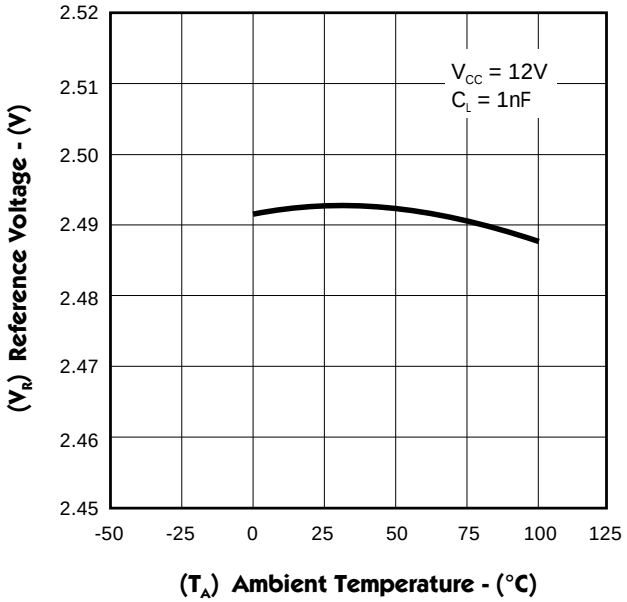


FIGURE 4. — REFERENCE VOLTAGE (Including Offset) vs. TEMPERATURE



CHARACTERISTIC CURVES

FIGURE 5. — E.A. INPUT BIAS CURRENT vs. TEMPERATURE

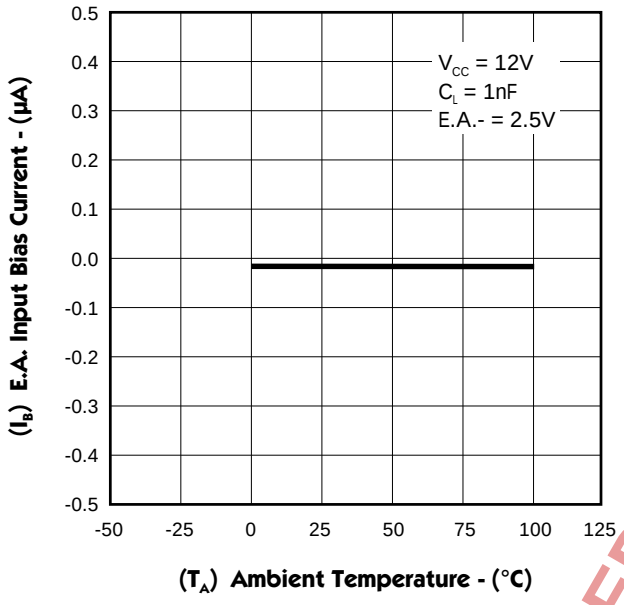


FIGURE 6. — E.A. SINK CURRENT @2V vs. TEMPERATURE

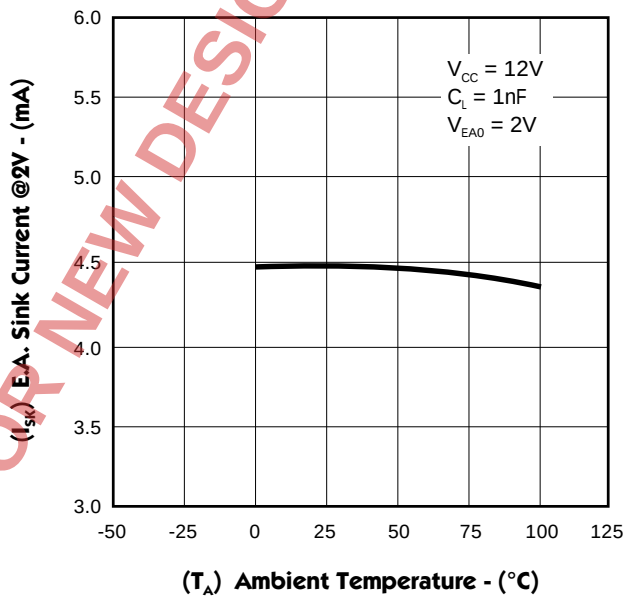


FIGURE 7. — START-UP SUPPLY CURRENT vs. TEMPERATURE

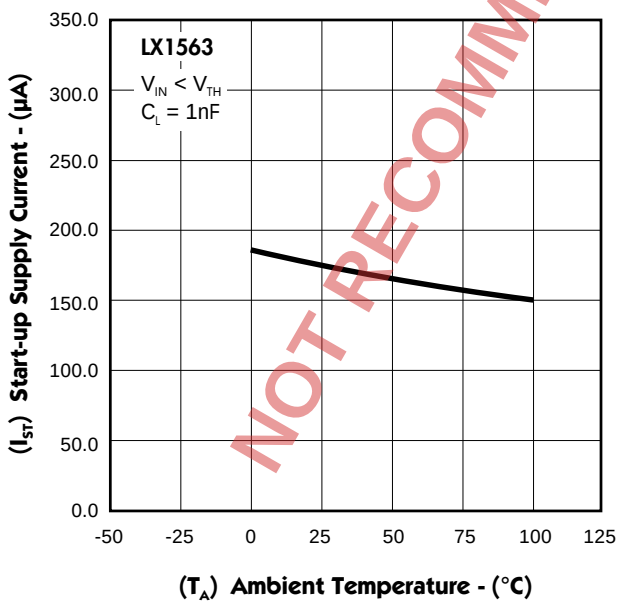
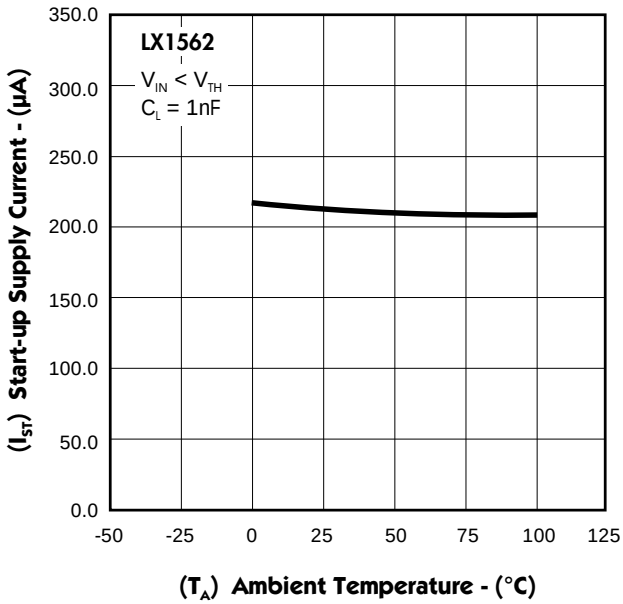


FIGURE 8. — START-UP SUPPLY CURRENT vs. TEMPERATURE



CHARACTERISTIC CURVES

FIGURE 9. — START-UP THRESHOLD vs. TEMPERATURE

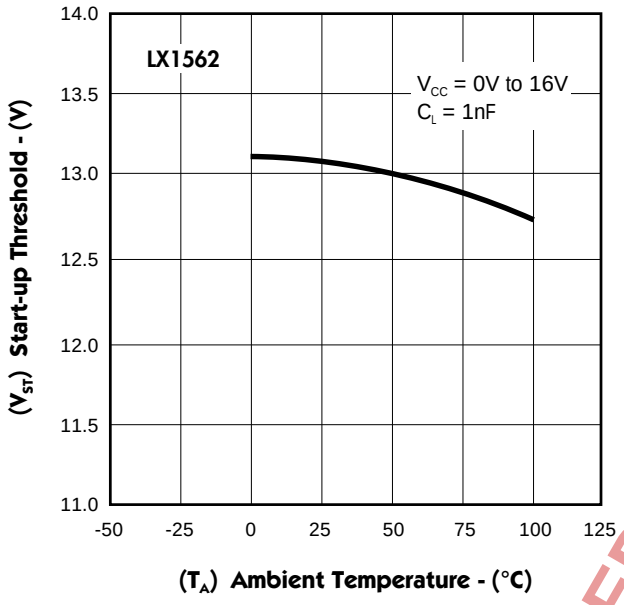


FIGURE 10. — START-UP THRESHOLD vs. TEMPERATURE

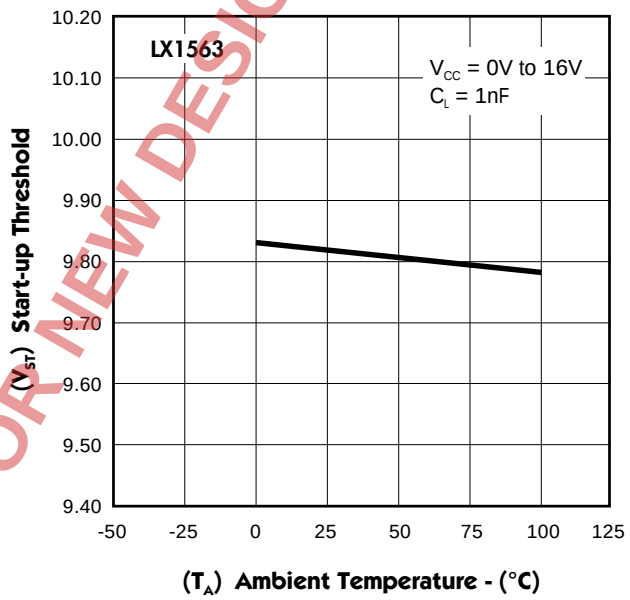


FIGURE 11. — UV LOCKOUT HYSTERESIS vs. TEMPERATURE

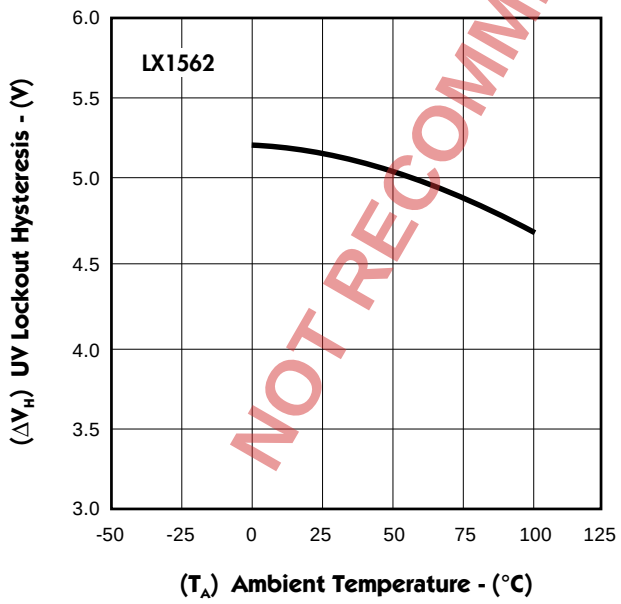
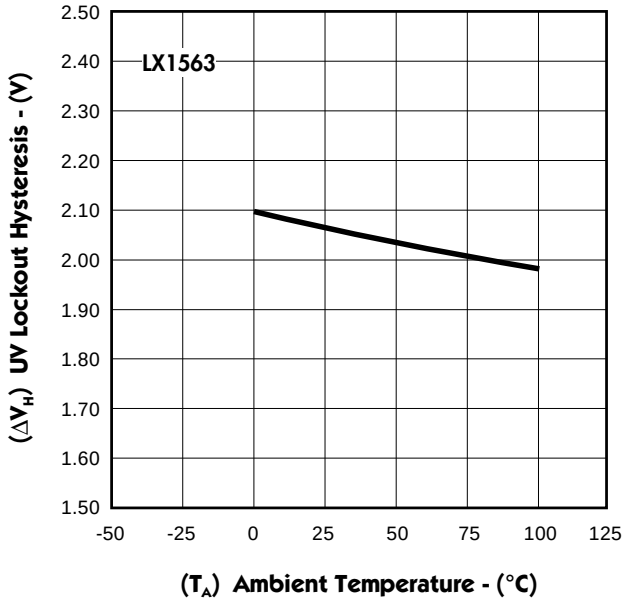


FIGURE 12. — UV LOCKOUT HYSTERESIS vs. TEMPERATURE



CHARACTERISTIC CURVES

FIGURE 13. — I_{DET} THRESHOLD HIGH vs. TEMPERATURE

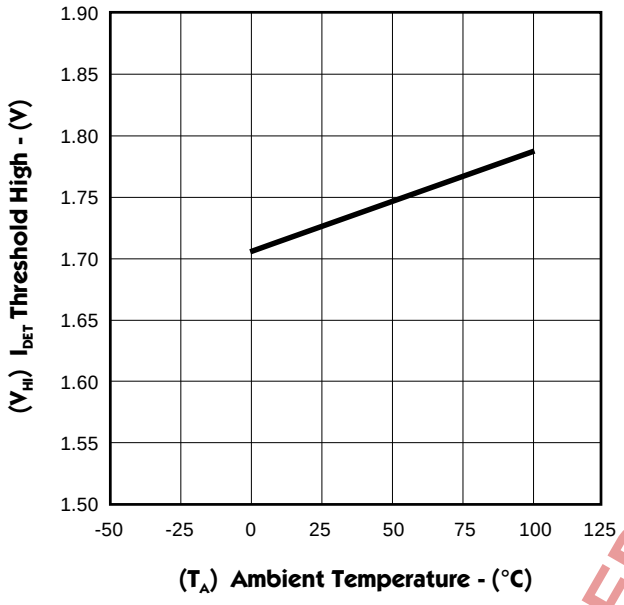


FIGURE 14. — I_{DET} INPUT HYSTERESIS vs. TEMPERATURE

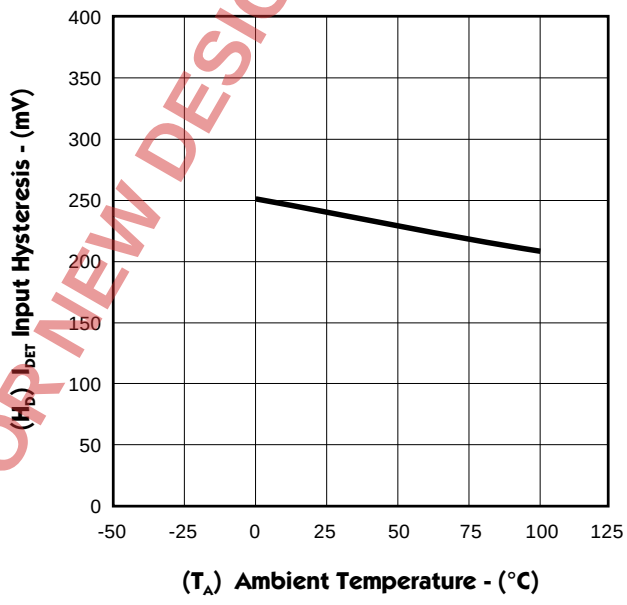


FIGURE 15. — RUN-AWAY COMPARATOR THRESHOLD vs. TEMPERATURE

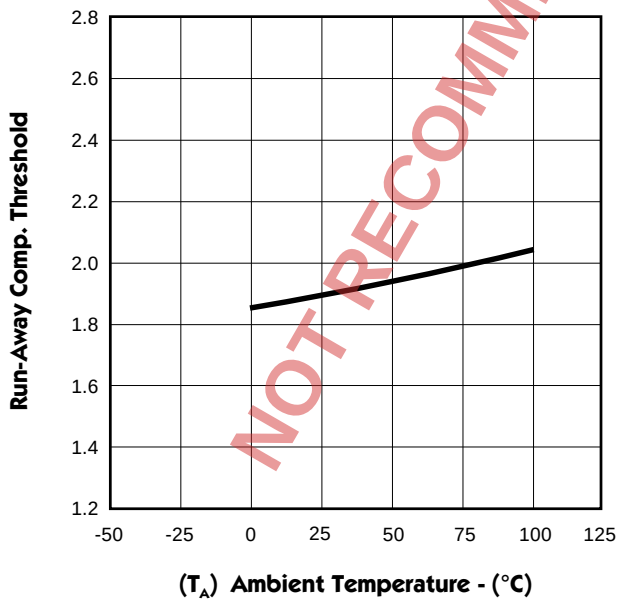
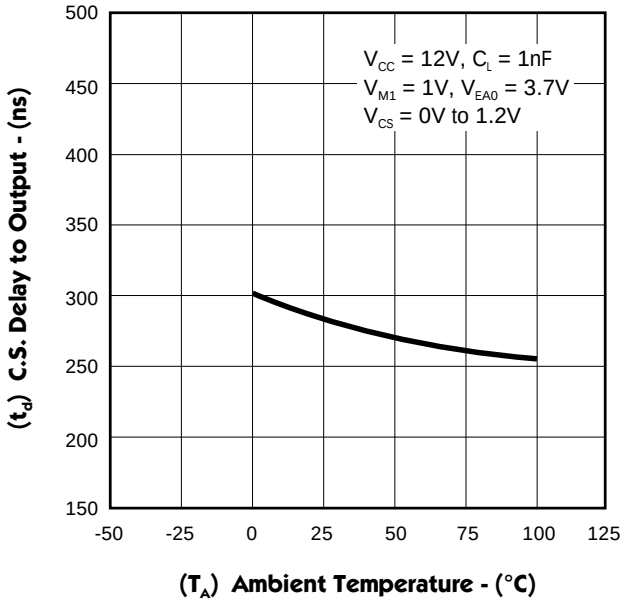


FIGURE 16. — C.S. DELAY TO OUTPUT vs. TEMPERATURE



CHARACTERISTIC CURVES

FIGURE 17. — C.S. BLANKING TIME vs. TEMPERATURE

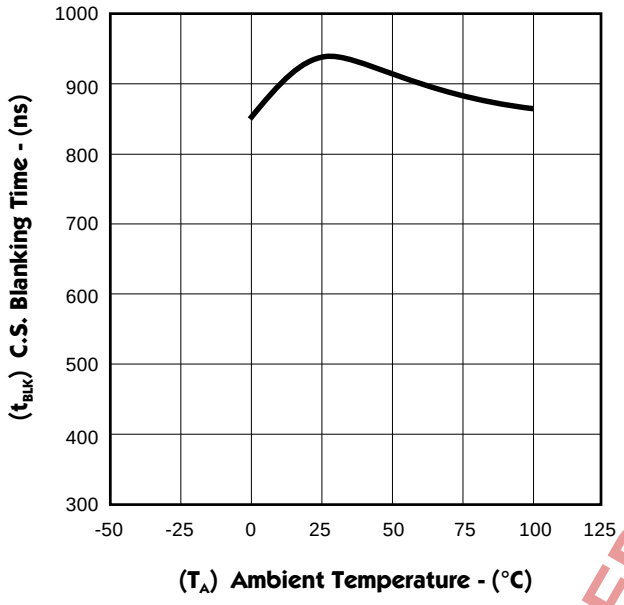


FIGURE 18. — RESTART TIME vs. TEMPERATURE

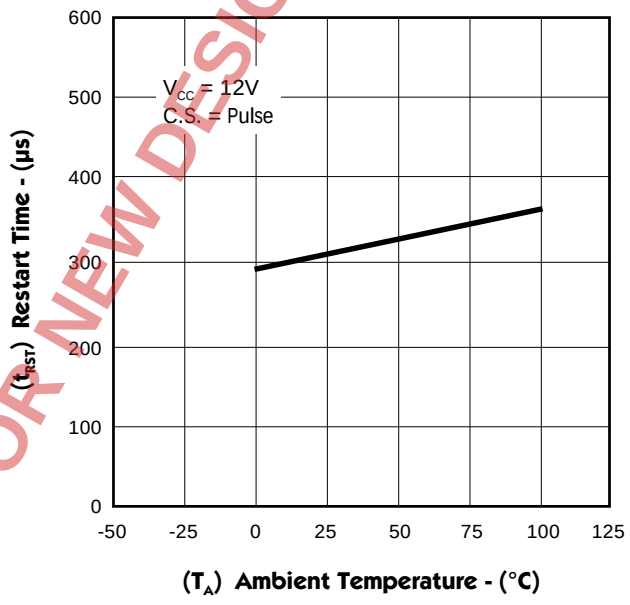


FIGURE 19. — FALL TIME vs. TEMPERATURE

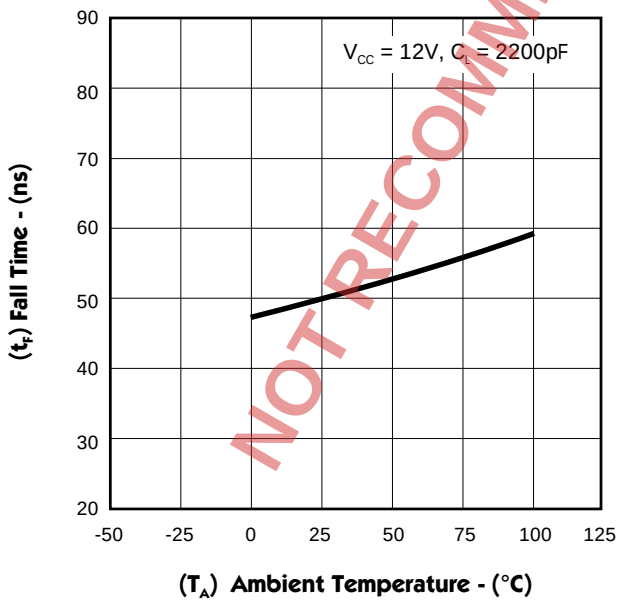
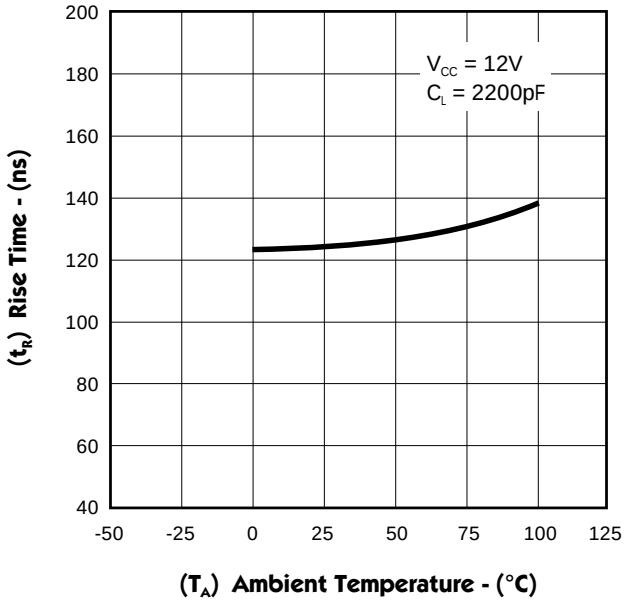


FIGURE 20. — RISE TIME vs. TEMPERATURE



CHARACTERISTIC CURVES

FIGURE 21. — SUPPLY CURRENT vs. SUPPLY VOLTAGE

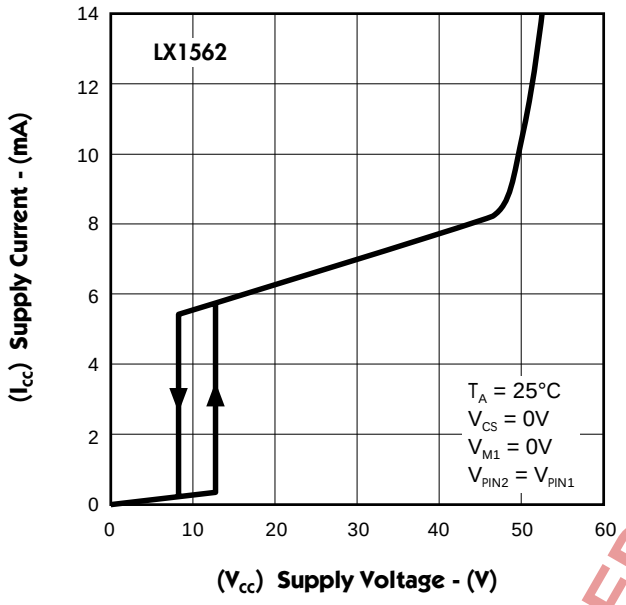


FIGURE 22. — SUPPLY CURRENT vs. SUPPLY VOLTAGE

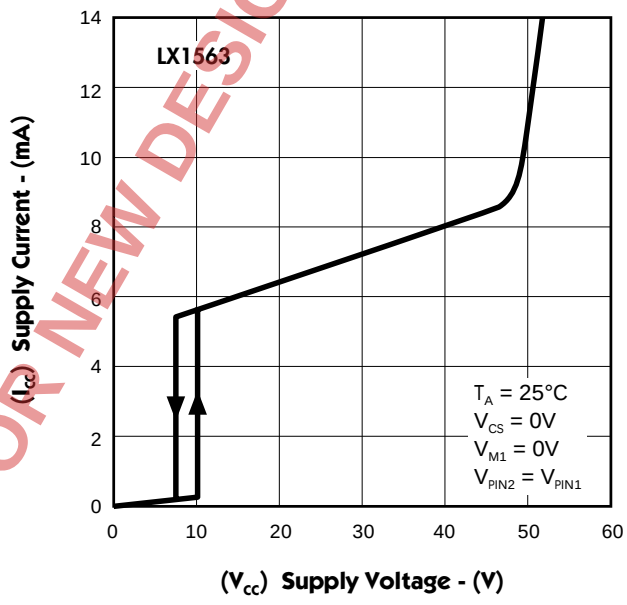
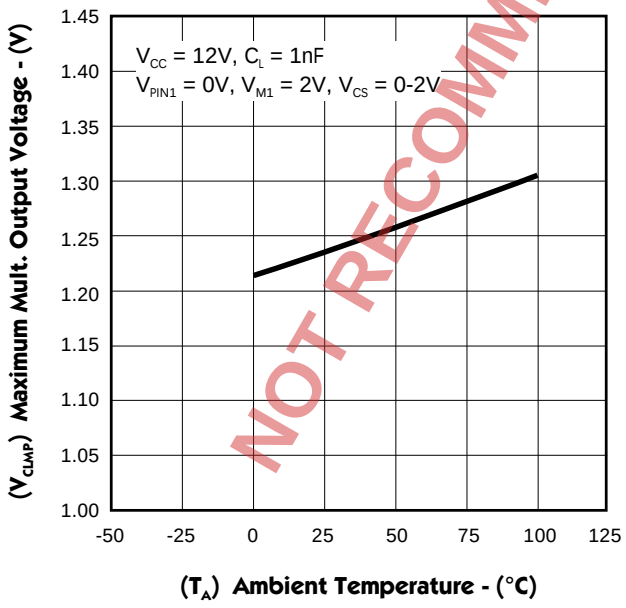


FIGURE 22a. — MAXIMUM MULTIPLIER OUTPUT vs. TEMPERATURE



FUNCTIONAL DESCRIPTION

The operation of the IC is best described by referring to the block-diagram. The output of the multiplier stage generates a voltage proportional to the product of the rectified AC line and the output of the error amplifier. This voltage serves as the reference for the inductor peak current that is sensed by the resistor in series with the external power MOSFET. When the sense voltage exceeds this threshold, C.S. comparator trips and resets the latch as well as turning the power MOSFET off.

The energy stored during switch on-time is now transferred and stored in the output capacitor, causing the inductor current to ramp down. When current reaches zero level (inductor runs out of energy) , boost diode (D1) stops conducting and the residual inductor energy and the drain to source capacitance of the power MOSFET create an LC tank circuit which causes drain voltage to resonate at this frequency. The resonating voltage is detected by the secondary winding (Idet winding) of the inductor. When this voltage swings negative "I detect" pin senses it and activates the blanking circuit , sets the latch, and turns power MOSFET on, repeating the cycle. This operation continues for the entire cycle of the AC rectified input resulting in an inductor current as shown in Figure 23. The high frequency content of this current is then filtered by the input capacitor (C1) resulting in a sine wave input current in phase with the AC line voltage.

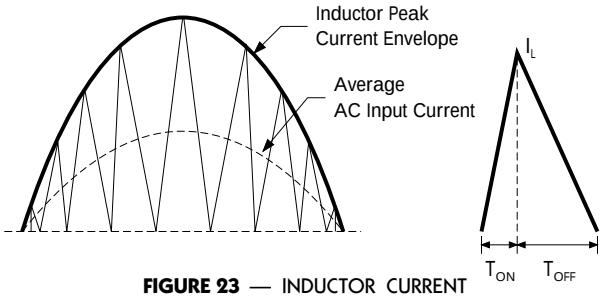


FIGURE 23 — INDUCTOR CURRENT

Output voltage regulation is accomplished when the error amplifier compares this voltage to an internal 2.5V reference and generates an error voltage. This voltage then controls the amplitude of the multiplier output adjusting the peak inductor current proportional to the load and line variations, maintaining a well regulated voltage.

IC DESCRIPTION

UNDERVOLTAGE LOCK OUT

The LX1562/63 undervoltage lock-out is designed to maintain an ultra low quiescent current of less than 300µA, while guaranteeing the IC is fully functional before the output stage is activated. Comparing this to the SG3561A device, a 40% reduction in start-up current is achieved, resulting in 40% less power dissipation in the start-up resistor. This is especially important in electronic ballast applications that are designed to operate in harsh environments, with convection cooling as the only means of heat dissipation.

Figure 24 shows an efficient supply voltage using the ultra low start-up current of the LX1562 in conjunction with a bootstrap winding off of the power transformer. Circuit operation is as follows:

The start-up capacitor (C1) is charged by current through resistor (R1) minus the start-up current drawn by the IC. This resistor is typically chosen to provide 2X the maximum start-up current at low line to guarantee start-up under the worst case condition. Once the capacitor voltage reaches the start-up threshold, the IC turns on, starting the switching cycle. The operation of the IC demands an increase in operating current which results in discharging the capacitor. During the discharge cycle, the flyback voltage of the auxiliary winding is rectified and filtered via rectifier (D1) and charges the capacitor above the minimum operating voltage of the device and takes over as the supply voltage. The start-up capacitor and auxiliary winding must be selected such that it satisfies worst case IC conditions. Figure 25 shows start-up time and voltage of capacitor C1.

Table 1 shows the start-up voltage and hysteresis for LX1562 and LX1563. The LX1562 is used for stand alone pre-regulator applications while LX1563 is ideal for applications where supply voltage is derived elsewhere and requires less than 14V start-up.

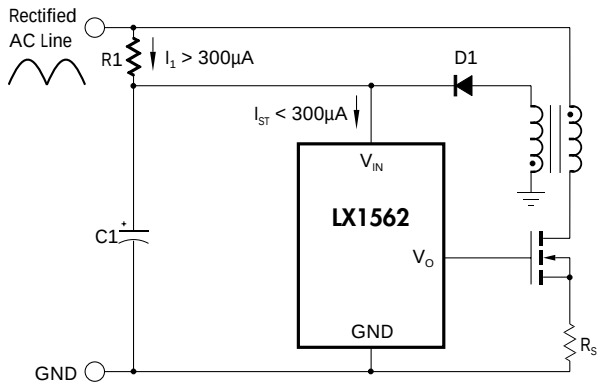


FIGURE 24 — TYPICAL APPLICATION OF START-UP CIRCUITRY

TABLE 1

Part #	Start-Up Voltage	Hysteresis Voltage
LX1562	13.1V	5.2V
LX1563	9.8V	2.1V

IC DESCRIPTION

VOLTAGE REFERENCE (continued)

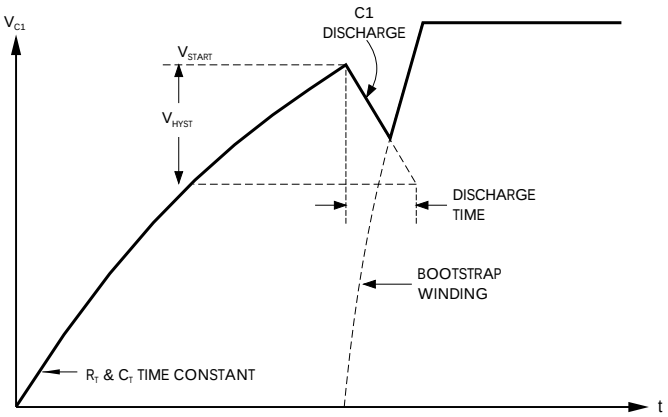


FIGURE 25 — START-UP CAPACITOR VOLTAGE

VOLTAGE REFERENCE

The voltage reference is a low drift bandgap design which provides a stable +2.5V output with maximum of ±1.5% initial accuracy. This voltage is internally tied to the non-inverting input of the amplifier and is not available for external connection. The initial accuracy of the reference includes error amplifier input offset voltage. Figure 26 shows typical variation of the reference voltage vs. temperature.

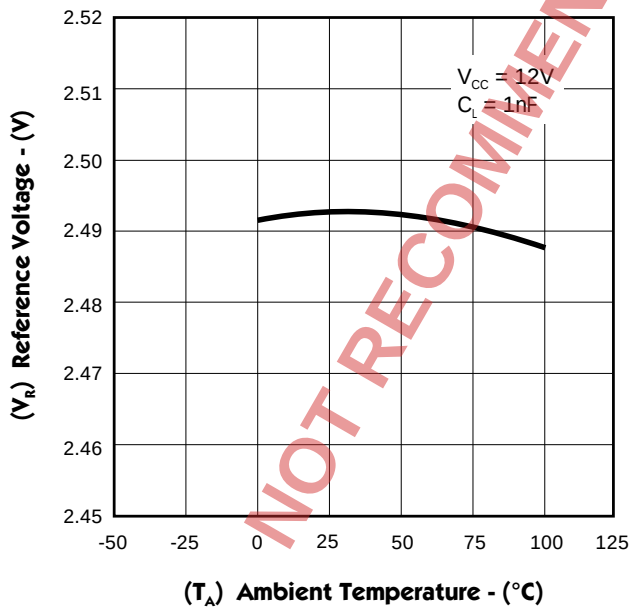


FIGURE 26 — REFERENCE VOLTAGE (Including Offset) vs. TEMPERATURE

ERROR AMPLIFIER

The error amplifier is an internally compensated op-amp with access to the inverting input and the output pin. The non-inverting input is internally connected to the voltage reference and is not available for external connection. The amplifier is designed for an open loop gain of 80dB, along with a typical bandwidth of 1.7MHz and 49 degrees of phase margin. The boost output voltage of the power factor pre-regulator is divided down and monitored by the inverting input. Input bias current (0.5µA max) can cause an output voltage error that is equal to the product of the input bias current and the value of the upper divider resistor. The amplifier's output is available for external loop compensation. Typically, the loop bandwidth is set below 10Hz in order to reject the low frequency ripple associated with 2X the line frequency. For example, if the error amplifier is configured as an integrator with 1.2Hz bandwidth, it will have 40dB ripple rejection at 120Hz frequency. This means that if the output of the error amp is allowed to have 100mV of ripple, the boost converter must be limited to less than 10V of ripple on its output.

To prevent boost output run away condition that may occur during removal of the output load, a separate comparator monitors the E.A. output voltage and compares it to an internal 1.8V reference. When load is removed, E.A. output swings lower than 1.8V, trips the comparator and turns output driver off till the inverting input voltage drops below 2.5V. At this point, the E.A. output swings positive, turns the output driver back on and repeats the cycle until the load is returned to normal condition.

To reduce output overshoot during line and load transients, the E.A. output is clamped to two diode drops above the reference voltage. This prohibits the amplifier from being saturated, allowing it to recover faster thus minimizing the boost voltage overshoot.

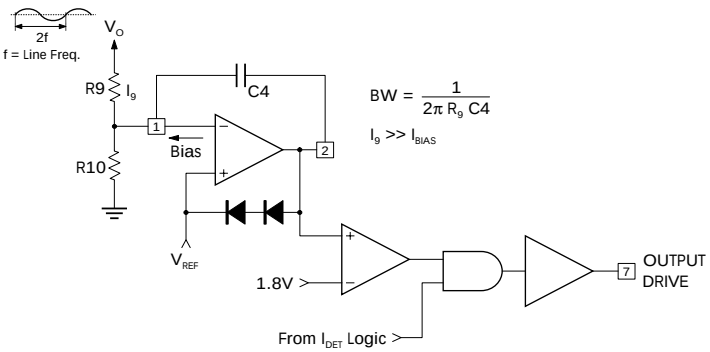


FIGURE 27 — THE AMPLIFIER CONFIGURED AS AN INTEGRATOR FOR LOOP COMPENSATION

IC DESCRIPTION

MULTIPLIER

The LX1562/63 features a one quadrant multiplier stage having two inputs. One (V_{M2}) is internally driven by a DC voltage which is the difference of E.A. output and V_{REF}. The other (V_{M1}), is connected to an external resistor divider monitoring the rectified AC line. The output of the multiplier which is a function of both inputs, controls inductor peak current during each cycle of operation. This allows the inductor peak current to follow the AC line thus forcing the average input current to be sinusoidal.

The multiplier is in the linear region if the V_{M1} input is limited to less than 2V and the E.A. output is kept below 3.5V under all line and load conditions. The output is internally clamped to 1.24V typically to limit the MOSFET peak current during turn on or under excessive load conditions. The equation below describes the relationship between multiplier output voltage and the its inputs.

$$V_{M0} = K * V_{M1} * (V_{EA0} - V_{REF})$$

where: K = Multiplier gain (typ. 0.65)
V_{M1} = Voltage at pin3 (0 to 2V)
V_{EA0} = Error amp output voltage (2.5 to 3.5V)
V_{M0} = Multiplier output voltage

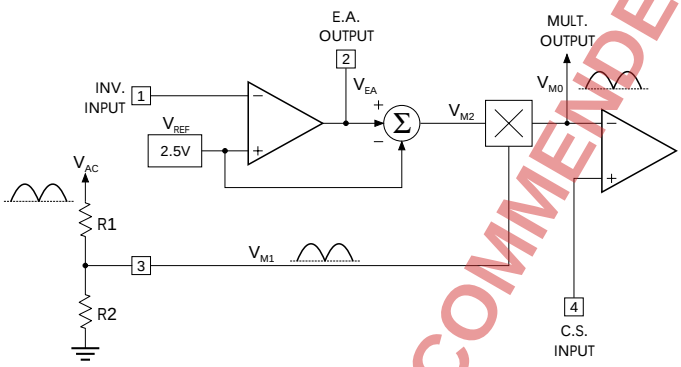


FIGURE 28 — MULTIPLIER SECTION

CURRENT SENSE COMPARATOR

Current sense comparator is configured as a PNP input differential stage with one input internally tied to the multiplier output and the other available for current sensing. Current is converted to voltage using an external sense resistor in series with the external power MOSFET. When sense voltage exceeds the threshold set by the multiplier output, the current sense comparator terminates the gate drive to the MOSFET and resets the PWM latch. The latch insures that the output remains in a low state after the switch current falls back to zero. The LX1562/63 features a leading edge blanking circuit that eliminates the need for an external RC filter otherwise required for proper operation of the circuit. This function is described in detail under "current detect logic" section.

The current sense comparator voltage is limited by an internal 1.24V (typ.) voltage clamp of the multiplier output. Therefore maximum switch current is typically given by:

$$I_{PK\ (MAX)} = 1.24V\ /\ R_S$$

Maximum switch peak current happens at full load and minimum line conditions.

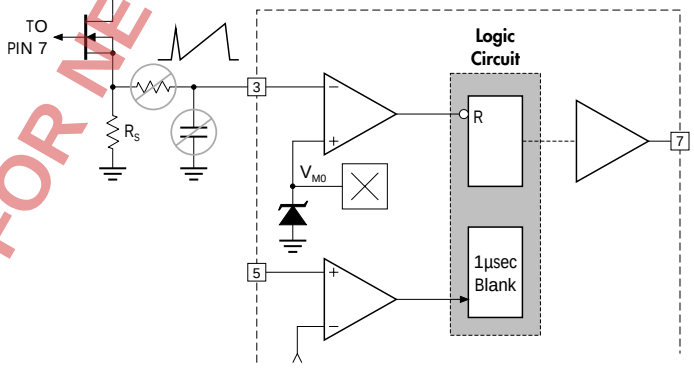


FIGURE 29 — CURRENT SENSE SECTION

CURRENT DETECT LOGIC

The function of "current detect logic" is to sense the operating state of the boost inductor and to enable the output driver accordingly. To achieve this, the downward slope of the inductor current is indirectly detected by monitoring the voltage across a separate winding and connecting it to the detector input "I_{DET}" pin. Once the inductor current reaches ground level, the voltage across the winding reverses polarity and changes the "I_{DET}" input and the comparator output to the low state (See Figure 30). When comparator changes state, it sets the latch and turns on the output driver for a period of 1µs (typ.) regardless of any changes in the latch output ($\overline{Q}$) within this period. This ensures that if the C.S. comparator changes state due to any turn-on spike, the driver output remains on and does not turn off prematurely.

However if the spike lasts longer than 1µs, the output driver turns off and the MOSFET stops conducting. This type of digital current sense blanking which is not amplitude dependent has higher noise immunity than the commonly used external RC filtering, allowing for more flexibility in board layout.

Since inductor voltage swings both positive and negative, internal voltage clamping is provided to protect the IC. The

IC DESCRIPTION

CURRENT DETECT LOGIC (continued)

upper 7.8V clamp prevents input overvoltage breakdown during switch off time, while during the on time the lower 0.7V clamp prevents substrate injection. An internal current limit resistor protects the lower clamp transistor in case the "I_{DET}" pin is accidently shorted to ground.

START-UP TIMER

A start-up timer circuit eliminates the need for an external oscillator when used in stand alone applications. The timer, as shown in Figure 30, provides a means to automatically start the pre converter if the latch output $\overline{Q}$ comes up in a wrong (HI) state. The timer capacitor ramps up and resets the latch to a low state, turning the output driver on.

OUTPUT DRIVER STAGE

The LX1562/63 output driver is designed for direct driving of an external power MOSFET. It is a totem pole stage with ±500mA peak current capability. This typically results in a 130ns rise and fall times into a 1000pF capacitive load. Additionally the output is held low during the undervoltage condition to ensure that the MOSFET remains in the off state until supply voltage reaches the start-up threshold.

Internal voltage clamping ensures that output driver is always lower than 13.8V (typ.) when supply voltage variation exceeds more than rated V_{GS} threshold (typ 20V) of the external MOSFET. This eliminates an external zener diode and extra power dissipation associated with it that otherwise is required for reliable circuit operation.

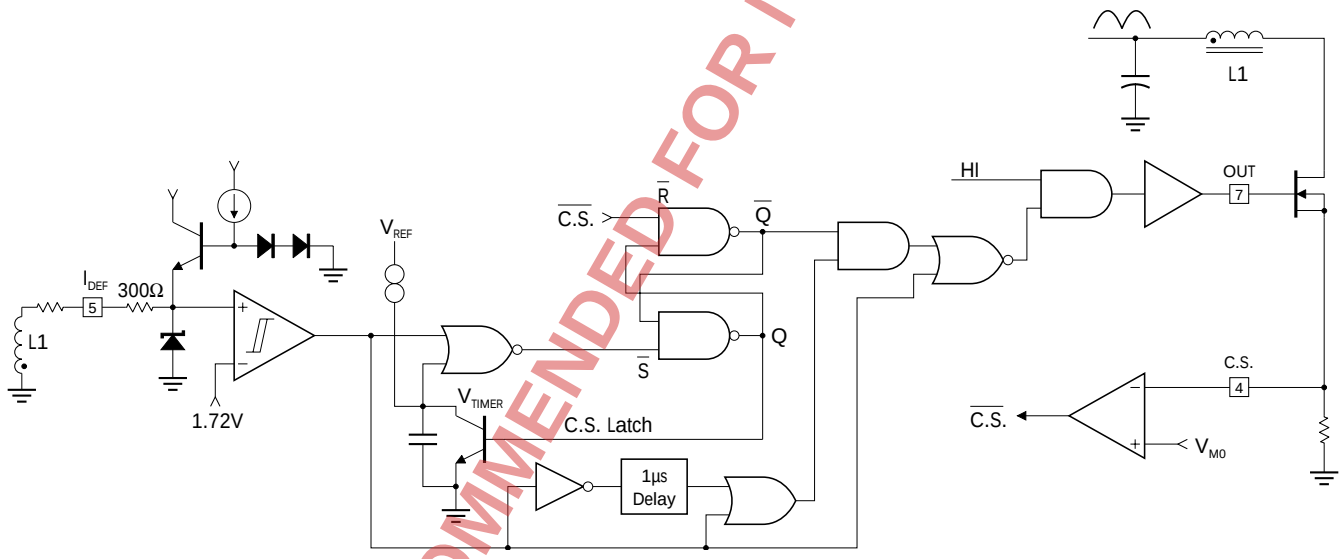


FIGURE 30 — START-UP TIMER & CURRENT DETECT LOGIC CIRCUITRY

APPLICATION INFORMATION

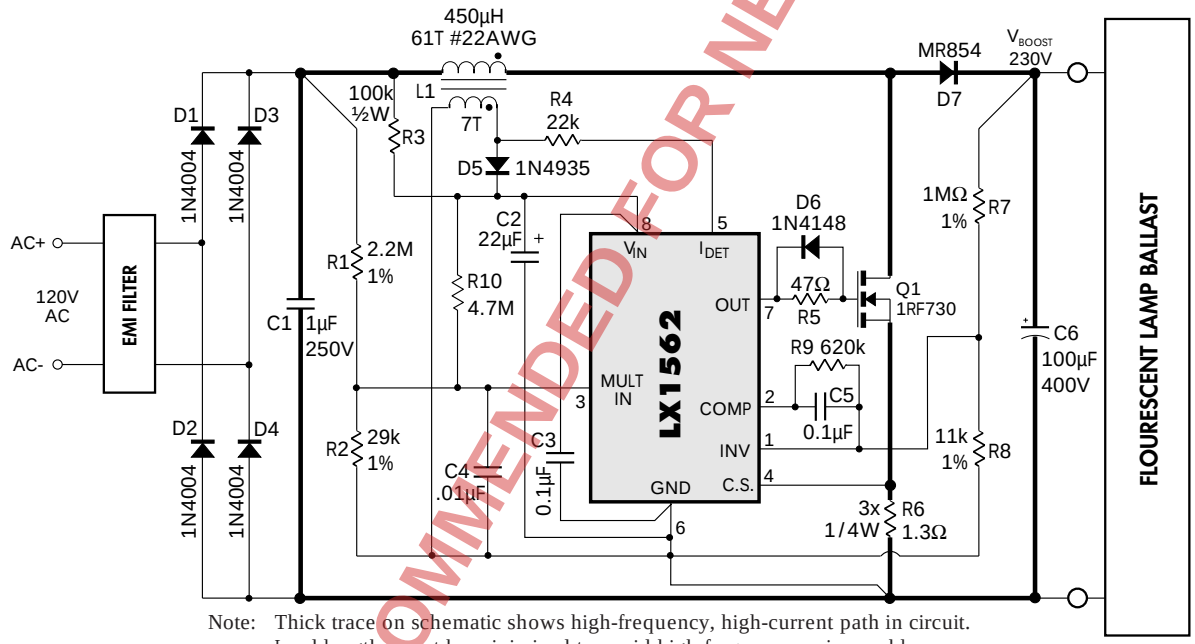
TYPICAL APPLICATION

The application circuit shown in Figure 31 uses the LX1562 as the controller to implement a boost type power factor regulator. The I.C. controls the regulator, such that the inductor current is always operating in a discontinuous conduction mode with no current gaps. This mode of operation has several advantages over the fixed frequency discontinuous conduction mode: 1) The switching frequency adjusts itself to the AC line envelope, causing a sinusoidal current draw, 2) Since there is no current gap between the switching cycles, the inductor voltage does not oscillate, causing less radiated noise, 3) The lower peak inductor current causes less power dissipation in the power MOSFET.

A set of formulas have been derived specifically for this mode, and are used throughout the design procedure. An example with the following specifications for the boost converter is given as:

Input Voltage Range	-	100 to 130V RMS
Output Power	-	80W
Efficiency	-	95% at full load
Power Factor	-	> 0.99 at full load
Total Harmonic Distortion	-	< 10% at full load

followed by a step by step design procedure which walks through component selection.



Note: Thick trace on schematic shows high-frequency, high-current path in circuit. Lead lengths must be minimized to avoid high-frequency noise problems.

FIGURE 31 — TYPICAL APPLICATION OF THE LX1562 IN AN 80W FLUORESCENT LAMP BALLAST WITH ACTIVE POWER FACTOR CONTROL

OUTPUT VOLTAGE REQUIREMENT

Since the converter is a boost type topology, it requires the output voltage to always be higher than the input voltage. It is recommended to select this voltage at least 15% higher than the maximum input voltage in order to: A) Avoid the inductor saturation during line transience, and B) To keep the operating frequency above the audible range at high line.

Figure 32 (next page) shows that when boost voltage is selected near the maximum AC line, the increase in off-time could reduce the operating frequency below the audible frequency and cause inductor humming. In fact, Figure 32 (next page) shows that for ±13% (100V to 130V) change in the line voltage the optimum range of the operating frequency is when off-time duty cycle (D') is between 0.57 and 0.75. This means that the boost voltage needs to be 245V when selecting D' = 0.75 at maximum AC line.

In this example, D' is chosen to be 0.8, to slightly reduce the voltage rating of the back end DC to AC fluorescent lamp inverter. This sets the boost voltage at:

$$V_O = \frac{130 * \sqrt{2}}{0.8} = 230V$$

APPLICATION INFORMATION

OUTPUT VOLTAGE REQUIREMENT (continued)

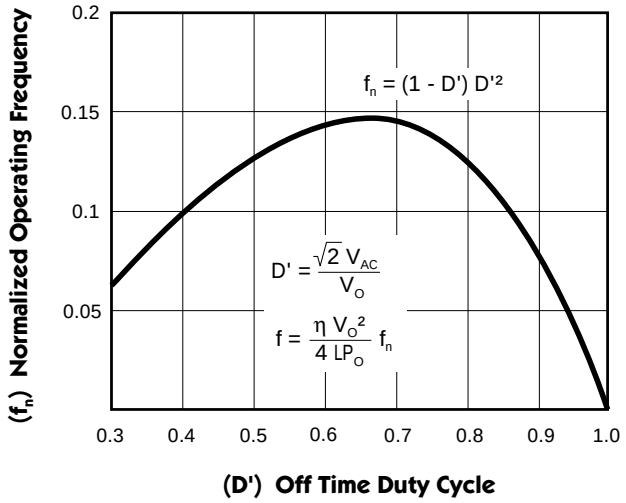


FIGURE 32 — NORMALIZED OPERATING FREQUENCY vs. OFF-TIME DUTY CYCLE

INDUCTOR PEAK CURRENT

It can be shown by referring to Figure 33 that the inductor peak current is always twice the average input current.

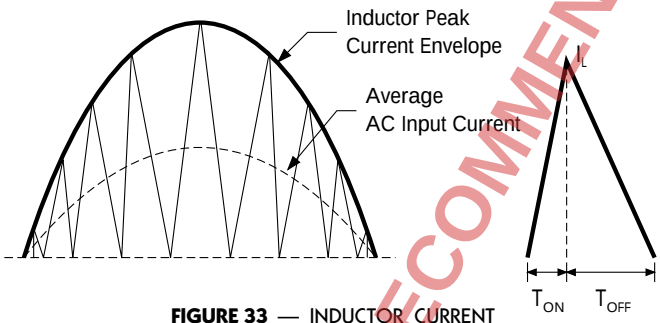


FIGURE 33 — INDUCTOR CURRENT

$$I_{IN(t)} = \sum AVE\ [\ I_L\ (t)\ ]$$

$$I_{IN} = \frac{1}{T}\left[\frac{(I_L)\ (T)}{2}\right] = \frac{I_L}{2}$$

$$I_{INpeak} = I_P = \frac{I_{LP}}{2}$$

I_{LP} = Inductor peak current at peak input voltage.

Maximum peak input current can be calculated using:

$$I_P = \frac{2P_O}{\eta V_P}$$

where: $\eta \equiv$ Converter efficiency
$V_P \equiv$ Peak AC input voltage

assuming: $\eta = 95\%$, $P_O = 80W$, $V_{Pmin} = 100\sqrt{2} = 141$

$$I_P = \frac{2 \times 80}{(.95)(141)} = 1.2A$$

$$I_{LP/min\ AC} = 2 * 1.2 = 2.4A$$

INDUCTOR DESIGN

The inductor value is calculated assuming a 50KHz operating frequency at the nominal AC voltage using the following equation:

$$L_1 = \frac{\eta\ \frac{V_O - V_P}{V_O}\ T\ V_P^2}{4\ P_O}$$

where: $\eta \equiv$ Efficiency
$V_O \equiv$ Output DC voltage
$V_P \equiv$ Peak AC input voltage
$T \equiv$ Switching period
$P_O \equiv$ Output Power

$$L_1 = \frac{.95\ (\frac{230 - 120\sqrt{2}}{230})\ 20 * 10^{-6} * (120\sqrt{2})^2}{4 * 80} = 448\mu H$$

choose T = 20µsec (50kHz)

Figure 32 shows that at nominal AC line (D' = 0.74) the normalized frequency is 0.142 and dropping to 0.13 at maximum line condition. This translates to a 10% drop in operating frequency which is still well above the audible range.

Once the inductance is known, we can either use the area product method (AP) or the K_g (based on copper losses method), for selecting proper core size. In this example, we apply the K_g approach using the following steps:

Step 1: Calculate K_g using

$$K_g = \frac{\Omega}{P_{CU}}\ (\frac{L_1 I_{LP}^2}{B})^2$$

where: $L_1 \equiv$ Required inductance
$\Omega \equiv 1.724 * 10^{-8}$ m
$B \equiv$ Maximum flux density
$I_{LP} \equiv$ Maximum peak inductor current
$P_{CU} \equiv$ Maximum copper dissipation

Assume: $P_{CU} = 1.6W$ (2% of total output)

$$K_g = \frac{1.724 * 10^{-8}}{1.6}\left[\frac{450 * 10^{-6} * (2.4)^2}{0.15}\right]^2 = 3.21 * 10^{-12}\ m^5$$

APPLICATION INFORMATION

INDUCTOR DESIGN (continued)

Step 2: Choose a core with higher K_g than the one calculated in Step 1.

$$K_g/\text{core} = k\,\frac{A_W A_E^2}{l_W}$$

where: k ≡ Winding coefficient (typ. k=0.4)
A_W ≡ Bobbin window area
A_E ≡ Effective core area
l_W ≡ Mean length per turn

K_g factor for TDK PQ2625:
$A_W = 47.7\text{mm}^2$
$A_E = 118\text{mm}^2$
$l_W = 56.2\text{mm}$

$$K_g = 0.4\,\frac{(47.7)\,(118)^2}{56.2}\,(\text{mm})^5 = 4.7 * 10^{-12}\ \text{m}^5$$

Step 3: Determine number of turns.

$$N = \frac{L\,I_{LP}}{B\,A_E}$$

$$N = \frac{450 * 10^{-6} * 2.4}{0.15 * 118 * 10^{-6}} = 61\ \text{turns}$$

$$A_{WIRE} = k\,\frac{A_W}{N} = 0.4\,\frac{47.7}{61} = 0.31\text{mm}^2 = 480\text{mil}^2$$

choose #22 AWG with r = 0.0165Ω/feet resistance.

$R_W = N * l_w * r$
$R_W = 0.185\Omega$

Step 4: Calculate air gap.

$$l_g = \frac{\mu_O\,N^2\,A_E}{L}$$

$$l_q = \frac{4\pi * 10^{-7} * (61)^2 * 118 * 10^{-6}}{450 * 10^{-6}} = 0.122\text{cm} = 48\ \text{mil}$$

CURRENT SENSE RESISTOR

Current sense resistor, R6 is selected using the minimum multiplier output clamp voltage and the maximum inductor peak current such that:

$$R6 = \frac{V_{CLAMP(MIN)}}{I_{L\,(MAX)}} = \frac{1.1}{2.4} = 0.45\Omega$$

Power dissipation is approximated by:

$$P_R \approx \frac{1}{6}\,I_{2\,(MAX)}{}^2\,(1 - D'_{MIN}), \quad \text{where } D'_{MIN} = 1 - \frac{\sqrt{2}\,V_{AC(MIN)}}{V_{BOOST}}$$

$$P_R \approx \frac{1}{6}\,(2.4)^2\ \ (1 - 0.61) = 0.374$$

Select **THREE** 1.3Ω, ¼W carbon comp resistors in parallel.

MULTIPLIER COMPONENT SELECTION

Calculate R1 & R2 resistor values such that under low line AC input the multiplier output is lower than the minimum clamp voltage.

$$\frac{R2}{R1 + R2} * \sqrt{2}\,V_{AC\,(MIN)} * K * (V_{EA0\,(MAX)} - V_{REF}) < V_{CLAMP\,(MIN)}$$

where: K ≡ Mult. Gain
$V_{EA)(MAX)}$ ≡ Maximum error amp output where multiplier is still in linear range. This voltage is ≈ 3.5V.

For K = 0.65 & $V_{CLAMP\,(MIN)}$ = 1.1V, the ratio of R1/R2 is:

$$\frac{R1}{R2} > 83$$

Assuming R1 is selected to be:

* **R1 = 2.2M (1%)**

$$R2 = \frac{2.2M}{83} = \textbf{26.4k (1%)} \qquad \text{select } \mathbf{R_2 = 26.7k\ (1\%)}$$

* For high input applications such as 277V, R1 must be divided into two resistors in series to meet the maximum rated voltage of the resistors.

To improve THD further (typ. 2-3%), a high value resistor can be connected from the supply voltage to this pin to allow an increase in the switch on-time at the zero crossing by adding an effective offset at the multiplier output.

ERROR AMPLIFIER COMPONENT SELECTION

Boost voltage is programmed with R7 & R8 resistor dividers using the following equation:

$$\frac{R7}{R8} = \frac{V_{BOOST}}{V_{REF}} - 1,$$

assuming that the product of R7 and the E.A. input bias current does not cause significant error in the output voltage setting.

Assuming **R7 = 1MΩ** (for output voltage of higher than 250V, two resistors may be added in series to meet the voltage requirement of the resistor.)

$\Delta V_{ERROR}\ (10^6)\ (0.5 * 10^{-6}) = 0.5\text{V}$, which is < 0.25% of the output voltage.

Calculating R8:

$$R8 = \frac{R7}{\frac{V_{BOOST}}{V_{REF}} - 1} = \textbf{11k (1%)}$$

Worst case output tolerance is the total of ±3.75% which is the sum of ±1.5% (Ref), ±2% (resistor dividers), and ±0.25% (E.A. input bias current).

APPLICATION INFORMATION

ERROR AMPLIFIER COMPONENT SELECTION (continued)

Capacitor C5 is primarily selected to reject the output ripple associated with twice the line frequency. For a 40dB ripple rejection:

$$C5 \geq \frac{100}{2\pi f_l R7} \qquad \text{where } f_l = 2x \text{ line frequency}$$

$$C5 \geq \frac{100}{2\pi * 120 * 2.2 * 10^6} = 0.062\mu F, \quad \text{Select } \mathbf{C5 = 0.1\mu F}$$

Resistor R9 can be used to improve load transient response at the cost of loosing 1 or 2% of load regulation. The value of this resistor should be much greater than R8:

R9 = 620k

One way of achieving desired load transient response without resorting to a complex mathematical model of the converter, is to dynamically switch the output load and empirically find the compensation network. The value of resistor R9 is selected using the method shown in Figure 34.

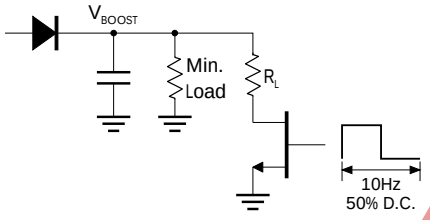


FIGURE 34 — LOAD TRANSIENT RESPONSE CIRCUIT

I_{DETECT} COMPONENT SELECTION

Figure 35 shows voltage envelope generated by flyback voltage across I_{DET} winding:

Select turns ratio n such that,

$$n = \frac{5V}{V_{BOOST} - \sqrt{2}\, V_{AC\,(MAX)}}$$

$$n = \frac{5V}{230 - \sqrt{2} * 130} = 0.11$$

I_{DET} winding turns are selected to be 7T.

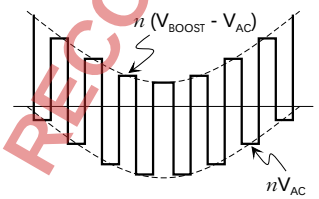


FIGURE 35 — FLYBACK VOLTAGE ACROSS I_{DET} WINDING

and R4 resistor:

$$\frac{n * V_{BOOST}}{3 * 10^{-3}} < R4 < 500k$$

$$\frac{0.11 * 230}{3 * 10^{-3}} < R4 < 500k, \text{ or} \qquad 8.4k < R4 < 500k$$

Select **R4 = 22k**

SUPPLY VOLTAGE

Resistor R3 must be selected such that it ensures converter start-up at low line and is rated for high line power dissipation.

$$R3 < \frac{\sqrt{2}\, V_{AC\,(MIN)}}{I_{ST\,(MAX)}}$$

where: I_{ST} ≡ Maximum start-up current
V_{ST} ≡ Start-up voltage
$T_{ST(MAX)}$ ≡ Maximum start-up time at AC power-on

$$R3 < \frac{\sqrt{2} * 100}{0.3 * 10^{-3}} = 466k\Omega$$

$$R3 > 4\, V_{AC\,(MAX)} \quad \text{(to keep power dissipation below 0.5W)}$$

$$R3 > 68k, \quad \text{select } \mathbf{R3 = 120k.}$$

Start-up time of converter is given by:

$$T_{ST\,(MAX)} \approx C2 \frac{V_{ST}}{\frac{\sqrt{2}\, V_{AC\,(MIN)}}{R3} - I_{ST}}$$

for our application this will be 25ms/µF.

The start-up capacitor is selected such that capacitor discharge time is always longer than the time it takes for the bootstrap voltage to reach above the minimum start-up threshold of the IC.

$$C3 < \frac{I_{OP} * \Delta t}{\Delta V_{MIN}}$$

where: I_{OP} ≡ Maximum dynamic supply current of the IC
Δt ≡ Rise time of the bootstrap voltage
ΔV_{MIN} ≡ Minimum hysteresis voltage (4V for 1562, 1.7V for 1563)

$$C3 < \frac{10 * 10^{-3} * 10 * 10^{-3}}{4} = 29\mu F$$

Select **C3 = 33µF.**

Start-up time is approximately 0.8 seconds.

The auxiliary winding turns are selected such that it provides 15V of operating voltage.

$$N_S \approx N_P * \frac{V_S}{V_O} = 61 * \frac{V_S}{V_O} = 4T$$

However, in this example I_{DETECT} winding is used to power the IC which eliminates the need for a third winding. This is possible since the internal clamping of the output drive limits the gate drive voltage to 14V (typ.) if the supply voltage exceeds this limit.

APPLICATION INFORMATION

POWER MOSFET SELECTION

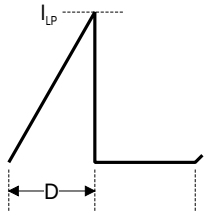
The voltage rating of MOSFET and rectifier must be higher than the maximum value of the output voltage.

$V_{DS} \geq 1.2\ V_{O\ MAX}$ $\quad V_{DS} \geq 282V$

The RMS current can be approximated by multiplying the RMS current at the peak of the line by 0.7.

$I_{RMS} = 0.7\ I_{LP}\ \sqrt{D/3}$ $\quad$ D ≡ On-time duty cycle

D = 0.39 at V_{AC} = 100V
I_{LP} = 2.4A



$I_{RMS} = (0.7)(2.4)(\sqrt{.39/3}) = 0.61A$

$$R_{DS} \leq \frac{P_{DC}}{I_{RMS}^2}$$

P_{DC} ≡ allowable power dissipation.

I_{RMS}/triangle = $I_{LP}\ \sqrt{D/3}$

$$R_{DS} \leq \frac{1}{0.61} = 1.6\Omega$$

IRF730 with R_{DS} = 1Ω and V_{DS} = 400V meets the above requirements.

INPUT RECTIFIER AND CAPACITOR SELECTION

The current through each diode is a half-wave rectified sine wave. The maximum current happens at minimum line with a peak value of 1.2A.

$$I_{AVE} = \frac{I_{PEAK}}{\pi} = \frac{1.2}{\pi} = 0.38A$$

choose **1N4004 with 1A rating.**

$P_{DISS} = (I_{AVE})\ (V_F) = 0.38 \times 0.9 = 0.344W$

$T_J = T_A + P_D \times \theta_{JA}$ $\quad$ assuming θ_{JA} = 65°C/W for 1/8" lead length.

$T_J = 80 + (.344)(65) = 102°C$

Assuming φ is the percentage of allowable input current ripple, C1 can be calculated using the following equations:

$$R_{EFF} = \frac{2\ P_O}{\eta\ I_P^2}$$

$$C1 \geq \frac{1}{\varphi\ 2\pi\ R_{EFF}\ f_{SW}}$$

f_{SW} ≡ Switching frequency of inductor current at peak input voltage.

if φ = 3%

$$R_{EFF} = \frac{2 \times 80}{(.95)(1.2)^2} = 117\Omega$$

$$C1 \geq \frac{1}{(.03)(2\pi)(117)(50000)} = 0.9\mu F$$

choose **1µF, 250V capacitor**.

OUTPUT CAPACITOR SELECTION

There are mainly two criteria for selecting the output capacitor: A large enough capacitance to maintain a low ripple voltage, and a low ESR value in order to prevent high power dissipation due to RMS currents.

The output capacitance can be approximated from the following equation:

$$C6 \geq \frac{I_{DC}}{2\pi\ f_{LINE}\ \Delta V}$$

where: I_{DC} ≡ DC output current
DV ≡ Output ripple

$$I_{DC} = \frac{80}{230} = 0.348A$$

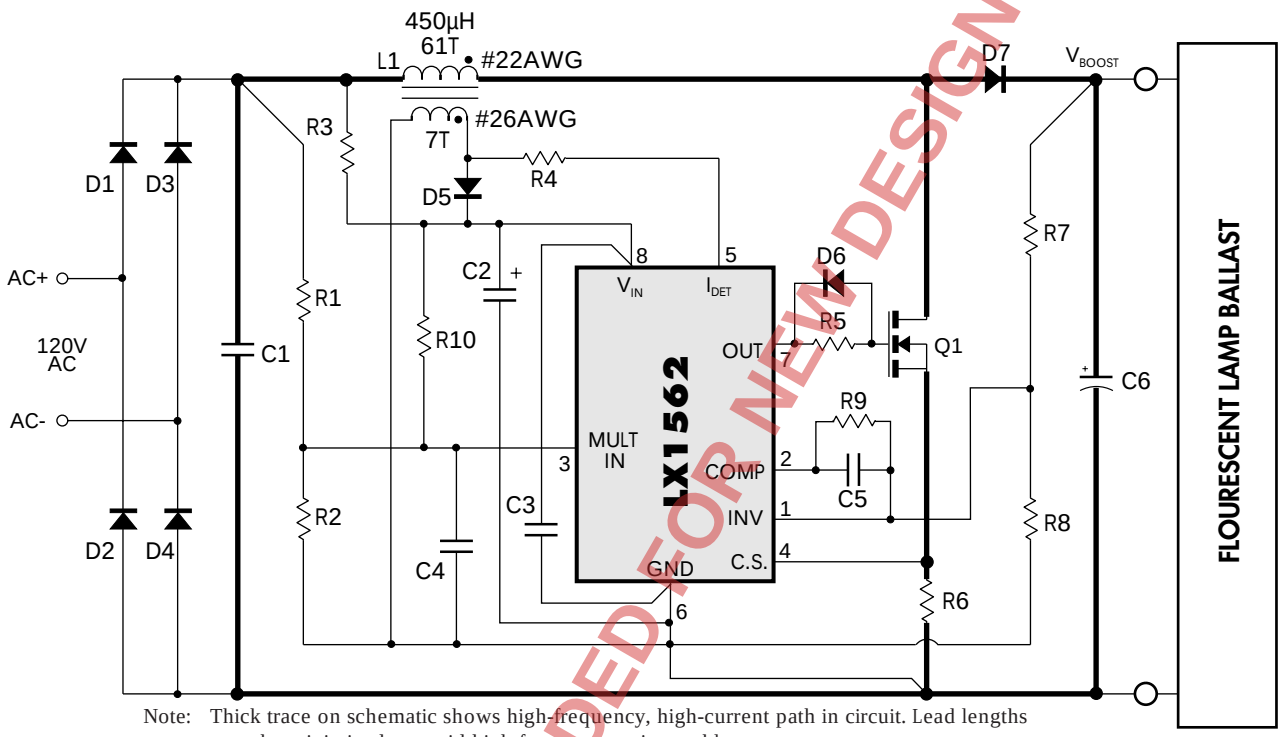
assuming 5% peak to peak ripple,

$$C6 \geq \frac{0.348}{2\pi\ (60)\ (11.5)} = 81\mu F$$

choose **C6 = 100µF**.

TYPICAL APPLICATIONS

120V



Note: Thick trace on schematic shows high-frequency, high-current path in circuit. Lead lengths must be minimized to avoid high-frequency noise problems.

FIGURE 36 — TYPICAL APPLICATION OF THE LX1562 IN AN 80W FLUORESCENT LAMP BALLAST WITH ACTIVE POWER FACTOR CONTROL.

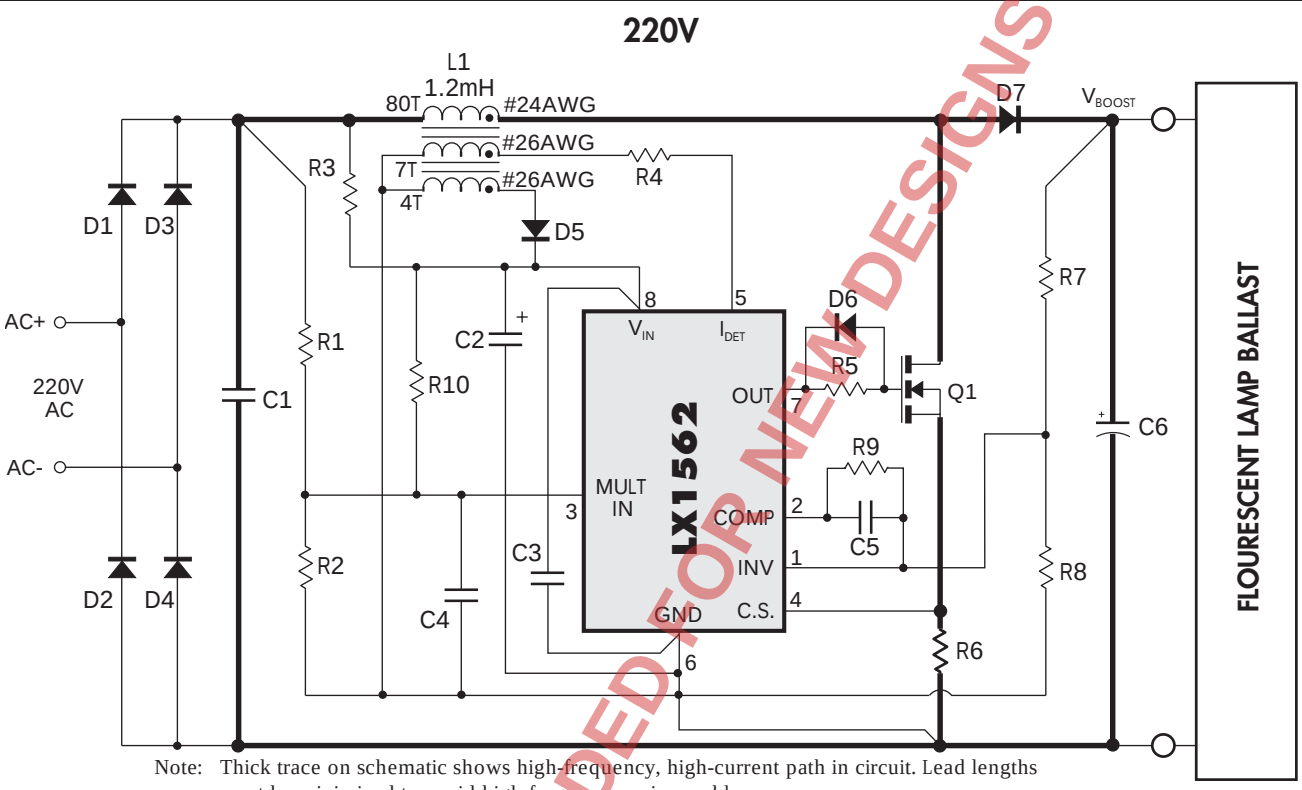
Electrical Specifications

120VAC Input — 230VDC / 80W Output

Ref.	Component	Manuf.	Ref.	Component	Manuf.
IC	LX1562	Linfinity	C1	QXF2E105KRPT	
L1	PQ2625/H7C1 Core	TDK		1µF/250V - Plastic Film (high freq.)	Nichicon
Q1	IRF730, 400V, 1Ω rds	I.R.	C2	22µF/35V - Electrolytic	
D1-D4	IN4004 1A, 400V	Motorola	C3	0.1µF/50V - Ceramic	
D5	1N4935 1A	Motorola	C4	0.01µF/50V - Ceramic	
D6	1N4148 (improves Q1 power dissipation)	Motorola	C5	0.1µF/50V - Ceramic	
D7	MR854, 3A, 400V	Motorola	C6	LGQ2G101MHS A/Z*	Nichicon
R1	2.2MΩ, ±1%			100µF/400V - Electrolytic	
R2	26.7kΩ, ±1%				
R3	100kΩ, ½W			* A = 25mm diam.	
R4	22kΩ			Z = 22mm diam.	
R5	47Ω				
R6	1.5Ω, Carbon type (3X)				
R7	1MΩ, 1%				
R8	11kΩ, 1%				
R9	620kΩ (improves load transient response)				
R10	4.7MΩ				

A complete evaluation board is available from Linfinity Microelectronics Inc.

TYPICAL APPLICATIONS



Note: Thick trace on schematic shows high-frequency, high-current path in circuit. Lead lengths must be minimized to avoid high-frequency noise problems.

FIGURE 37 — TYPICAL APPLICATION OF THE LX1562 IN AN 80W FLUORESCENT LAMP BALLAST WITH ACTIVE POWER FACTOR CONTROL.

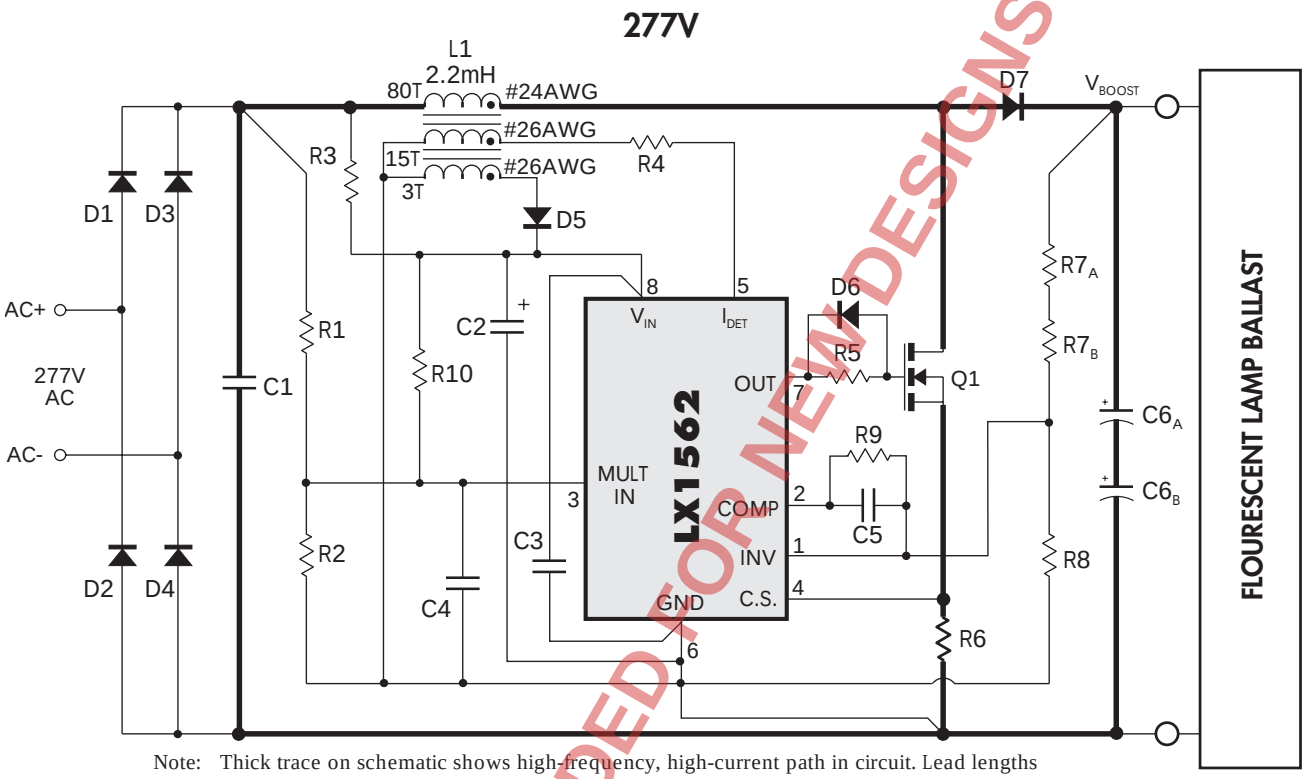
Electrical Specifications

220VAC Input — 400VDC / 80W Output

Ref.	Component	Manuf.	Ref.	Component	Manuf.
IC	LX1562	Linfinity	C1	QXF2J224KRPT	
L1	PQ2625/H7C1 Core	TDK		0.22µF/630V - Plastic Film	Nichicon
Q1	IRF830, 500V, 1.5Ω rds	I.R.	C2	22µF/35V - Electrolytic	
D1-D4	IN4007 1A, 1000V	Motorola	C3	0.1µF/50V - Ceramic	
D5	1N4935 1A	Motorola	C4	0.01µF/50V - Ceramic	
D6	1N4148 (improves Q1 power dissipation)	Motorola	C5	0.1µF/50V - Ceramic	
D7	MR856, 3A, 600V	Motorola	C6*	LGQ2W680MHS A/Z*	Nichicon
R1	2.2MΩ, ±1%			68µF/450V - Electrolytic	
R2	12kΩ, ±1%				
R3	220kΩ, ½W			* A = 25mm diam.	
R4	22kΩ			Z = 22mm diam.	
R5	47Ω				
R6	1.8Ω, Carbon type (2X)				
R7	1MΩ, 1%				
R8	6.19kΩ, 1%				
R9	620kΩ (improves load transient response)				
R10	2.7MΩ				

A complete evaluation board is available from Linfinity Microelectronics Inc.

TYPICAL APPLICATIONS



Note: Thick trace on schematic shows high-frequency, high-current path in circuit. Lead lengths must be minimized to avoid high-frequency noise problems.

FIGURE 38 — TYPICAL APPLICATION OF THE LX1562 IN AN 80W FLUORESCENT LAMP BALLAST WITH ACTIVE POWER FACTOR CONTROL.

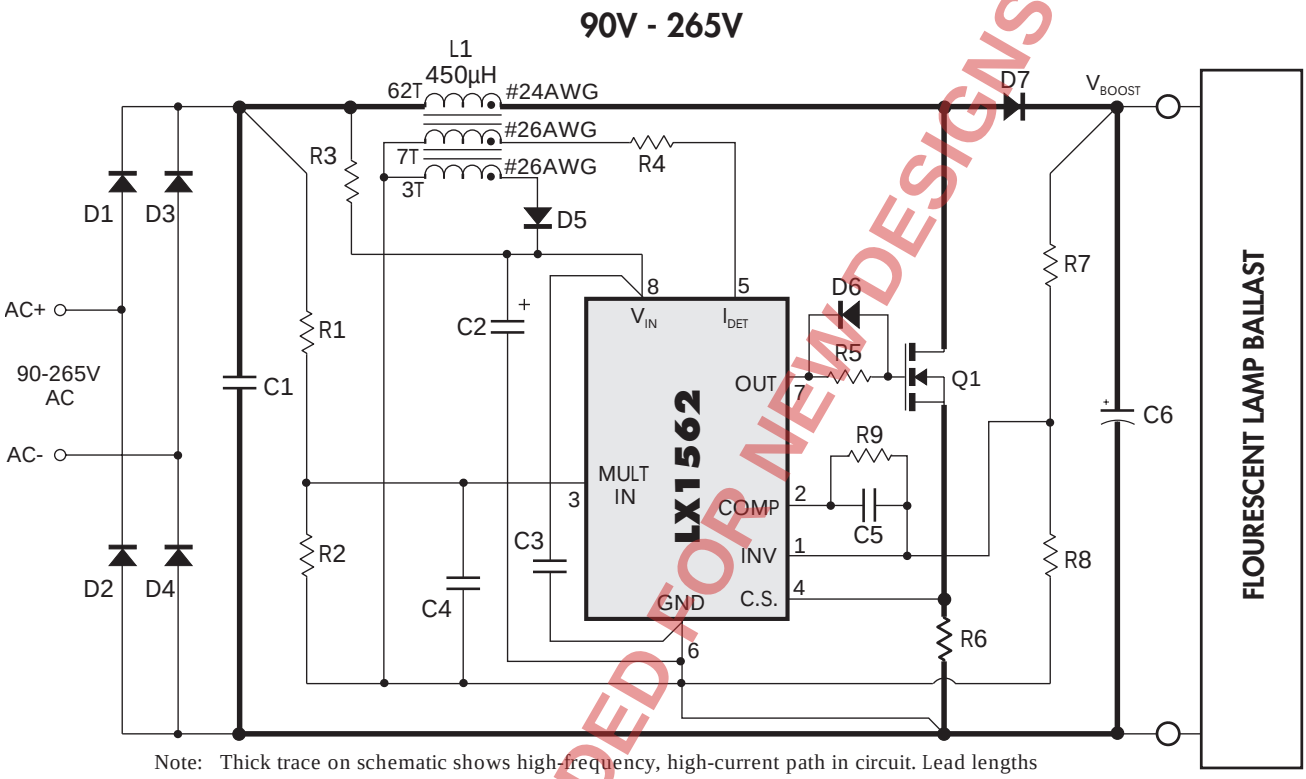
Electrical Specifications

277VAC Input — 480VDC / 80W Output

Ref.	Component	Manuf.	Ref.	Component	Manuf.
IC	LX1562	Linfinity	C1	QXF2J224KRPT	
L1	PQ2625/H7C1 Core	TDK		0.22µF/630V - Plastic Film	Nichicon
Q1	IRF830, 500V, 1.5Ω rds	I.R.	C2	22µF/35V - Electrolytic	
D1-D4	IN4007 1A, 1000V	Motorola	C3	0.1µF/50V - Ceramic	
D5	1N4935 1A	Motorola	C4	0.01µF/50V - Ceramic	
D6	1N4148 (improves Q1 power dissipation)	Motorola	C5	0.22µF/50V - Ceramic	
D7	MR856, 3A, 600V	Motorola	C6	UVZ2F470MEH (2X)	Nichicon
R1	2.2MΩ, ±1%			47µF/315V - Electrolytic	
R2	10kΩ, ±1%				
R3	390kΩ, ½W				
R4	22kΩ				
R5	47Ω				
R6	2.2Ω, Carbon type (2X)				
R7	499kΩ, 1% (2X)				
R8	5.23kΩ, 1%				
R9	620kΩ (improves load transient response)				
R10	2.2MΩ				

A complete evaluation board is available from Linfinity Microelectronics Inc.

TYPICAL APPLICATIONS



Note: Thick trace on schematic shows high-frequency, high-current path in circuit. Lead lengths must be minimized to avoid high-frequency noise problems.

FIGURE 39 — TYPICAL APPLICATION OF THE LX1562 IN AN 80W FLUORESCENT LAMP BALLAST WITH ACTIVE POWER FACTOR CONTROL.

Electrical Specifications

90-265VAC Input — 400VDC / 80W Output

Ref.	Component	Manuf.	Ref.	Component	Manuf.
IC	LX1562	Linfinity	C1	QXF2J224KRPT	
L1	PQ2625/H7C1 Core	TDK		0.47µF/630V - Plastic Film	Nichicon
Q1	IRF840, 500V, 1Ω rds	I.R.	C2	22µF/35V - Electrolytic	
D1-D4	IN4007 1A, 1000V	Motorola	C3	0.1µF/50V - Ceramic	
D5	1N4935 1A	Motorola	C4	0.01µF/50V - Ceramic	
D6	1N4148 (improves Q1 power dissipation)	Motorola	C5	0.33µF/50V - Ceramic	
D7	MR856, 3A, 600V	Motorola	C6*	LGQ2W680MHS A/Z*	Nichicon
R1	2.2MΩ, ±1%			68µF/450V - Electrolytic	
R2	16.3kΩ, ±1%				
R3	130kΩ, ½W			* A = 25mm diam.	
R4	22kΩ			Z = 22mm diam.	
R5	47Ω				
R6	1Ω, Carbon type (4X)				
R7	1MΩ, 1%				
R8	6.19kΩ, 1%				
R9	620kΩ (improves load transient response)				

A complete evaluation board is available from Linfinity Microelectronics Inc.