Le7942B

Subscriber Line Interface Circuit

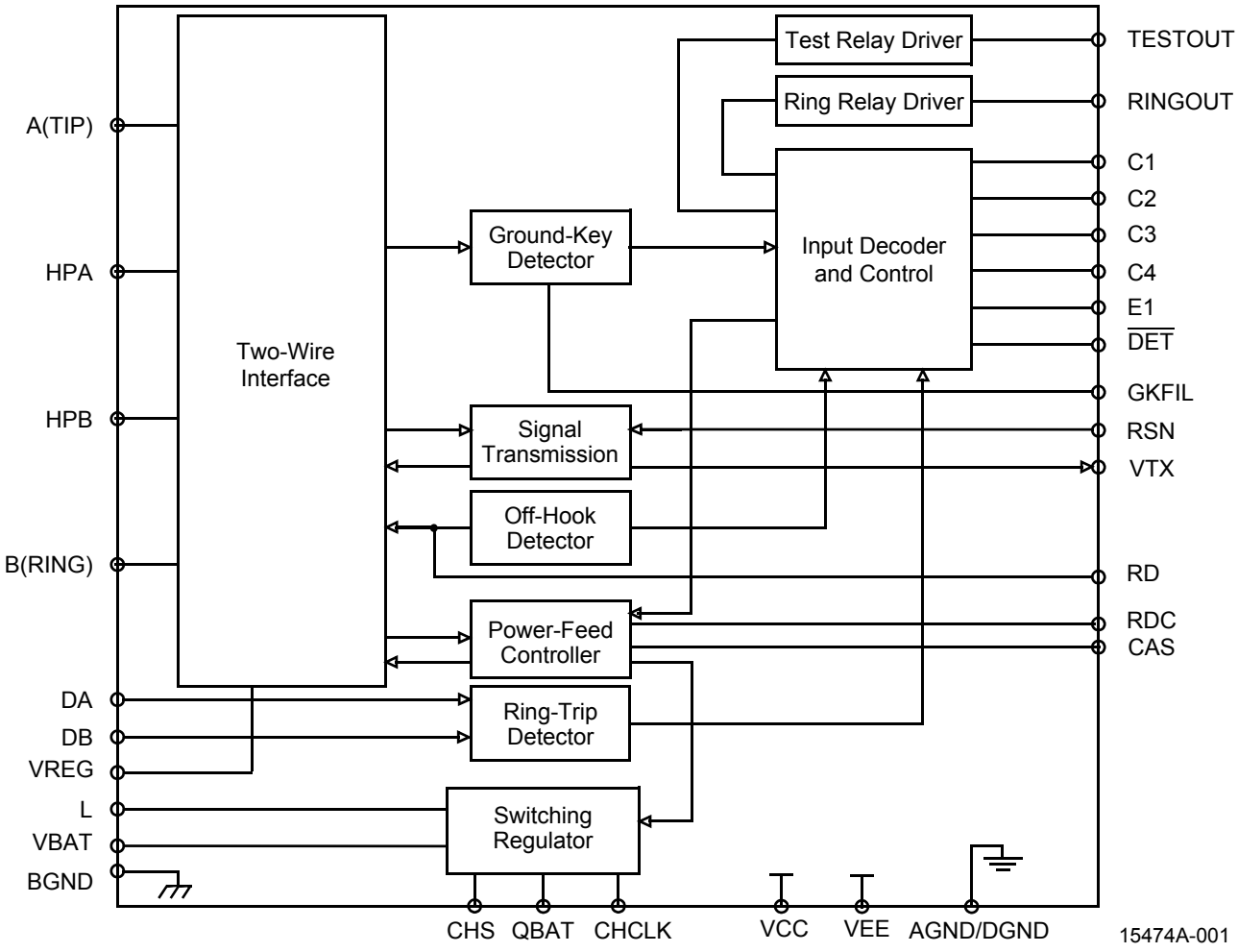
VE580 Series

A Legerity Voice Solution

DISTINCTIVE CHARACTERISTICS

- Programmable constant-current feed
- Receive current gain = 500
- Programmable loop-detect threshold
- Low standby power
- Performs polarity reversal
- Ground-key detector
- Pin for external ground-key noise filter capacitor
- Test relay driver option
- Compatible with Le7942 Device
- Tip Open state for ground-start lines
- –19 V to –58 V battery operation
- Ideal for PBX and KTS applications
- On-chip switching regulator for low-power dissipation
- Can be used with or without the on-chip switching regulator
- On-hook transmission

BLOCK DIAGRAM



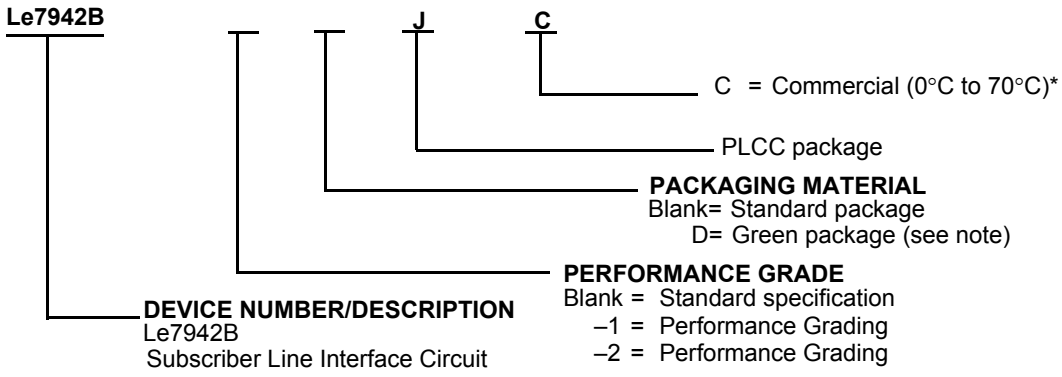
NOTE: On August 3, 2007, Zarlink Semiconductor acquired the products and technology of Legerity Holdings.

Document ID#	081195	Date:	Sep 19, 2007
Rev:	E	Version:	2
Distribution:	Public Document		

ORDERING INFORMATION

Standard Products

Legerity standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Note: The green package meets RoHS Directive 2002/95/EC of the European Council to minimize the environmental impact of electrical equipment.

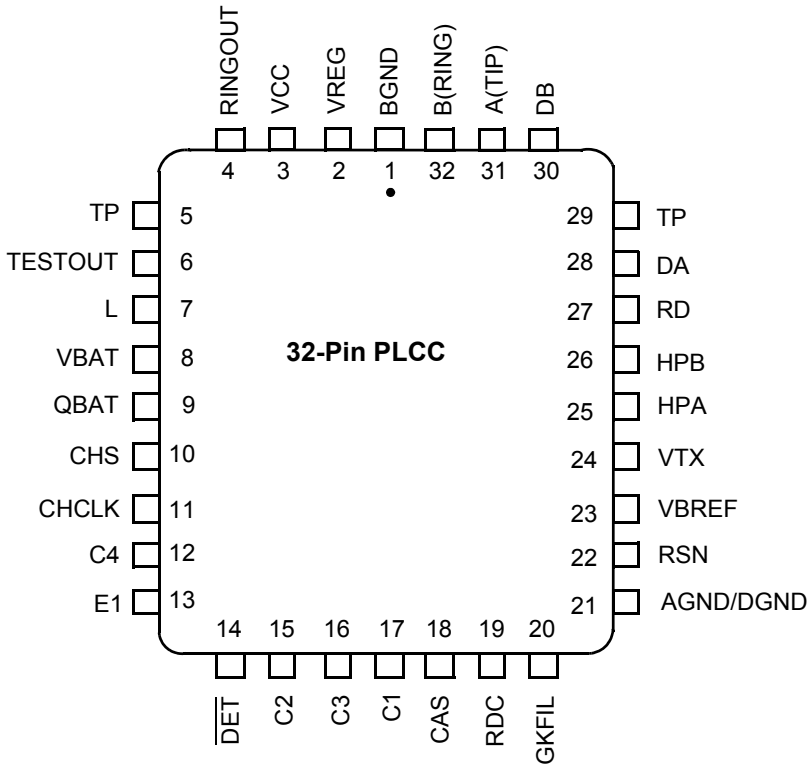
Valid Combinations
Green Package
Le7942BDJC
Le7942B–1DJC
Le7942B–2DJC
Non-Green Package
Le7942BJC
Le7942B-1JC
Le7942B-2JC

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local Legerity sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on Legerity's standard military–grade products.

CONNECTION DIAGRAMS

Top View



Notes:

1. *Pin 1 is marked for orientation.*
2. *TP is a thermal conduction pin tied to substrate (QBAT).*

PIN DESCRIPTIONS

Pin Names	Type	Description
AGND/DGND	Gnd	Analog and Digital ground.
A (TIP)	Output	Output of A(TIP) power amplifier.
BGND	Gnd	Battery (power) ground.
B (RING)	Output	Output of B(RING) power amplifier.
C3–C1	Input	Decoder. TTL compatible. C3 is MSB and C1 is LSB.
C4	Input	Test Relay Driver Command. TTL compatible. A logic Low enables the driver.
CAS	Capacitor	Anti-saturation pin for capacitor to filter reference voltage when operating in anti-saturation region.
CHCLK	Input	Chopper Clock. Input to switching regulator (TTL compatible). Freq = 256 kHz (typ). (See Note 1).
CHS	Input	Chopper Stabilization. (See Note 1) Connection for external chopper stabilizing components.
DA	Input	Ring-trip negative. Negative input to ring-trip comparator.
DB	Input	Ring-trip positive. Positive input to ring-trip comparator.
$\overline{\text{DET}}$	Output	Switchhook detector. When enabled, a logic Low indicates the selected detector is tripped. The detector is selected by the logic inputs (C3–C1, E1). The output is open-collector with a built-in 15 kΩ pull-up resistor.
E1	Input	Ground-Key Enable. E1 = High connects the ground-key detector to $\overline{\text{DET}}$. E1 = Low connects the off-hook or ring-trip detector to $\overline{\text{DET}}$.
GKFIL	—	Connection for external ground-key, noise-filter capacitor. (See Note 2.)
HPA	Capacitor	High-Pass Filter Capacitor. A(TIP) side of high-pass filter capacitor.
HPB	Capacitor	High-Pass Filter Capacitor. B(RING) side of high-pass filter capacitor.
L	Output (See Note 1)	Switching Regulator Power Transistor. Connection point for filter inductor and anode of Switching Regulator Power Transistor. Connection point for filter inductor and anode of catch diode. Has up to 60 V of pulse waveform on it and must be isolated from sensitive circuits. Keep the diode connections short because of the high currents and high di/dt.
QBAT	Battery	Quiet Battery. (See Note 1). Filtered battery supply for the signal processing circuits.
RD	Resistor	Detector resistor. Detector threshold set and filter pin. May be connected to ground or -5V.
RDC	Resistor	DC feed resistor. Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN).
RINGOUT	Output	Ring Relay Driver. Open-collector driver with emitter internally connected to BGND. (See Note 3)
RSN	Input	Receive Summing Node. The metallic current (AC and DC) between A(TIP) and B(RING) is equal to 500 x the current into this pin. The networks that program receive gain, two-wire impedance, and feed current all connect to this node.
TESTOUT	Output	Test Relay Driver. Open collector driver with emitter internally connected to BGND. (See Note 3)
TP	Thermal	Thermal pin. Connection for heat dissipation. Internally connected to substrate (QBAT). Leave as open circuit or connected to QBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation.
VBAT	Battery	Battery supply.
VCC	Power	+5 V power supply.
VBREF	Power	Reference voltage. No current on the pin. May be connected to QBAT or –5 V.
VREG	Input	Regulated Voltage. (See Note 1.) Provides negative power supply for power amplifiers. Connection point for inductor, filter capacitor, and chopper stabilization.
VTX	Output	Transmit Audio. This output is a unity gain version of the A(TIP) and B(RING) metallic voltage. VTX also sources the two-wire input impedance programming network.

Notes:

1. *All pins, except CHCLK, connect to VBAT when using SLIC without a switching regulator. CHCLK is connected to AGND/DGND.*
2. *To prevent noise pickup by the detection circuits when using Ground-Key Detect state (E1 = logical 1), a 3300 pF minimum bypass capacitor is recommended between the GKFIL pin and ground.*
3. *Each relay driver has a zener clamp to BGND.*

ABSOLUTE MAXIMUM RATINGS

Storage temperature . . . . . –55°C to +150°C

V_{CC} with respect to AGND/DGND . . .–0.4 V to +7.0 V

V_{EE} with respect to AGND/DGND . . . +0.4 V to QBAT

V_{BAT} with respect to AGND/DGND. . . +0.4 V to –70 V

Note: *Rise time of V_{BAT} (dv/dt) must be limited to 27 V/μs or less when Q_{BAT} bypass = 0.33 μF.*

BGND with respect to AGND/DGND .+1.0 V to –3.0 V

A(TIP) or B(RING) to BGND:

Continuous . . . . . –70 V to +1.0 V

10 ms (f = 0.1 Hz) . . . . . –70 V to +5.0 V

1 μs (f = 0.1 Hz) . . . . . .–90 V to +10 V

250 ns (f = 0.1 Hz) . . . . . .–120 V to +15 V

Current from A(TIP) or B(RING). . . . . .±150 mA

Voltage on RINGOUT, TESTOUT . . . .BGND to + 7 V

Voltage on RINGOUT, TESTOUT (transient) . . . . . BGND to +10 V

Current through relay drivers . . . . . 60 mA

Voltage on ring-trip inputs (DA and DB) . . . . . V_{BAT} to 0 V

Current into ring-trip inputs . . . . . .±10 mA

Peak current into regulator switch (L pin). . . . . 150 mA

Switcher transient peak off voltage on L pin. . . . . +1.0 V

C4–C1, E1, CHCLK to AGND/DGND . . . . . .–0.4 V to V_{CC} + 0.4 V

Maximum power dissipation, T_A (see note) . . . . .70°C

In 32-pin PLCC package. . . . . 1.74 W

Note: *Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never be exposed to this temperature. Operation above 145°C junction temperature may degrade device reliability. See the SLIC Packaging Considerations for more information.*

Stresses above those listed under Absolute Maximum Ratings cancause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient temperature . . . . . 0°C to +70°C*

V_{CC} . . . . . 4.75 V to 5.25 V

V_{EE} . . . . . .–4.75 V to QBAT

V_{BAT}. . . . . .–19 V to –58 V**

AGND/DGND . . . . . 0 V

BGND with respect to AGND/DGND. . . . . –100 mV to +100 mV

Load Resistance on VTX to ground . . . . . 10 kΩ min

The Operating Ranges define those limits between which the functionality of the device is guaranteed.

**Legerity guarantees the performance of this device over commercial (0 to 70°C) and industrial (-40 to 85 °C) temperature ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore TR-TSY-000357 Component Reliability Assurance Requirements for Telecommunications Equipment.*

***Can be used without switching regulator components in this range of battery voltages, provided maximum power dissipation specifications are not exceeded.*

Package Assembly

The non-green package devices are assembled with industry-standard mold compounds, and the leads possess a tin/lead (Sn/Pb) plating. These packages are compatible with conventional SnPb eutectic solder board assembly processes. The peak soldering temperature should not exceed 225°C during printed circuit board assembly.

The green package devices are assembled with enhanced environmental compatible lead-free, halogen-free, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes. The peak soldering temperature should not exceed 245°C during printed circuit board assembly.

Refer to IPC/JEDEC J-Std-020B Table 5-2 for the recommended solder reflow temperature profile

ELECTRICAL CHARACTERISTICS

Description	Test Conditions (See Note 1)	Grade	Min	Typ	Max	Unit	Note
Analog (V_{TX}) output impedance		all	3	—		Ω	4
Analog (V_{TX}) output offset	0°C to +70°C	–1 –2	–35 –35 –30	—	+35 +35 +30	mV	—
	–40°C to +85°C	–1 –2	–40 –40 –35	—	+40 +40 +35		4
Analog (RSN) input impedance	300 Hz to 3.4 kHz	all	—	1	20	Ω	—
Longitudinal impedance at A or B		all	—	—	35		—
Overload level	4-wire 2-wire	all	–2.5	—	+2.5	Vpk	2
Transmission Performance, 2-Wire Impedance (See Test Circuit D)							
2-wire return loss	300 to 3400 Hz	all	26	—	—	dB	4, 10
Longitudinal Balance (2-Wire and 4-Wire, See Test Circuit C); R_L = 600 Ω							
Longitudinal to metallic L-T, L-4	200 Hz to 1 kHz normal polarity 0°C to +70°C normal polarity –40°C to +85°C reverse polarity	–1 –2 –2 –2	52 52 63 58 54	—	—	dB	1, 2 1, 2, 4 1, 2
	1 kHz to 3.4 kHz normal polarity 0°C to +70°C normal polarity –40°C to +85°C reverse polarity	–1 –2 –2 –2	52 52 58 54 54	—	—		1, 2 1, 2, 4 1, 2
Longitudinal signal generation 4-L	300 Hz to 800 Hz Reverse polarity	–1 –2	40 40 42	—	—		
Longitudinal current capability per wire	Active state OHT state	all	—	28 18	—	mArms	4
Insertion Loss (4- to 2-Wire, See Test Circuit B) **BAT = –48 V, R_{LDC} = R_{LAC} = 600 Ω; BAT = –24 V, R_{LDC} = 300 Ω, R_{LAC} = 600 Ω**							
Gain accuracy	0 dBm, 1 kHz 0°C to +70°C	–1 –2	–0.15 –0.15 –0.10	—	+0.15 +0.15 +0.10	dB	
	0 dBm, 1 kHz –40°C to +85°C	–1 –2	–0.20 –0.20 –0.15	—	+0.20 +0.20 +0.15		4
Variation with frequency	300 Hz to 3400 Hz Relative to 1 kHz 0°C to +70°C	–1 –2	–0.15 –0.15 –0.10	—	+0.15 +0.15 +0.10		
	300 Hz to 3400 Hz Relative to 1 kHz –40°C to +85°C	–1 –2	–0.20 –0.20 –0.15	—	+0.20 +0.20 +0.15		4

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Grade	Min	Typ	Max	Unit	Note
Gain tracking	0°C to +70°C +7 dBm to –55 dBm Reference: –0 dBm	all	–0.10	—	+0.10	dB	
	–40°C to +85°C +7 dBm to –55 dBm Reference: –0 dBm	all	–0.15	—	+0.15		4
Insertion Loss and Balance Return Signal (2- to 4-Wire and 4- to 4-Wire, See Test Circuits A and B) **BAT = –48 V, R_{LDC} = R_{LAC} = 600 Ω; BAT = –24 V, R_{LDC} = 300 Ω, R_{LAC} = 600 Ω**							
Gain accuracy	0 dBm, 1 kHz 0°C to +70°C	–1 –2	–6.17 –6.17 –6.12	–6.02	–5.87 –5.87 –5.92	dB	3 3 3
	0 dBm, 1 kHz –40°C to +85°C	–1 –2	–6.22 –6.22 –6.17	–6.02	–5.82 –5.82 –5.87		3, 4 3, 4 3, 4
Variation with frequency	300 Hz to 3400 Hz Relative to 1 kHz 0°C to +70°C	all	–0.10		+0.10		3
	300 Hz to 3400 Hz Relative to 1 kHz –40°C to +85°C	all	–0.15		+0.15		3, 4
Gain tracking	0°C to +70°C +3 dBm to –55 dBm Reference: 0 dBm	all	–0.10		+0.10		3
	–40°C to +85°C +3 dBm to –55 dBm Reference: 0 dBm	all	–0.15		–0.15		3, 4
Group delay	f = 1 kHz	all		5.3		µs	4, 12
Total Harmonic Distortion (2- to 4-Wire and 4- to 2-Wire, See Test Circuits A and B) **BAT = –48 V, R_{LDC} = R_{LAC} = 600 Ω**							
Harmonic distortion	0 dBm	all		–64	–50	dB	
300 Hz to 3400 Hz	+7 dBm	all		–55	–40		6
Idle Channel Noise **BAT = –48 V, R_{LDC} = R_{LAC} = 600 Ω; BAT = –24 V, R_{LDC} = 300 Ω, R_{LAC} = 600 Ω**							
C-message weighted noise	2-wire, 0°C to +70°C 2-wire, –40°C to +85°C	all		+7	+10 +12	dBmc	4 4
Psophometric weighted noise	2-wire, 0°C to +70°C 2-wire, –40°C to +85°C	all		–83	–80 –78	dBmp	— 4
Single Frequency Out-of-Band Noise (See Test Circuit E)							
Metallic	4 kHz to 9 kHz 9 kHz to 1 MHz 256 kHz and harmonics**	all		–76 –76 –63		dBm	4 4, 5, 8 4, 5
Longitudinal	1 kHz to 15 kHz Above 15 kHz 256 kHz and harmonics**	all		–70 –85 –57			4 4, 5, 8 4, 5

Note:
***Applies only when switching regulator is used.*

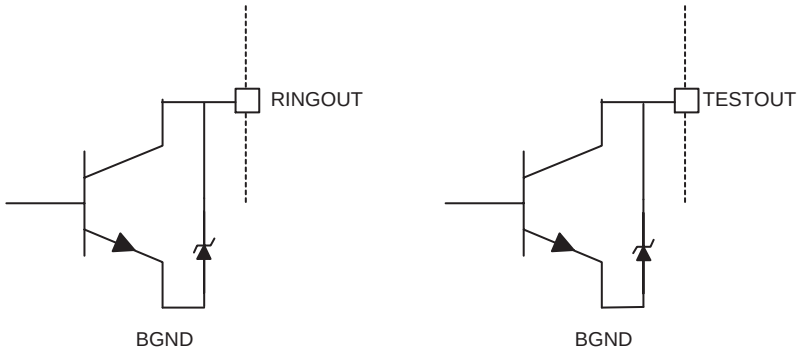
ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Grade	Min	Typ	Max	Unit	Note
Line Characteristics (See Figures 1a, 1b, 1c)							
Short loops, Active state	V_{BAT} = –24 V, R_{LDC} = 300 Ω V_{BAT} = –43 V, R_{LDC} = 600 Ω V_{BAT} = –48 V, R_{LDC} = 600 Ω	all	31.8	34.4	37.0	mA	4, 9 4 —
Long loops, Active state	V_{BAT} = –24 V, R_{LDC} = 640 Ω V_{BAT} = –43 V, R_{LDC} = 1300 Ω V_{BAT} = –48 V, R_{LDC} = 1900 Ω	all	20.0 23.0 18.0				4, 9 4 —
OHT state	V_{BAT} = –24 V, R_{LDC} = 300 Ω V_{BAT} = –48 V, R_{LDC} = 600 Ω	all	31.4	34.4	37.4		4, 9 —
Loop current	Tip Open state, R_L = 0 Ω Disconnect state, R_L = 0 Ω	all			1.0		
I_LLIM (I_{Tip} and I_{Ring})	Tip and ring shorted to GND	all		70	120		
Power Dissipation Battery, Normal Loop Polarity							
On-hook Open Circuit state	V_{BAT} = –24 V, w/o switching reg. V_{BAT} = –48 V, with switching reg.	all		30 35	75 100	mW	9 —
On-hook OHT state	V_{BAT} = –24 V, w/o switching reg. V_{BAT} = –48 V, with switching reg.	all		80 130	225		9 —
On-hook Active state	V_{BAT} = –24 V, w/o switching reg. V_{BAT} = –48 V, with switching reg.	all		80 130	225 300		9 —
Off-hook OHT state R_L = 50 Ω	V_{BAT} = –24 V, w/o switching reg. V_{BAT} = –48 V, with switching reg.	all		500 400	950 750		9 —
Off-hook Active state R_L = 50 Ω	V_{BAT} = –24 V, w/o switching reg. V_{BAT} = –48 V, with switching reg.	all		800 450	1100 1000		9 —
Supply Currents, Battery = –24 V or –48 V							
V_{CC} on-hook supply current	Open Circuit state OHT state Active state	all		2.5 4.5 4.5	4.5 10.0 12.0	mA	9
V_{BREF} on-hook supply current	Open Circuit state OHT state Active state	all		0 0 0			
V_{BAT} on-hook supply current	Open Circuit state OHT state Active state	all		0.6 2.3 2.3	1.0 5.0 6.0		
Power Supply Rejection Ratio (V_{RIPPLE} = 50 mVrms)							
V_{CC}	50 Hz to 3.4 kHz 3.4 kHz to 50 kHz	all	25 22	45 35		dB	6
V_{BAT}	50 Hz to 3.4 kHz 3.4 kHz to 50 kHz	all	27 20	45 40			
Effective int. resistance	CAS to GND	all	85	170	255	kΩ	4
Off-Hook Detector							
Current threshold	I_{DET} = 365/R_D If R_D to gnd I_{DET} = 1825/R_D If R_D to –5V	all	–20		+20	%	

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Grade	Min	Typ	Max	Unit	Note
Ground-Key Detector Thresholds, Active State							
Ground-key resistance threshold	V_{BAT} = –24 V, B(RING) to GND V_{BAT} = –48 V, B(RING) to GND	all	1.0 2.0	2.2 5.0	4.5 10.0	kΩ	9 —
Ground-key current threshold	B(RING) to GND Midpoint to GND	all		9 9		mA	7
Effective internal resistance	GKFIL to AGND/DGND	all	18	36	54	kΩ	4
Ring-Trip Detector Input							
Bias current		all	–5	–0.05		µA	
Offset voltage	Source resistance = 0 to 2 MΩ	all	–50	0	+50	mV	11
Logic Inputs (C4–C1, E1, and CHCLK)							
Input High voltage		all	2.0			V	
Input Low voltage		all			0.8		
Input High current	All inputs except E1	all	–75		40	µA	
Input High current	Input E1	all	–75		45		
Input Low current		all	–0.4			mA	
Logic Output ($\overline{\text{DET}}$)							
Output Low voltage	I_{OUT} = 0.3 mA	all			0.4	V	
Output High voltage	I_{OUT} = –0.1 mA	all	2.4				
Relay Driver Outputs (RINGOUT, TESTOUT)							
On voltage	25 mA sink	all		0.3	+1.5	V	
Off leakage	V_{OH} = 5 V	all			100	µA	
Zener break-over	I_L = 100 µA	all	6	7.2		V	
Zener on voltage	I_L = 30 mA	all		8			

RELAY DRIVER SCHEMATICS

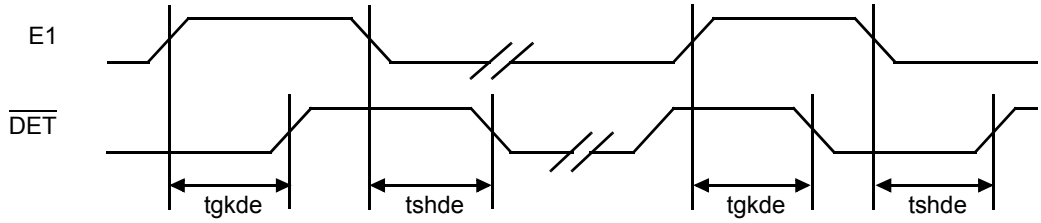


SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Temperature Range	Min	Typ	Max	Unit	Note
tgkde	E1 Low to $\overline{\text{DET}}$ High (E0 = 1)	Ground-Key Detect state R_L open, R_G connected (See Figure H)	0°C to +70°C –40°C to +85°C			3.8 4.0	µs	4
	E1 Low to $\overline{\text{DET}}$ Low (E0 = 1)		0°C to +70°C –40°C to +85°C			1.1 1.6		
tshde	E1 High to $\overline{\text{DET}}$ Low (E0 = 1)	Switchhook Detect state R_L = 600 Ω, R_G open (See Figure G)	0°C to +70°C –40°C to +85°C			1.2 1.7		
	E1 High to $\overline{\text{DET}}$ High (E0 = 1)		0°C to +70°C –40°C to +85°C			3.8 4.0		

SWITCHING WAVEFORMS

E1 to $\overline{\text{DET}}$



Note:
All delays measured at 1.4 V levels.

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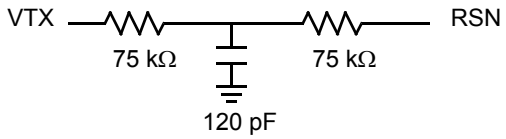
Notes:

1. *Unless otherwise noted, test conditions are BAT = –48 V, V_{CC} = +5 V, R_L = 600 Ω, C_{HP} = 0.33 μF, R_{DC1} = R_{DC2} = 9.09 kΩ, C_{DC} = 0.39 μF, R_D = 35.4 kΩ when R_D is connected to ground and R_D = 177 kΩ when Rd is connected to -5V. C_{CAS} = 0.47 μF, no fuse resistors, R_T =150 kΩ, and R_{RX} = 150 kΩ. Switching regulator components: L = 1 mH, C_{FIL} = 0.47 μF (see Application Circuit).*
2. *Overload level is defined when THD = 1%.*
3. *Balance return signal is the signal generated at V_{TX} by V_{RX}. This specification assumes the two-wire AC load impedance matches the programmed impedance.*
4. *Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
5. *For frequencies below 12 kHz, these tests are performed with a longitudinal impedance of 90 Ω and metallic impedance of 300 Ω. For frequencies greater than 12 kHz, a longitudinal impedance of 90 Ω and a metallic impedance of 135 Ω is used. These tests are extremely sensitive to circuit board layout. Please refer to application notes for details.*
6. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*
7. *"Midpoint" is defined as the connection point between two 300 Ω series resistors connected between A(TIP) and B(RING).*
8. *Fundamental and harmonics from 256 kHz switch regulator chopper are not included.*
9. *For –24 V battery, switching regulator is disabled. L, CHS, and VREG pins connected to VBAT pin; CHCLK pin connected to AGND/DGND.*
10. *Assumes the following Z_T network:*



11. *Tested with 0 Ω source impedance. 2 MΩ is specified for system design purposes only.*
12. *Group delay can be considerably reduced by using a Z_T network such as that shown in Note 10 above. The network reduces the group delay to less than 2 μs. The effect of group delay on linecard performance may be compensated for by using the QSLAC™ or DSLAC™ device.*

Table 1. SLIC Device Decoding

				$\overline{\text{DET}}$ Output	
State	**C3**	**C2**	**C1**	**Two-Wire Status**	**E1 = 0**	**E1 = 1**
0	0	0	0	Open Circuit	Ring trip	Ring trip
1	0	0	1	Ringing	Ring trip	Ring trip
2	0	1	0	Active	Loop detector	Ground key
3	0	1	1	On-Hook TX (OHT)	Loop detector	Ground key
4	1	0	0	Tip Open	Loop detector	—
5	1	0	1	Reserved	Loop detector	—
6	1	1	0	Active Polarity Reversal	Loop detector	Ground key
7	1	1	1	OHT Polarity Reversal	Loop detector	Ground key

Table 2. User-Programmable Components

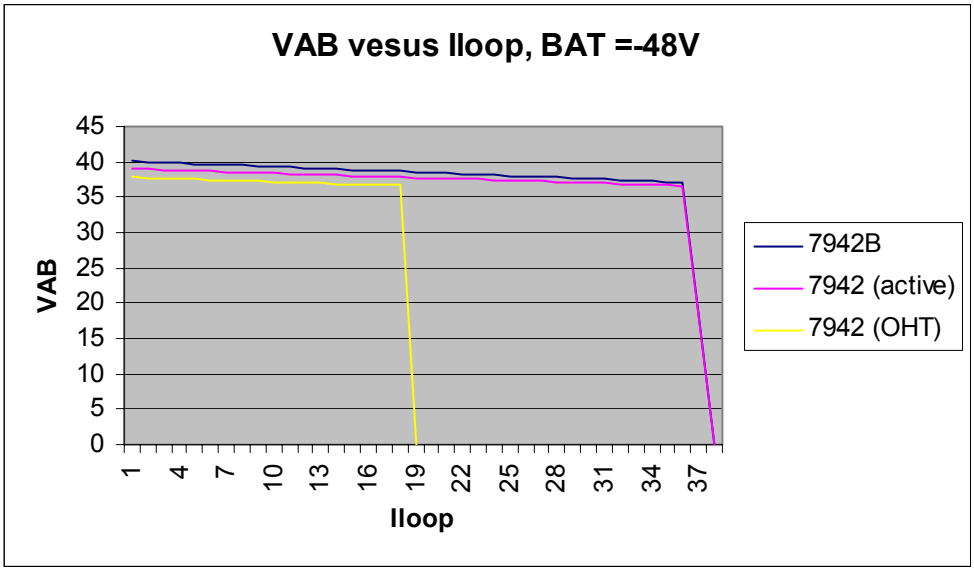
$Z_T = 250(Z_{2WIN} - 2R_F^*)$	Z_T is connected between the VTX and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.

Table 2. User-Programmable Components

$Z_{RX} = \frac{Z_L}{G42_L} \bullet \frac{500Z_T}{Z_T + 250(Z_L + 2R_F)}$	Z_{RX} is connected from V_{RX} to the R_{SN}. Z_T is defined above, and G_{42L} is the desired receive gain.
$R_{DC1} + R_{DC2} = \frac{625}{I_{LOOP}}$ $C_{DC} = 1.5\ ms \bullet \frac{R_{DC1} + R_{DC2}}{R_{DC1}\ R_{DC2}}$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the RDC pin. R_{DC1} and R_{DC2} are approximately equal. I_{LOOP} is the desired loop current in the constant-current region.
$R_D = \frac{365}{I_T}$ If R_D is connected to ground. $R_D = \frac{1825}{I_T}$ If R_D is connected to -5V. $C_D = \frac{0.5\ ms}{R_D}$	R_D and C_D form a network connected from RD to either ground or –5 V, and I_T is the threshold current between on hook and off hook.
$C_{CAS} = \frac{1}{3.4 \bullet 10^5 \pi f_c}$	C_{CAS} is the regulator filter capacitor, and f_c is the desired filter cut-off frequency.

Note:
**R_{FUSE} = 20 – 50 Ω, user selectable.*

DC FEED CHARACTERISTICS



$R_{DC1} + R_{DC2} = R_{DC} = 18.18\ k\Omega$

Active state

OHT state

Notes:

1. *Constant-current region:*

   Active state: $I_L = \frac{625}{R_{DC}}$

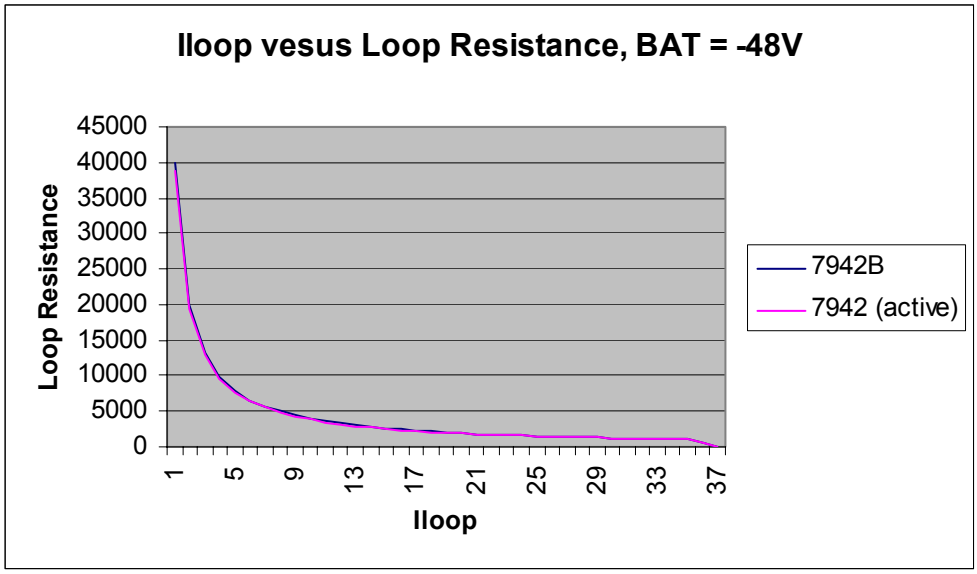
   OHT state: $I_L = \frac{625}{R_{DC}}$

2. *Anti-saturation 2 region:*

   Active state:
   and
   OHT state: $V_{AB} = |BAT| - 7.9 - I_L\left(\frac{R_{DC}}{210}\right)$

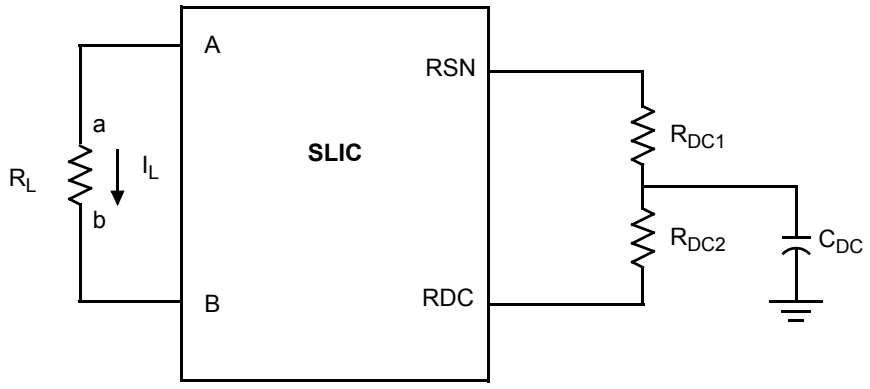
a. V_A–V_B (V_{AB}) Voltage vs. Loop Current (Typical)

DC FEED CHARACTERISTICS (continued)



$R_{DC1} + R_{DC2} = R_{DC} = 18.18\ k\Omega$

b. Loop Current vs. Load Resistance (Typical)



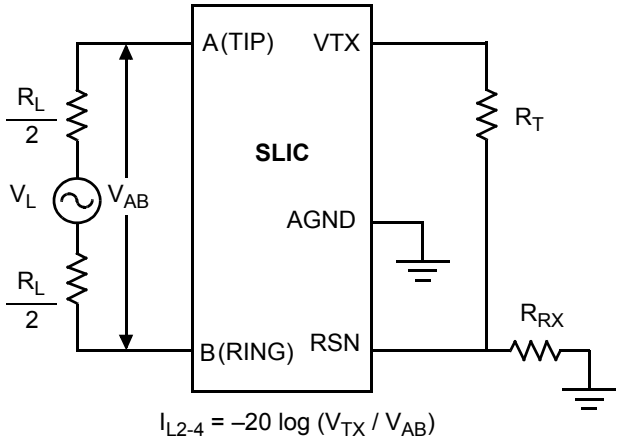
Feed current programmed by R_{DC1} and R_{DC2}

c. Feed Programming

15474A-004

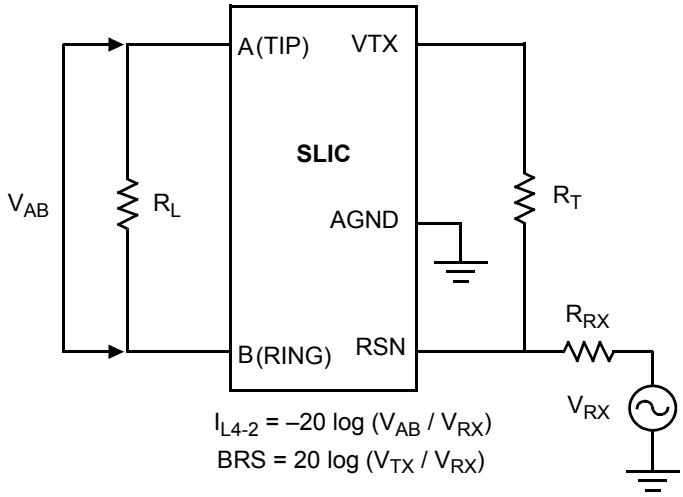
Figure 1. DC Feed Characteristics

TEST CIRCUITS



$I_{L2-4} = -20 \log (V_{TX} / V_{AB})$

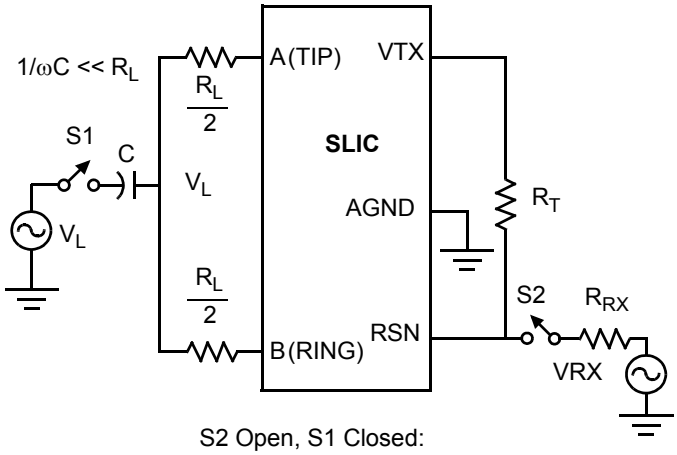
A. Two- to Four-Wire Insertion Loss



$I_{L4-2} = -20 \log (V_{AB} / V_{RX})$

$BRS = 20 \log (V_{TX} / V_{RX})$

B. Four- to Two-Wire Insertion Loss and Balance Return Signal



S2 Open, S1 Closed:

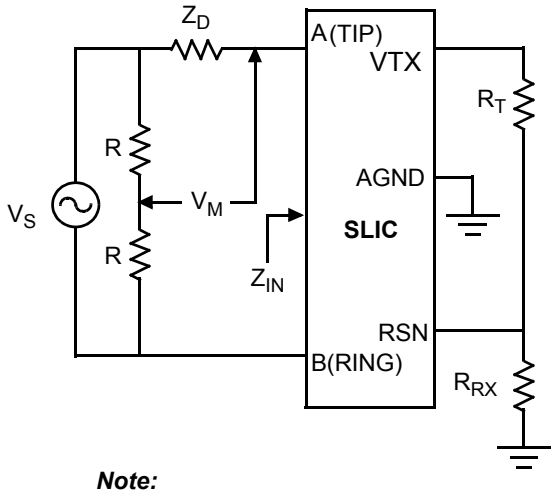
L-T Long. Bal. = 20 log (V_{AB} / V_L)

L-4 Long. Bal. = 20 log (V_{TX} / V_L)

S2 Closed, S1 Open:

4-L Long. Sig. Gen. = 20 log (V_L / V_{RX})

C. Longitudinal Balance



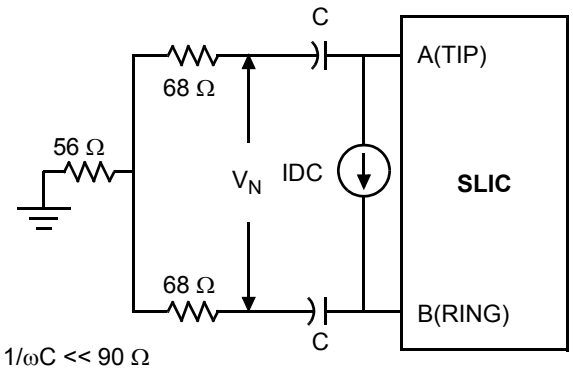
Note:

Z_D is the desired impedance (e.g., the characteristic impedance of the line).

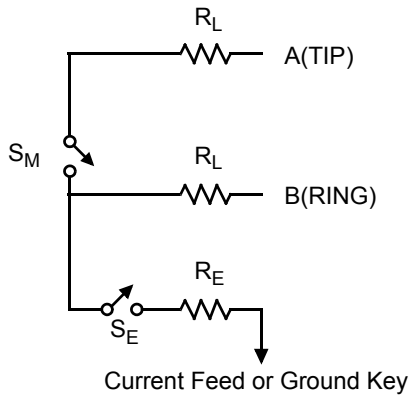
$R_L = -20 \log (2 V_M / V_S)$

D. Two-Wire Return Loss Test Circuit

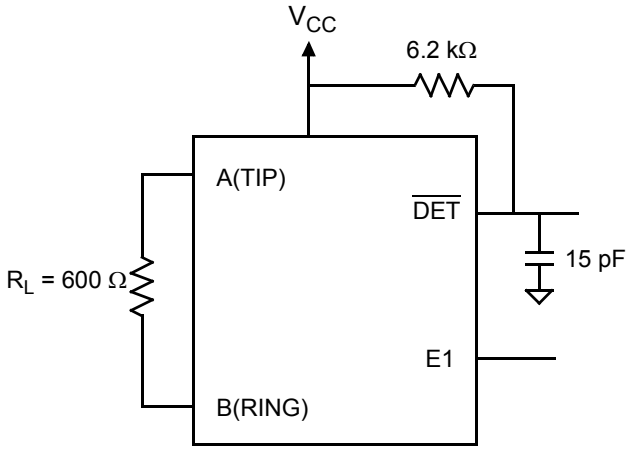
TEST CIRCUITS (continued)



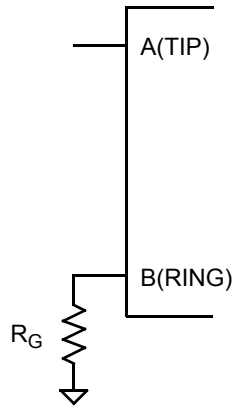
E. Single-Frequency Noise



F. Ground-Key Detection Center Point Test



G. Loop-Detector Switching

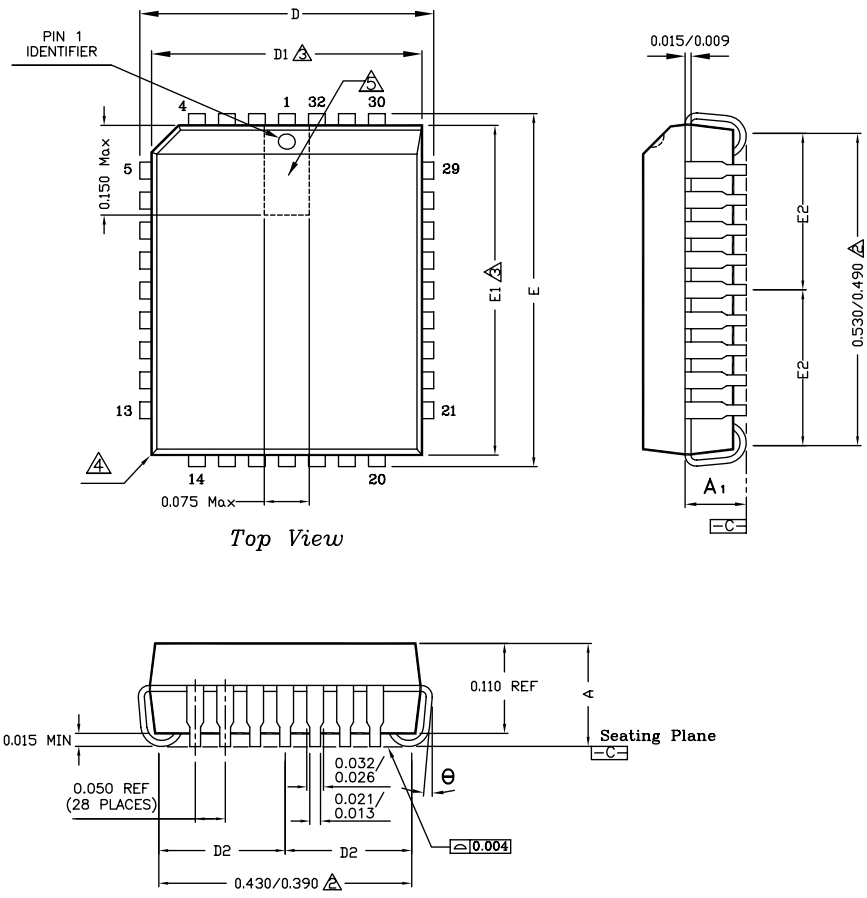


R_G: 2 kΩ at V_{BAT} = –48 V
1 kΩ at V_{BAT} = –24 V

H. Ground-Key Switching

PHYSICAL DIMENSIONS

32-Pin PLCC



32-Pin PLCC			
JEDEC # MS-016			
Symbol	**Min**	**Nom**	**Max**
A	0.125	--	0.140
A1	0.075	0.090	0.095
D	0.485	0.490	0.495
D1	0.447	0.450	0.453
D2		0.205 REF	
E	0.585	0.590	0.595
E1	0.547	0.550	0.553
E2		0.255 REF	
θ	0 deg	--	10 deg

NOTES:

1 Dimensioning and tolerancing conform to ASME Y14,5M-1994.

2 To be measured at seating plan - C - contact point.

3 Dimensions “D1” and “E1” do not include mold protrusion. Allowable mold protrusion is 0.010 inch per side. Dimensions “D” and “E” include mold mismatch and determined at the parting line; that is “D1” and “E1” are measured at the extreme material condition at the upper or lower parting line.

4 Exact shape of this feature is optional.

5 Details of pin 1 identifier are optional but must be located within the zone indicated.

6 Sum of DAM bar protrusions to be 0.007 max per lead.

7 Controlling dimension : Inch.

8 Reference document : JEDEC MS-016

32-Pin PLCC

Note:

Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.

REVISION HISTORY

Revision A1 to B1

- Page 12, modified ZRX equation.

Revision B1 to C1

- Page 8, Line characteristics, OHT State, V_{BAT} = –24 V, R_{LDC} = 600 Ω to R_{LDC} = 300 Ω.
- Page 8, Power Dissipation, Off-hook OHT state R_L = 50 Ω, V_{BAT} = –24 V, w/o switching reg., max 800mW to 950mW.

Revision C1 to D1

- Page 8, Line characteristics, I_LLIM (I_{Tip} and I_{Ring}), changed Max value from 105 to 120.

Revision D1 to E1

- Added green package OPN
- Added *Package Assembly* section

Revision E1 to E2

- Enhanced format of package drawing in *Physical Dimensions* section
- Added new headers/footers due to Zarlink purchase of Legerity on August 3, 2007

For more information about all Zarlink products visit our Web Site at:

www.zarlink.com