

ABRIDGED DATA SHEET

19-5256; Rev 1; 11/10



DS31400

8-Input, 14-Output, Dual DPLL Timing IC with Sub-ps Output Jitter

General Description

The DS31400 is a flexible, high-performance timing IC for diverse frequency conversion and frequency synthesis applications. On each of its eight input clocks and 14 output clocks, the device can accept or generate nearly any frequency between 2kHz and 750MHz. The device offers two independent DPLLs to serve two independent clock-generation paths.

The input clocks are divided down, fractionally scaled as needed, and continuously monitored for activity and frequency accuracy. The best input clock is selected, manually or automatically, as the reference clock for each of the two flexible, high-performance digital PLLs. Each DPLL lock to the selected reference and provides programmable bandwidth, very high-resolution holdover capability and truly hitless switching between input clocks. The digital PLLs are followed by a clock synthesis subsystem that has seven fully programmable digital frequency synthesis blocks, three high-speed low-jitter APLLs, and 14 output clocks, each with its own 32-bit divider and phase adjustment. The APLLs provide fractional scaling and output jitter less than 1ps RMS.

For telecom systems, the device has all required features and functions to serve as a central timing function or as a line card timing IC. With a suitable oscillator the device meets the requirements of Stratum 2, 3E, 3, 4E and 4; G.812 Types I-IV; G.813; and G.8262.

Applications

Frequency Conversion Applications in a Wide Variety of Equipment Types

Telecom Line Cards or Timing Cards with Any Mix of SONET/SDH, Synchronous Ethernet, and/or OTN Ports in WAN Equipment Including MSPPs, Ethernet Switches, Routers, DSLAMs, and Base Stations

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS31400GN	-40°C to +85°C	256 CSBGA
DS31400GN+	-40°C to +85°C	256 CSBGA

+Denotes a lead(Pb)-free/RoHS-compliant package.

SPI is a trademark of Motorola, Inc.

Features

- ◆ **Eight Input Clocks**
 - Differential or CMOS/TTL Format
 - Any Frequency from 2kHz to 750MHz
 - Fractional Scaling for 64B/66B and FEC Scaling (e.g., 64/66, 237/255, 238/255) or Any Other Downscaling Requirement
 - Continuous Input Clock Quality Monitoring
 - Automatic or Manual Clock Selection
 - Three 2/4/8kHz Frame Sync Inputs
- ◆ **Two High-Performance DPLLs**
 - Hitless Reference Switching on Loss of Input
 - Automatic or Manual Phase Build-Out
 - Holdover on Loss of All Inputs
 - Programmable Bandwidth, 0.5MHz to 400Hz
- ◆ **Seven Digital Frequency Synthesizers**
 - Each Can Slave to Either DPLL
 - Produce Any 2kHz Multiple Up to 77.76MHz
 - Per-DFS Clock Phase Adjust
- ◆ **Three Output APLLs**
 - Output Frequencies to 750MHz
 - High Resolution Fractional Scaling for FEC and 64B/66B (e.g., 255/237, 255/238, 66/64) or Any Other Scaling Requirement
 - Less than 1ps RMS Output Jitter
 - Simultaneously Produce Three Low-Jitter Rates from the Same Reference (e.g., 622.08MHz for SONET, 255/237 x 622.08MHz for OTU2, and 156.25MHz for 10GE)
- ◆ **14 Output Clocks in Seven Groups**
 - Nearly Any Frequency from < 1Hz to 750MHz
 - Each Group Slaves to a DFS Clock, Any APLL Clock, or Any Input Clock (Divided and Scaled)
 - Each Has a Differential Output (Three CML, Four LVDS/LVPECL) and Separate CMOS/TTL Output
 - 32-Bit Frequency Divider per Output
 - Two Sync Pulse Outputs: 8kHz and 2kHz
- ◆ **General Features**
 - Suitable Line Card IC or Timing Card IC for Stratum 2/3E/3/4E/4, SMC, SEC/EEC, or SSU
 - Accepts and Produces Nearly Any Frequency Up to 750MHz, Including 1Hz, 2kHz, 8kHz, NxDS1, NxES1, DS2/J2, DS3, E3, 2.5MHz, 25MHz, 125MHz, 156.25MHz, and Nx19.44MHz Up to 622.08MHz
 - Internal Compensation for Local Oscillator Frequency Error
 - SPI™ Processor Interface
 - 1.8V Operation with 3.3V I/O (5V Tolerant)
 - 17mm x 17mm CSBGA Package



Maxim Integrated Products 1

Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, go to: www.maxim-ic.com/errata. For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

DS31400

The diagram illustrates the timing and data flow in a system with multiple line cards. It shows a Backplane connected to multiple Timing Cards (1 of 2, 2 of 2) and Line Cards (1 of N, N of N). The Timing Card (1 of 2) contains a DS31400 chip, a TCXO or OCXO, and a processor. It receives data from the Backplane and sends data to the Backplane. The Line Card (1 of N) contains a Line Card Timing IC and receives data from the Backplane. The diagram also shows a BITS/SSU interface and a clock/data recovery, equalizer, framer, and extract SSMs block.

Backplane: The Backplane is the central communication bus. It has multiple data lines (represented by vertical lines) and control lines. Data lines are labeled with $\leq 0 \rangle$ and $\langle 1 \rangle$ for the Timing Card and $\langle N \rangle$ for the Line Cards. Control lines are labeled with N .

Timing Card (1 of 2): This card is responsible for timing and data recovery. It contains a DS31400 chip, a TCXO or OCXO, and a processor. The DS31400 chip has a Monitor, Divider, Selector block, two DPLL blocks (DPLL1, DPLL2), and two APLL blocks (APLL and divider, APLL, divider and fanout). The TCXO or OCXO provides a reference clock to the Monitor, Divider, Selector block. The processor is connected to the APLL, divider and fanout block. The Timing Card (1 of 2) is connected to the Backplane via data lines $\leq 0 \rangle$ and $\langle 1 \rangle$ and control lines N . It also has a BITS/SSU interface and a clock/data recovery, equalizer, framer, and extract SSMs block.

Timing Card (2 of 2): This card is identical to Timing Card (1 of 2).

Line Card (1 of N): This card contains a Line Card Timing IC (see Fig 2-2). It is connected to the Backplane via data lines $\langle 1 \rangle$ and $\leq 1 \rangle$ and control lines N . It also has a from port SERDES and to port SERDES interface.

Line Card (N of N): This card is identical to Line Card (1 of N).

Annotations:

- activity and frequency monitoring, select highest priority valid input for each DPLL
- create derived DS1 or E1/2048kHz clock locked to selected clock
- clock/data recovery, equalizer, framer, extract SSMs
- from BITS/SSU
- to BITS/SSU
- Stratum 2, 3E or 3: jitter/wander filtering, hitless switching, phase adjust, holdover
- typically 19.44MHz, 25MHz or 8kHz, point-to-point or multidrop buses
- selects best system clock, best recovered line clock, hitless switching, frequency conversion, jitter cleanup

The diagram illustrates the DS31400's internal structure and its interfaces. The central component is the **DS31400**, which contains two main processing blocks: the **DPLL1 Path** and the **DPLL2 Path**.

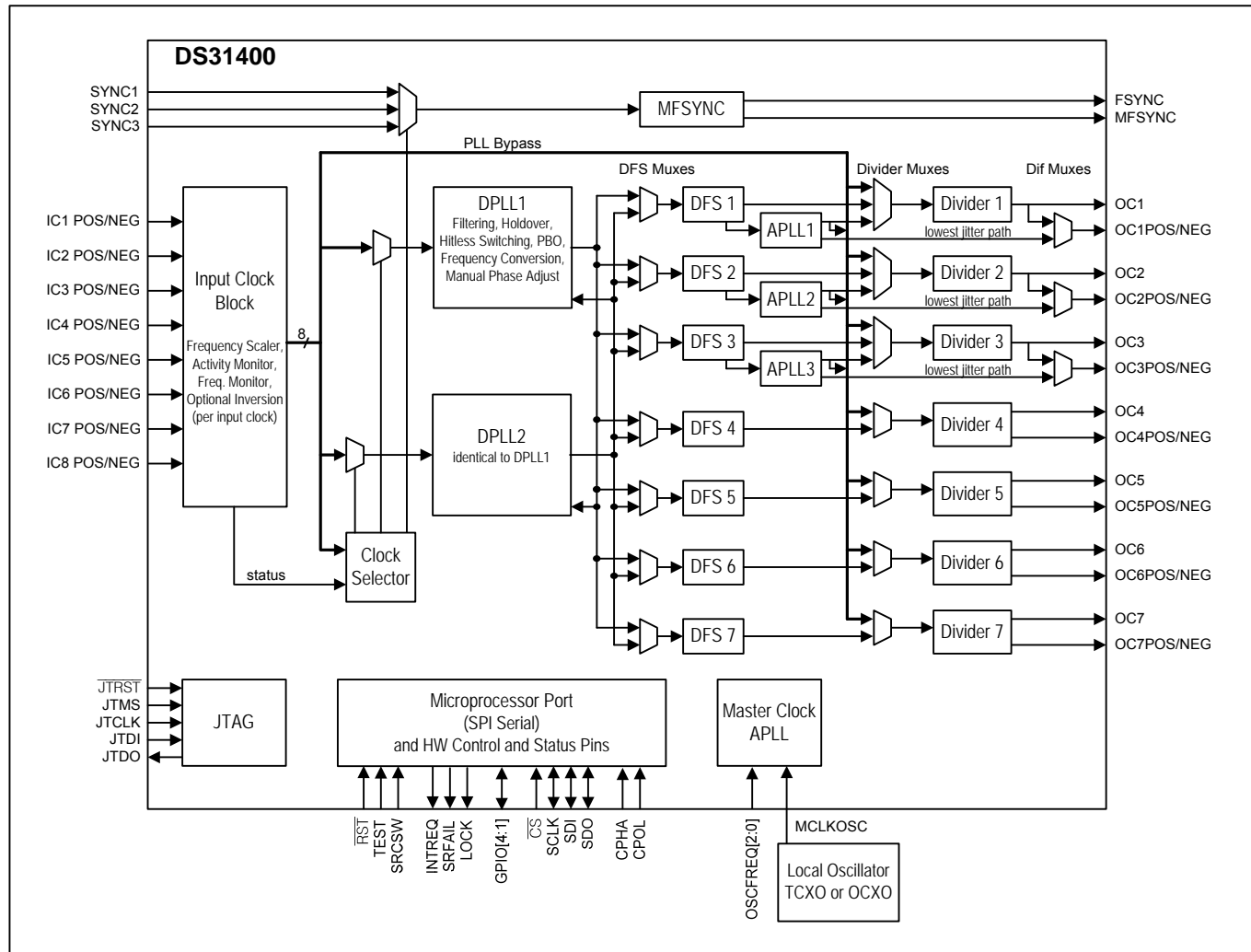
- System Timing Interface (Left):** Two input lines, **IC1** and **IC2**, enter the DPLL1 Path from a "system timing from master and slave timing cards". Two output lines, **OC6** and **OC7**, exit the DPLL2 Path to "line timing to master and slave timing cards".
- Line Card SERDES Interface (Right):** A multi-bit bus labeled **OC1 to OC5** (with a slash and 'n') connects the DPLL1 Path to "clocks to line card SERDES". Another multi-bit bus labeled **IC3 to IC8** (with a slash and 'n') connects the DPLL2 Path from the "recovered line clocks from SERDES".
- Frequency Ranges:**
 - Inputs IC1 and IC2 are associated with frequencies: 19.44MHz, 38.88MHz, 25MHz, etc.
 - Outputs OC6 and OC7 are associated with frequencies: 8kHz, 19.44MHz, 38.88MHz, 25MHz, etc.
 - The SERDES interface (OC1-OC5 and IC3-IC8) handles frequencies: 155.52M, 622.08M, 25M, 125M, 156.25M, etc., with or without fractional scaling for FEC, 64B/66B, etc. It notes that "MANY other rates possible, including DS1, E1, DS3, E3, 10M and Nx19.44M."
- Functional Capabilities:**
 - At the top, a dotted line points to the DPLL1 Path with the text: "clock monitoring and selection, hitless switching, holdover, frequency conversion, fractional scaling, jitter attenuation".
 - At the bottom, a dotted line points to the DPLL2 Path with the text: "clock monitoring and selection, undo fractional scaling, frequency conversion".

Additional notes on the right side specify that the SERDES interface can handle "3 unrelated frequencies simultaneously at <1ps rms jitter plus other frequencies at somewhat higher jitter" and that "recovered line clocks from SERDES" can be "unrelated to one another".

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Block Diagram



Detailed Features

Input Clock Features

- Eight input clocks, differential or CMOS/TTL signal format
- Input clocks can be any frequency from 2kHz up to 750MHz
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTU1, OTU2, OTU3
- Per-input fractional scaling (i.e., multiplying by N/D where N is a 16-bit integer and D is a 32-bit integer and $N < D$) to undo 64B/66B and FEC scaling (e.g., 64/66, 238/255, 237/255, 236/255)
- Special mode allows locking to 1Hz input clocks
- All inputs constantly monitored by programmable activity monitors and frequency monitors
- Fast activity monitor can disqualify the selected reference after a few missing clock cycles
- Frequency measurement and frequency monitor thresholds with 0.2ppm resolution
- Three optional 2/4/8kHz frame-sync inputs

DPLL Features

- Very high-resolution DPLL architecture
- Sophisticated state machine automatically transitions between free-run, locked, and holdover states
- Revertive or nonrevertive reference selection algorithm
- Programmable bandwidth from 0.5mHz to 400Hz
- Separately configurable acquisition bandwidth and locked bandwidth
- Programmable damping factor to balance lock time with peaking: 1.2, 2.5, 5, 10, or 20
- Multiple phase detectors: phase/frequency and multicycle
- Phase/frequency locking ($\pm 360^\circ$ capture) or nearest-edge phase locking ($\pm 180^\circ$ capture)
- Multicycle phase detection and locking (up to ± 8191 UI) improves jitter tolerance and lock time
- Phase build-out in response to reference switching for true hitless switching
- Less than 1ns output clock phase transient during phase build-out
- Output phase adjustment up to ± 200 ns in 6ps steps with respect to selected input reference
- High-resolution frequency and phase measurement
- Holdover frequency averaging over 1-second, 5.8-minute, and 93.2-minute intervals
- Fast detection of input clock failure and transition to holdover mode
- Low-jitter frame sync (8kHz) and multiframe sync (2kHz) aligned with output clocks

Digital Frequency Synthesizer Features

- Seven independently programmable DFS blocks
- Each DFS can slave to either of the DPLLs
- Each DFS can synthesize any 2kHz multiple up to 77.76MHz
- Per-DFS phase adjust (1/256UI steps)
- Approximately 40ps RMS output jitter

Output APLL Features

- Simultaneously produce three high-frequency, low-jitter, rates from the same reference clock, e.g. 622.08MHz for SONET, $255/237 \times 622.08$ MHz for OTU2, and 156.25MHz for 10GE
- Standard telecom output frequencies include 622.08MHz, 155.52MHz, and 19.44MHz for SONET/SDH and 156.25MHz, 125MHz, and 25MHz for Synchronous Ethernet
- Very high-resolution fractional scaling (i.e., noninteger multiplication)
- Less than 1ps RMS output jitter

Output Clock Features

- 14 output clock signals in seven groups
- Output clock groups OC1–OC3 have a very high-speed differential output (current-mode logic, $\leq 750\text{MHz}$) and a separate CMOS/TTL output ($\leq 125\text{MHz}$)
- Output clock groups OC4–OC7 have a high-speed differential output (LVDS/LVPECL, $\leq 312.5\text{MHz}$) and a separate CMOS/TTL output ($\leq 125\text{MHz}$)
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTU1, OTU2, OTU3
- Internal clock muxing allows each output group to slave to its associated DFS block, any of the APLLs, or any input clock (after being divided and scaled)
- Outputs sourced directly from APLLs have less than 1ps RMS output jitter
- Outputs sourced directly from DFS blocks have approximately 40ps RMS output jitter
- Optional 32-bit frequency divider per output
- 8kHz frame sync and 2kHz multiframe sync outputs have programmable polarity and pulse width and can be disciplined by a 2kHz or 8kHz frame sync input
- Per-output delay adjustment
- Per-output enable/disable
- All outputs disabled during reset

General Features

- SPI serial microprocessor interface
- Four general-purpose I/O pins
- Register set can be write-protected
- Operates from a 12.8MHz, 25.6MHz, 10.24MHz, 20.48MHz, 10MHz, 20MHz, 19.44MHz, or 38.88MHz local oscillator
- On-chip watchdog circuit for the local oscillator
- Internal compensation for local oscillator frequency error

Note to readers: This document is an abridged version of the full data sheet. To request the full data sheet, go to www.maxim-ic.com/DS31400 and click on **Request Full Data Sheet**.