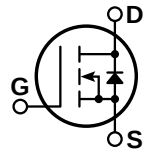


POWER MOS 7® FREDFET

Power MOS 7® is a new generation of low loss, high voltage, N-Channel enhancement mode power MOSFETS. Both conduction and switching losses are addressed with Power MOS 7® by significantly lowering $R_{DS(ON)}$ and Q_g . Power MOS 7® combines lower conduction and switching losses along with exceptionally fast switching speeds inherent with APT's patented metal gate structure.



- Lower Input Capacitance
- Lower Miller Capacitance
- Lower Gate Charge, Q_g
- Increased Power Dissipation
- Easier To Drive
- Popular SOT-227 Package
- **FAST RECOVERY BODY DIODE**



MAXIMUM RATINGS

All Ratings: $T_C = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	APT5510JFLL	UNIT
V_{DSS}	Drain-Source Voltage	550	Volts
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	44	Amps
I_{DM}	Pulsed Drain Current ^①	176	
V_{GS}	Gate-Source Voltage Continuous	± 30	Volts
V_{GSM}	Gate-Source Voltage Transient	± 40	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	463	Watts
	Linear Derating Factor	3.70	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ^① (Repetitive and Non-Repetitive)	44	Amps
E_{AR}	Repetitive Avalanche Energy ^①	35	mJ
E_{AS}	Single Pulse Avalanche Energy ^④	2500	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V, I_D = 250\mu A$)	550			Volts
$I_{D(on)}$	On State Drain Current ^② ($V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max, $V_{GS} = 10V$)	44			Amps
$R_{DS(on)}$	Drain-Source On-State Resistance ^② ($V_{GS} = 10V, 22A$)			0.100	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = 550V, V_{GS} = 0V$)			250	μA
	Zero Gate Voltage Drain Current ($V_{DS} = 440V, V_{GS} = 0V, T_C = 125^\circ\text{C}$)			1000	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V, V_{DS} = 0V$)			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 2.5mA$)	3		5	Volts



CAUTION: These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

APT Website - <http://www.advancedpower.com>

DYNAMIC CHARACTERISTICS

APT5510JFLL

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C_{iss}	Input Capacitance	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1\text{ MHz}$		5823		pF
C_{oss}	Output Capacitance			1124		
C_{rss}	Reverse Transfer Capacitance			81		
Q_g	Total Gate Charge ③	$V_{GS} = 10V$ $V_{DD} = 275V$ $I_D = 49A @ 25^\circ C$		124		nC
Q_{gs}	Gate-Source Charge			34		
Q_{gd}	Gate-Drain ("Miller") Charge			64		
$t_{d(on)}$	Turn-on Delay Time	RESISTIVE SWITCHING $V_{GS} = 15V$ $V_{DD} = 275V$ $I_D = 49A @ 25^\circ C$ $R_G = 0.6\Omega$		16		ns
t_r	Rise Time			12		
$t_{d(off)}$	Turn-off Delay Time			33		
t_f	Fall Time			5		
E_{on}	Turn-on Switching Energy ⑥	INDUCTIVE SWITCHING @ 25°C $V_{DD} = 367V, V_{GS} = 15V$ $I_D = 49A, R_G = 5\Omega$		697		μJ
E_{off}	Turn-off Switching Energy			577		
E_{on}	Turn-on Switching Energy ⑥	INDUCTIVE SWITCHING @ 125°C $V_{DD} = 367V, V_{GS} = 15V$ $I_D = 49A, R_G = 5\Omega$		1025		
E_{off}	Turn-off Switching Energy			664		

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I_S	Continuous Source Current (Body Diode)			44	Amps
I_{SM}	Pulsed Source Current ① (Body Diode)			176	
V_{SD}	Diode Forward Voltage ② ($V_{GS} = 0V, I_S = -44A$)			1.3	Volts
dv/dt	Peak Diode Recovery dv/dt ⑤			15	V/ns
t_{rr}	Reverse Recovery Time ($I_S = -44A, di/dt = 100A/\mu s$)	$T_j = 25^\circ C$		280	ns
		$T_j = 125^\circ C$		600	
Q_{rr}	Reverse Recovery Charge ($I_S = -44A, di/dt = 100A/\mu s$)	$T_j = 25^\circ C$	1.9		μC
		$T_j = 125^\circ C$	5.7		
I_{RRM}	Peak Recovery Current ($I_S = -44A, di/dt = 100A/\mu s$)	$T_j = 25^\circ C$	15		Amps
		$T_j = 125^\circ C$	23		

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.27	$^\circ C/W$
$R_{\theta JA}$	Junction to Ambient			40	

① Repetitive Rating: Pulse width limited by maximum junction temperature

② Pulse Test: Pulse width < 380 μs , Duty Cycle < 2%

③ See MIL-STD-750 Method 3471

④ Starting $T_j = +25^\circ C$, $L = 2.58mH$, $R_G = 25\Omega$, Peak $I_L = 44A$

⑤ dv/dt numbers reflect the limitations of the test circuit rather than the device itself. $I_S \leq -I_D 44A$ $di/dt \leq 700A/\mu s$ $V_R \leq V_{DSS}$ $T_j \leq 150^\circ C$

⑥ Eon includes diode reverse recovery. See figures 18, 20.

APT Reserves the right to change, without notice, the specifications and information contained herein.

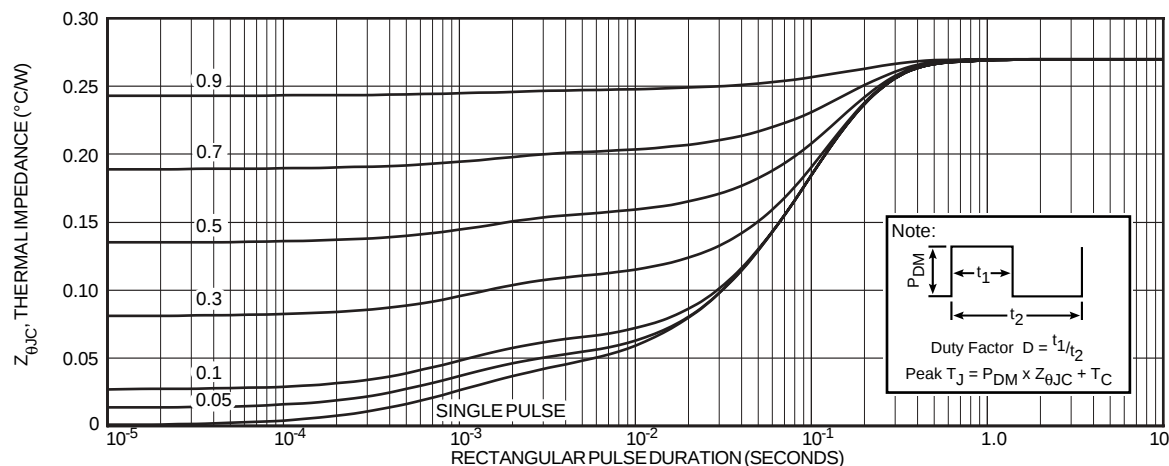


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Typical Performance Curves

APT5510JFLL

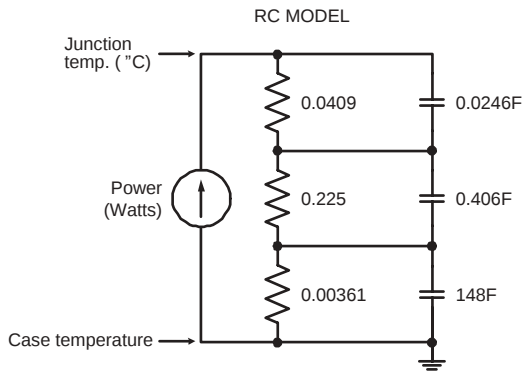


FIGURE 2, TRANSIENT THERMAL IMPEDANCE MODEL

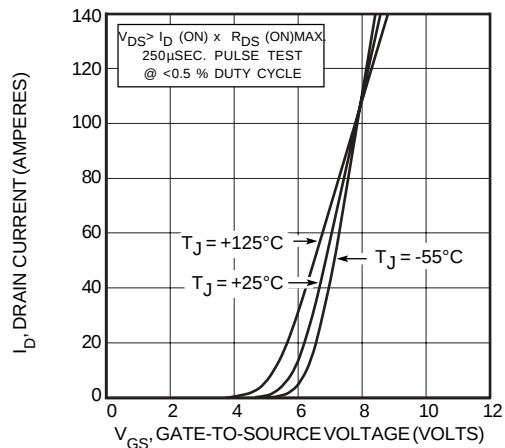


FIGURE 4, TRANSFER CHARACTERISTICS

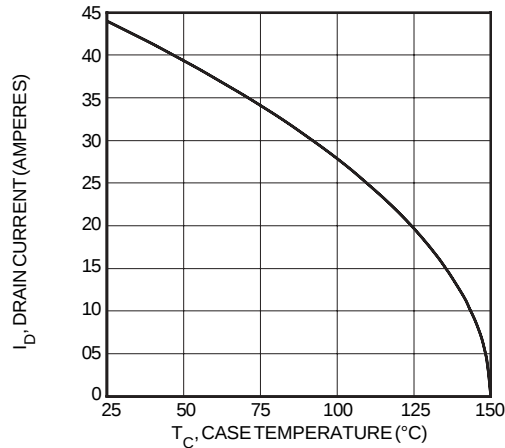


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

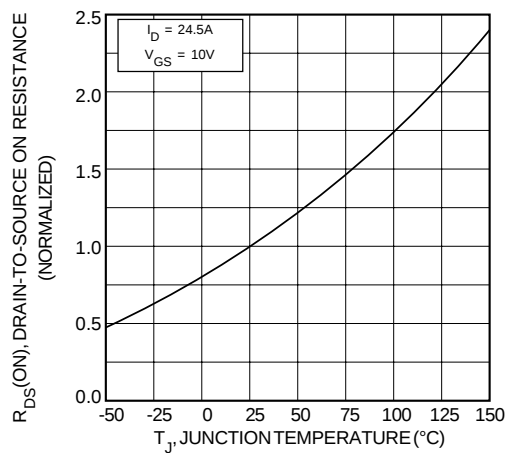


FIGURE 8, ON-RESISTANCE vs. TEMPERATURE

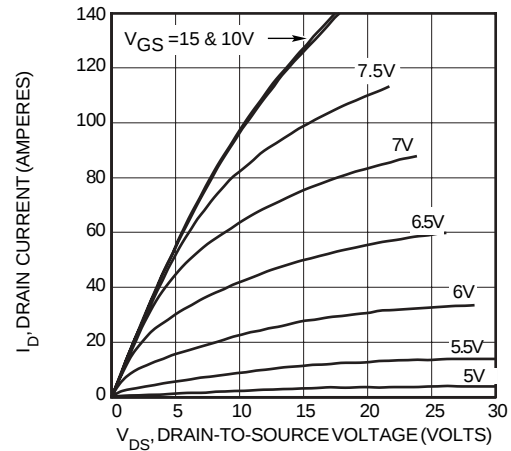


FIGURE 3, LOW VOLTAGE OUTPUT CHARACTERISTICS

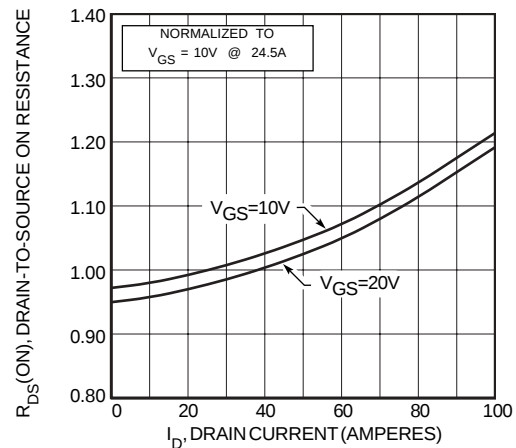


FIGURE 5, $R_{DS}(\text{ON})$ vs DRAIN CURRENT

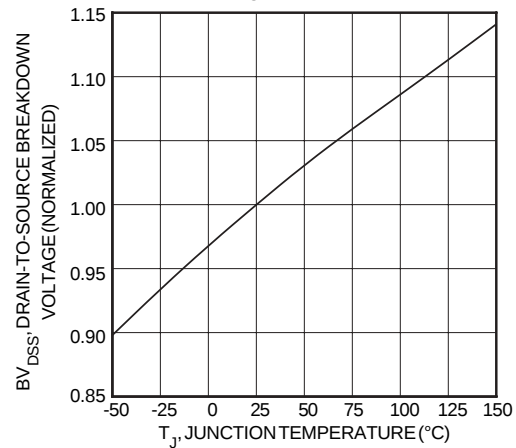


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

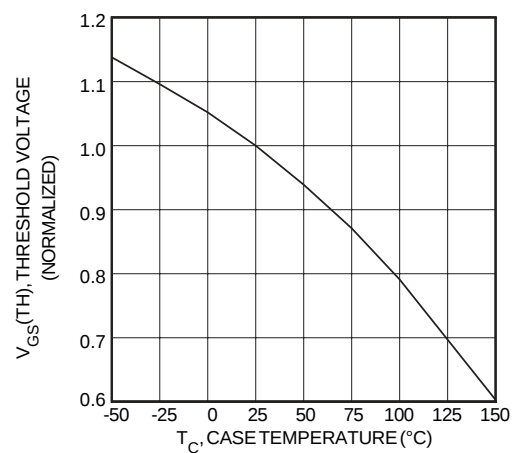


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

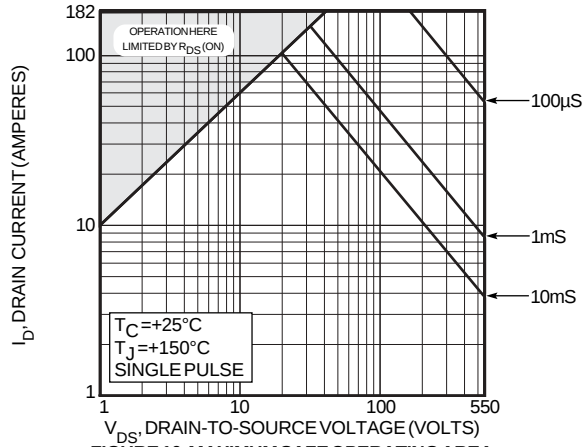


FIGURE 10, MAXIMUM SAFE OPERATING AREA

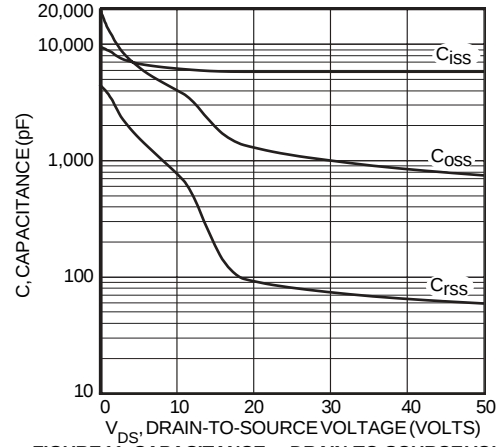


FIGURE 11, CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

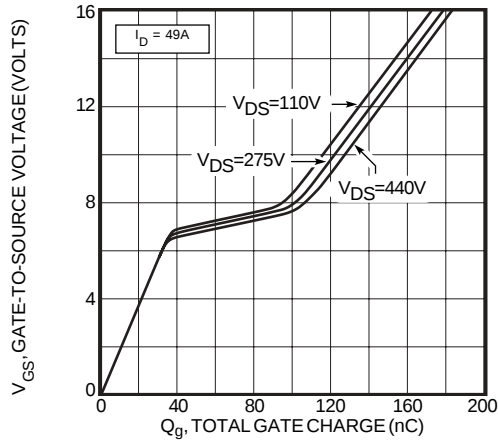


FIGURE 12, GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

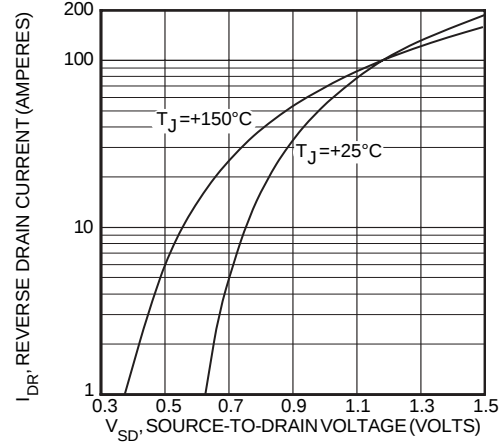


FIGURE 13, SOURCE-DRAIN DIODE FORWARD VOLTAGE

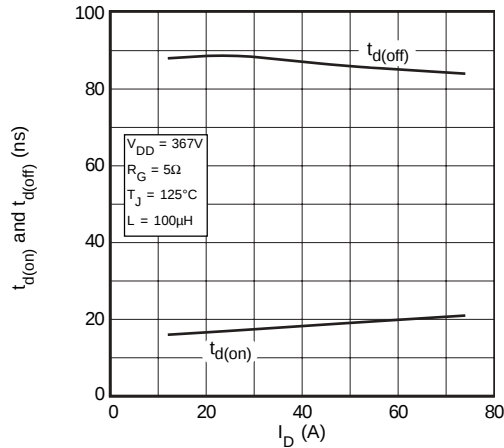


FIGURE 14, DELAY TIMES vs CURRENT

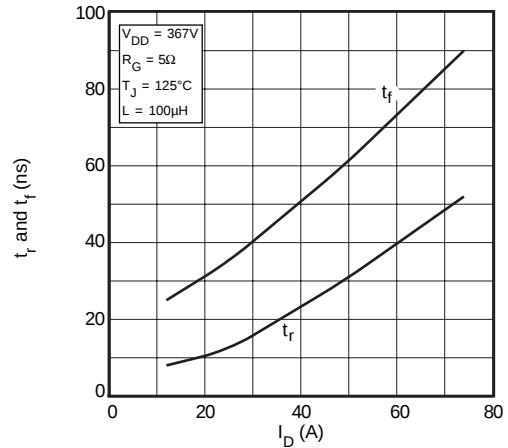


FIGURE 15, RISE AND FALL TIMES vs CURRENT

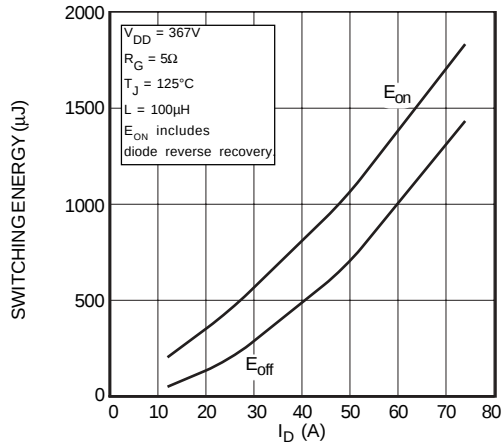


FIGURE 16, SWITCHING ENERGY vs CURRENT

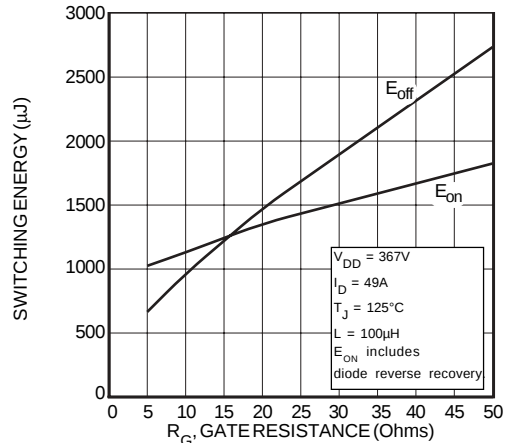


FIGURE 17, SWITCHING ENERGY vs. GATE RESISTANCE

APT5510JFLL

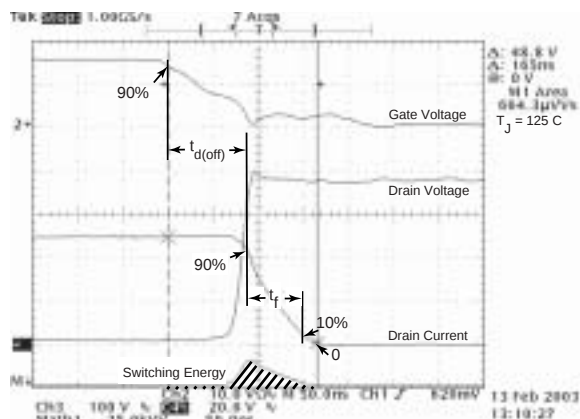
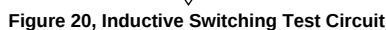


Figure 19. Turn-off Switching Waveforms and Definitions



Top View Dimensions:

- Overall width: 31.5 (.1240) / 31.7 (.1248)
- Pin pitch (center-to-center): 7.8 (.307) / 8.2 (.322)
- Pin diameter: 4.0 (.157) (2 places)
- Pin thickness: 4.2 (.165) (2 places)
- Pin width: 3.3 (.129) / 3.6 (.143)
- Pin spacing (inner): 14.9 (.587) / 15.1 (.594)
- Pin spacing (outer): 30.1 (.1185) / 30.3 (.1193)
- Overall pin width: 38.0 (.1496) / 38.2 (.1504)

Side View Dimensions:

- Overall height: 11.8 (.463) / 12.2 (.480)
- Lead thickness: 8.9 (.350) / 9.6 (.378)
- Lead width: 0.75 (.030) / 0.85 (.033)
- Lead spacing: 12.6 (.496) / 12.8 (.504)
- Overall lead width: 25.2 (.0992) / 25.4 (1.000)
- Lead thickness (bottom): 1.95 (.077) / 2.14 (.084)

Detail View Dimensions:

- W=4.1 (.161)
- W=4.3 (.169)
- H=4.8 (.187)
- H=4.9 (.193) (4 places)

Notes:

- * Source
- Drain
- * Source terminals are shorted internally. Current handling capability is equal for either Source terminal.
- * Source
- Gate

APT's products are covered by one or more of U.S. patents 4,895,810 5,045,903 5,089,434 5,182,234 5,019,522 5,262,336 6,503,786 5,256,583 4,748,103 5,283,202 5,231,474 5,434,095 5,528,058 and foreign patents. US and Foreign patents pending. All Rights Reserved.