

DDR3 SDRAM UDIMM

MT16JTF25664AY – 2GB
MT16JTF51264AY – 4GB

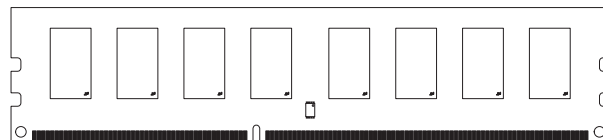
For component data sheets, refer to Micron's Web site: www.micron.com

Features

- DDR3 functionality and operations supported as per component data sheet
- 240-pin, unbuffered dual in-line memory module (UDIMM)
- Fast data transfer rates: PC3-10600, PC3-8500, or PC3-6400
- 2GB (256 Meg x 64), 4GB (512 Meg x 64)
- $V_{DD} = V_{DDQ} = +1.5V \pm 0.75V$
- $V_{DDSPD} = +3.0V$ to $+3.6V$
- Reset pin for improved system stability
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Dual rank
- 8 internal device banks for concurrent operation
- Fixed burst length of 8 (BL8) and burst chop of 4 (BC4) via the mode register
- Adjustable data-output drive strength
- Serial presence-detect (SPD) EEPROM
- Gold edge contacts
- Pb-free
- Addresses are mirrored for second rank
- Fly-by topology
- Terminated command, address, and control bus

Figure 1: 240-Pin UDIMM (MO-269 R/C B)

PCB height: 30mm (1.18in)



Options

- Operating temperature¹
 - Commercial ($0^{\circ}C \leq T_A \leq +70^{\circ}C$)
 - Industrial ($-40^{\circ}C \leq T_A \leq +85^{\circ}C$)
- Frequency/CAS latency
 - 1.5ns @ CL = 9 (DDR3-1333)
 - 1.5ns @ CL = 10 (DDR3-1333)
 - 1.87ns @ CL = 7 (DDR3-1066)
 - 1.87ns @ CL = 8 (DDR3-1066)
 - 2.5ns @ CL = 5 (DDR3-800)
 - 2.5ns @ CL = 6 (DDR3-800)

Marking

None
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-1G4
-1G3
-1G1
-1G0
-80C
-80B

Notes: 1. Contact Micron for industrial temperature module offerings.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)						t_{RCD} (ns)	t_{RP} (ns)	t_{RC} (ns)
		CL = 10	CL = 9	CL = 8	CL = 7	CL = 6	CL = 5			
-1G4	PC3-10600	–	1333	1066	800	–	–	13.5	13.5	49.5
-1G3	PC3-10600	1333	1066	800	–	–	–	15	15	51
-1G1	PC3-8500	–	–	–	1066	800	–	13.125	13.125	50.625
-1G0	PC3-8500	–	–	1066	800	–	–	15	15	52.5
-80C	PC3-6400	–	–	–	–	–	800	12.5	12.5	50
-80B	PC3-6400	–	–	–	–	800	–	15	15	52.5



2GB, 4GB (x64, DR) 240-Pin DDR3 SDRAM UDIMM Features

Table 2: Addressing

Parameter	2GB	4GB
Refresh count	8K	8K
Row address	16K (A0–A13)	32K (A0–A14)
Device bank address	8 (BA0–BA2)	8 (BA0–BA2)
Device page size per bank	1KB	1KB
Device configuration	1Gb (128 Meg x 8)	2Gb (256 Meg x 8)
Column address	1K (A0–A9)	1K (A0–A9)
Module rank address	2 (S0#, S1#)	2 (S0#, S1#)

Table 3: Part Numbers and Timing Parameters 2GB Modules

Base device: MT41J128M8¹, 1Gb DDR3 SDRAM

Part Number ²	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	CL- ^t RCD- ^t RP (Clock Cycles)
MT16JTF25664A(I)Y-1G4__	2GB	256 Meg x 64	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT16JTF25664A(I)Y-1G3__	2GB	256 Meg x 64	10.6 GB/s	1.5ns/1333 MT/s	10-10-10
MT16JTF25664A(I)Y-1G1__	2GB	256 Meg x 64	8.5 GB/s	1.87ns/1066 MT/s	7-7-7
MT16JTF25664A(I)Y-1G0__	2GB	256 Meg x 64	8.5 GB/s	1.87ns/1066 MT/s	8-8-8
MT16JTF25664A(I)Y-80C__	2GB	256 Meg x 64	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT16JTF25664A(I)Y-80B__	2GB	256 Meg x 64	6.4 GB/s	2.5ns/800 MT/s	6-6-6

Table 4: Part Numbers and Timing Parameters 4GB Modules

Base device: MT41J256M8¹, 2Gb DDR3 SDRAM

Part Number ²	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	CL- ^t RCD- ^t RP (Clock Cycles)
MT16JTF51264A(I)Y-1G4__	4GB	512 Meg x 64	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT16JTF51264A(I)Y-1G3__	4GB	512 Meg x 64	10.6 GB/s	1.5ns/1333 MT/s	10-10-10
MT16JTF51264A(I)Y-1G1__	4GB	512 Meg x 64	8.5 GB/s	1.87ns/1066 MT/s	7-7-7
MT16JTF51264A(I)Y-1G0__	4GB	512 Meg x 64	8.5 GB/s	1.87ns/1066 MT/s	8-8-8
MT16JTF51264A(I)Y-80C__	4GB	512 Meg x 64	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT16JTF51264A(I)Y-80B__	4GB	512 Meg x 64	6.4 GB/s	2.5ns/800 MT/s	6-6-6

- Notes:
1. Data sheets for the base device parts can be found on Micron's Web site.
 2. All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT16JTF51264AY-1G1B1.



2GB, 4GB (x64, DR) 240-Pin DDR3 SDRAM UDIMM Pin Assignments and Descriptions

Pin Assignments and Descriptions

Table 5: Pin Assignments

240-Pin UDIMM Front								240-Pin UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREFDQ	31	DQ25	61	A2	91	DQ41	121	Vss	151	Vss	181	A1	211	Vss
2	Vss	32	Vss	62	VDD	92	Vss	122	DQ4	152	DM3	182	VDD	212	DM5
3	DQ0	33	DQS3#	63	CK1	93	DQS5#	123	DQ5	153	NC	183	VDD	213	NC
4	DQ1	34	DQS3	64	CK1#	94	DQS5	124	Vss	154	Vss	184	CK0	214	Vss
5	Vss	35	Vss	65	VDD	95	Vss	125	DM0	155	DQ30	185	CK0#	215	DQ46
6	DQS0#	36	DQ26	66	VDD	96	DQ42	126	NC	156	DQ31	186	VDD	216	DQ47
7	DQS0	37	DQ27	67	VREFCA	97	DQ43	127	Vss	157	Vss	187	NC	217	Vss
8	Vss	38	Vss	68	NC	98	Vss	128	DQ6	158	NC	188	A0	218	DQ52
9	DQ2	39	NC	69	VDD	99	DQ48	129	DQ7	159	NC	189	VDD	219	DQ53
10	DQ3	40	NC	70	A10	100	DQ49	130	Vss	160	Vss	190	BA1	220	Vss
11	Vss	41	Vss	71	BA0	101	Vss	131	DQ12	161	NC	191	VDD	221	DM6
12	DQ8	42	NC	72	VDD	102	DQS6#	132	DQ13	162	NC	192	RAS#	222	NC
13	DQ9	43	NC	73	WE#	103	DQS6	133	Vss	163	Vss	193	S0#	223	Vss
14	Vss	44	Vss	74	CAS#	104	Vss	134	DM1	164	NC	194	VDD	224	DQ54
15	DQS1#	45	NC	75	VDD	105	DQ50	135	NC	165	NC	195	ODT0	225	DQ55
16	DQS1	46	NC	76	S1#	106	DQ51	136	Vss	166	Vss	196	A13	226	Vss
17	Vss	47	Vss	77	ODT1	107	Vss	137	DQ14	167	NC	197	VDD	227	DQ60
18	DQ10	48	NC	78	VDD	108	DQ56	138	DQ15	168	RESET#	198	NC	228	DQ61
19	DQ11	49	NC	79	NC	109	DQ57	139	Vss	169	CKE1	199	Vss	229	Vss
20	Vss	50	CKE0	80	Vss	110	Vss	140	DQ20	170	VDD	200	DQ36	230	DM7
21	DQ16	51	VDD	81	DQ32	111	DQS7#	141	DQ21	171	NC	201	DQ37	231	NC
22	DQ17	52	BA2	82	DQ33	112	DQS7	142	Vss	172	NC/A14 ¹	202	Vss	232	Vss
23	Vss	53	NC	83	Vss	113	Vss	143	DM2	173	VDD	203	DM4	233	DQ62
24	DQS2#	54	VDD	84	DQS4#	114	DQ58	144	NC	174	A12	204	NC	234	DQ63
25	DQS2	55	A11	85	DQS4	115	DQ59	145	Vss	175	A9	205	Vss	235	Vss
26	Vss	56	A7	86	Vss	116	Vss	146	DQ22	176	VDD	206	DQ38	236	VDDSPD
27	DQ18	57	VDD	87	DQ34	117	SA0	147	DQ23	177	A8	207	DQ39	237	SA1
28	DQ19	58	A5	88	DQ35	118	SCL	148	Vss	178	A6	208	Vss	238	SDA
29	Vss	59	A4	89	Vss	119	SA2	149	DQ28	179	VDD	209	DQ44	239	Vss
30	DQ24	60	VDD	90	DQ40	120	VTT	150	DQ29	180	A3	210	DQ45	240	VTT

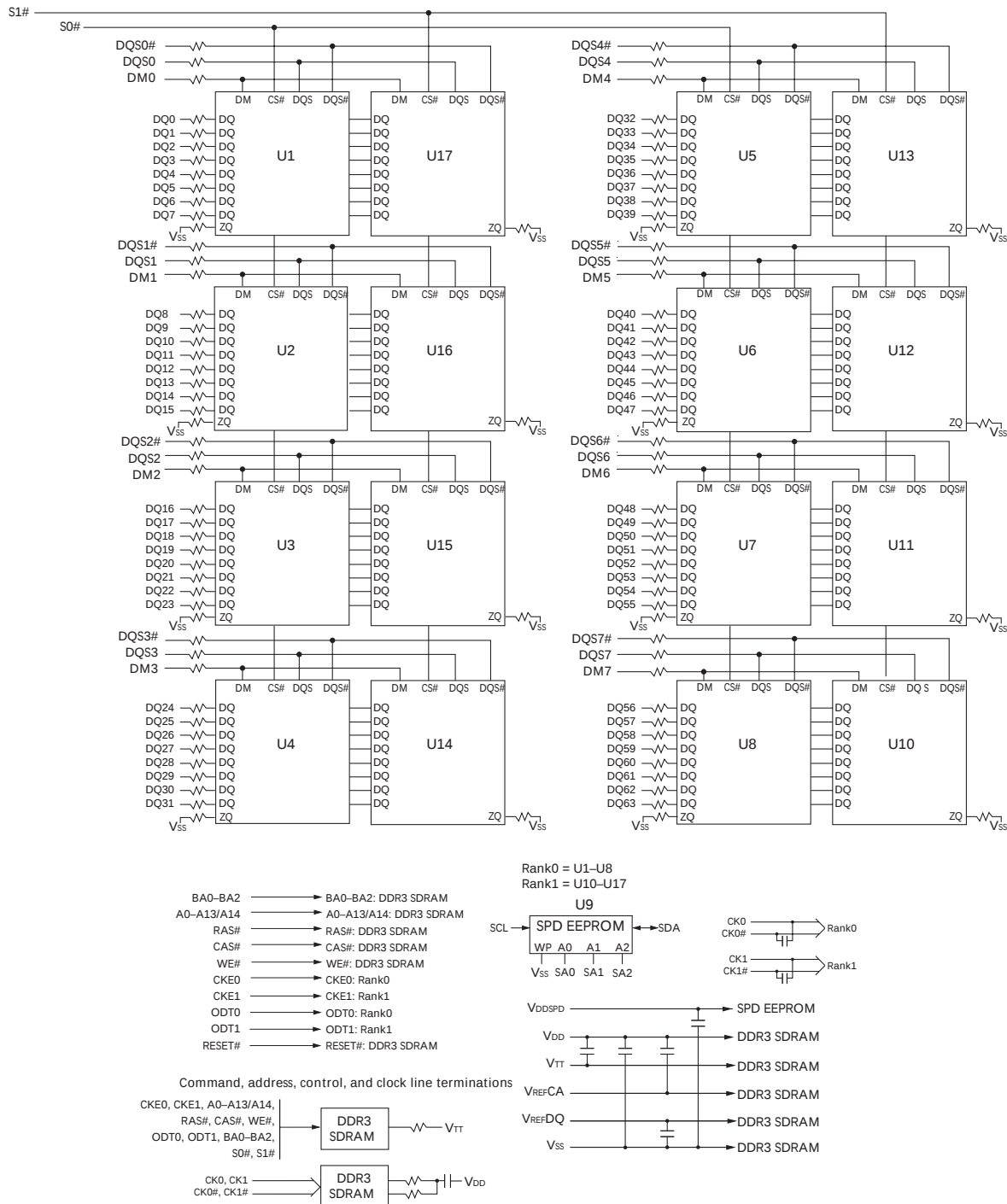
Notes: 1. Pin 172 is NC for 2GB and A14 for 4GB.

Table 6: Pin Description

Symbol	Type	Description
A0–A14	Input	Address inputs: Provide the row address for ACTIVE commands and the column address and auto precharge bit for READ/WRITE commands to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. The address inputs also provide the op-code during mode register command set. A0–A13 (2GB) A0–A14 (4GB).
BA0–BA2	Input	Bank address inputs: BA0, BA1 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0, BA1 define which mode register, including MR, EMR, EMR(2), and EMR(3), is loaded during the LOAD MODE command.
CK0, CK0#, CK1, CK1#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS/ DQS#) is referenced to the crossings of CK and CK#.
CKE0, CKE1	Input	Clock enable: CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR3 SDRAM.
DM0–DM7	Input	Data input mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS7 pins.
ODT0 ODT1	Input	On-die termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to the following pins: DQ, DQS, DQS# and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input	Reset: An active LOW CMOS input referenced to Vss and not referenced to VREFCA or VREFDQ. The reset pin input receiver is a CMOS input and is defined as a rail-to-rail signal with a DC HIGH $\geq 0.8 \times V_{DDQ}$ and DC LOW $\leq 0.2 \times V_{DDQ}$ (1.20V for HIGH and 0.30V for LOW). RESET# assertion and desertion are asynchronous. System applications will most likely be unterminated, heavily loaded, and have very slow slew rates. A slow slew rate receiver design is recommended along with implementing on-chip noise filtering to prevent false triggering (RESET# assertion minimum pulse width is 100ns).
S0#, S1#	Input	Chip select: S# enables (registered LOW) and disables (registered HIGH) the command decoder. With both inputs HIGH, all outputs of the register(s) are disabled except for CKE and ODT. CKE, ODT, and chip select remain in previous state when both outputs are HIGH.
SA0–SA2	Input	Presence-detect address inputs: These pins are used to configure the SPD EEPROM address range.
SCL	Input	Serial clock for presence-detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
DQ0–DQ63	I/O	Data input/output: Bidirectional data bus.
DQS0–DQS7 DQS0#–DQS7#	I/O	Data strobe: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data.
SDA	I/O	Serial presence-detect data: SDA is a bidirectional pin used to transfer addresses and data into and out of the SPD EEPROM on the module.
VDD	Supply	Power supply: 1.5V $\pm 0.075V$.
VDDSPD	Supply	Serial EEPROM positive power supply: +3.0V to +3.6V.
VREFDQ	Supply	Reference voltage: DQ, DM. $V_{DD}/2$.
VREFCA	Supply	Reference voltage: Command, address, and control. $V_{DD}/2$.
Vss	Supply	Ground.
VTT	Supply	Termination voltage: Used for address, command, control, and clock nets. $V_{DD}/2$.
NC	–	No connect: These pins should be left unconnected.

Functional Block Diagram

Figure 2: Functional Block Diagram



Notes: 1. ZQ ball on each DDR3 component is connected to an external 240Ω resistor that is tied to ground. Used for the calibration of the component's on-die termination and output driver.

General Description

The MT16JTF25664AY and MT16JTF51264AY DDR3 SDRAM modules are high-speed, CMOS, dynamic random-access 2GB and 4GB memory modules organized in a x64 configuration. These DDR3 SDRAM modules use internally configured 8-bank (1Gb and 2Gb) DDR3 SDRAM devices.

DDR3 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially an $8n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM module effectively consists of a single $8n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding n -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR3 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR3 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Fly-By Topology

DDR3 modules utilize faster clock speeds than earlier DDR technologies, making signal quality more important than ever. To ensure the best possible signal quality the clock and command/address busses have been routed in a fly-by topology, where each clock and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by utilizing the write leveling feature of DDR3.

Serial Presence-Detect Operation

DDR3 SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes are programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I²C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to VSS on the module, permanently disabling hardware write protect.

Electrical Specifications

Stresses greater than those listed in Table 7, may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in the device data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 7: Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Units
VDD ¹	VDD supply voltage relative to Vss		−0.4	+1.975	V
VIN, VOUT	Voltage on any pin relative to Vss		−0.4	+1.975	V
II	Input leakage current; Any input 0V ≤ VIN ≤ VDD; VREF input 0V ≤ VIN ≤ 0.95V (All other pins not under test = 0V)	Address inputs RAS#, CAS#, WE#, S#, CKE, ODT, BA	−16	+16	μA
		CK, CK#	−8	+8	
		DM	−2	+2	
IOZ	Output leakage current; 0V ≤ VOUT ≤ VDDQ; DQs and ODT are disabled	DQ, DQS, DQS#	−2	+2	μA
IVREF	VREF leakage current; VREF = valid VREF level		−32	+32	μA

Notes: 1. VREF must not be greater than $0.6 \times V_{DD}$. When VDD is less than 500mV, VREF may be equal to or less than 300mV.

Table 8: Operating Conditions

Symbol	Parameter		Min	Max	Units
I _{VTT}	Termination reference current from V _{TT}		−600	+600	mA
V _{TT} ¹	Termination reference voltage – command address bus		−0.483 x V _{DD}	+0.517 x V _{DD}	V
T _A ^{2,4}	Module ambient operating temperature	Commercial	0	+70	°C
		Industrial	−40	+85	°C
T _C ^{2,4}	DDR3 SDRAM component case operating temperature ³	Commercial	0	+85	°C
		Industrial	−40	+95	°C

Notes: 1. VTT termination voltage in excess of stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.
2. TA and TC are simultaneous requirements.
3. Refresh rate is required to double when $85^{\circ}C < T_C \leq 95^{\circ}C$.
4. For further information, refer to technical note [TN-00-08: Thermal Applications](#), available on Micron's Web site.

Input Capacitance

Micron encourages designers to simulate the performance of the module to achieve optimum values. Simulations are significantly more accurate and realistic than a gross estimation of module capacitance when inductance and delay parameters associated with trace lengths are used in simulations.

Component AC Timing and Operating Conditions

Recommended AC operating conditions are given in the DDR3 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown in Table 9.



2GB, 4GB (x64, DR) 240-Pin DDR3 SDRAM UDIMM Electrical Specifications

Table 9: Module and Component Speed Grades

DDR3 components must be able to meet or exceed the listed speed grade.

Module Speed Grade	Component Speed Grade
-1G4	-15E
-1G3	-15
-1G1	-187E
-1G0	-187
-80C	-25E
-80B	-25



2GB, 4GB (x64, DR) 240-Pin DDR3 SDRAM UDIMM Electrical Specifications

IDD Specifications

Table 10: DDR3 IDD Specifications and Conditions – 2GB

Values shown for each data rate are for the MT41J128M8 DDR3 SDRAM only and are computed from values specified in the 1Gb (128 Meg x 8) component data sheet

Parameter	Symbol	1333	1067	800	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	IDD0	1,080	1,000	840	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	IDD1	1,280	1,120	960	mA
Precharge power down current: Slow exit	IDD2P	400	400	400	mA
Precharge power down current: Fast exit	IDD2P	160	160	160	mA
Precharge quiet standby current	IDD2Q	1,120	960	800	mA
Precharge standby current	IDD2N	1,200	1,040	880	mA
Active power-down current	IDD3P	880	720	640	mA
Active standby current	IDD3N	1,440	1,200	960	mA
Burst read operating current	IDD4R	2,080	1,840	1,600	mA
Burst write operating current	IDD4W	2,280	2,000	1,720	mA
Refresh current	IDD5B	4,640	4,080	3,440	mA
Self-refresh temperature current: MAX $T_C = 85^\circ\text{C}$	IDD6	96	96	96	mA
Self-refresh temperature current (SRT-enabled): MAX $T_C = 95^\circ\text{C}$	IDD6ET	144	144	144	mA
All bank interleaved read current	IDD7	4,400	3,840	3,600	mA

Table 11: DDR3 IDD Specifications and Conditions – 4GB

Values shown for each data rate are for the MT41J256M8 DDR3 SDRAM only and are computed from values specified in the 2Gb (256 Meg x 8) component data sheet

Parameter	Symbol	1333	1067	800	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	IDD0	1,020	1,040	880	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	IDD1	1,320	1,060	1,000	mA
Precharge power down current: Slow exit	IDD2P	400	400	400	mA
Precharge power down current: Fast exit	IDD2P	160	160	160	mA
Precharge quiet standby current	IDD2Q	1,120	960	800	mA
Precharge standby current	IDD2N	1,120	960	800	mA
Active power-down current	IDD3P	960	800	720	mA
Active standby current	IDD3N	1,520	1,280	1,040	mA
Burst read operating current	IDD4R	1,880	1,880	1,640	mA
Burst write operating current	IDD4W	2,480	2,200	1,920	mA
Refresh current	IDD5B	5,120	4,560	3,920	mA
Self-refresh temperature current: MAX $T_C = 85^\circ\text{C}$	IDD6	128	128	128	mA
Self-refresh temperature current (SRT-enabled): MAX $T_C = 95^\circ\text{C}$	IDD6ET	192	192	192	mA
All bank interleaved read current	IDD7	3,760	3,520	3,280	mA

Serial Presence-Detect

Table 12: Serial Presence-Detect EEPROM DC Operating Conditions

All voltages referenced to V_{SS}

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V _{DDSPD}	3.0	3.6	V
Input high voltage: Logic 1; All inputs	V _{IH}	V _{DDSPD} × 0.7	V _{DDSPD} + 0.5	V
Input low voltage: Logic 0; All inputs	V _{IL}	−0.6	V _{DDSPD} × 0.3	V
Output low voltage: I _{OUT} = 3mA	V _{OL}	−	0.4	V
Input leakage current: V _{IN} = GND to V _{DD}	I _{LI}	0.10	3	μA
Output leakage current: V _{OUT} = GND to V _{DD}	I _{LO}	0.05	3	μA
Standby current	I _{SB}	1.6	4	μA
Power supply current, READ: SCL clock frequency = 100 kHz	I _{CCR}	0.4	1	mA
Power supply current, WRITE: SCL clock frequency = 100 kHz	I _{CCW}	2	3	mA

Table 13: Serial Presence-Detect EEPROM AC Operating Conditions

All voltages referenced to V_{SS}

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	t _{AA}	0.2	0.9	μs	1
Time the bus must be free before a new transition can start	t _{BUF}	1.3	−	μs	
Data-out hold time	t _{DH}	200	−	ns	
SDA and SCL fall time	t _F	−	300	ns	2
Data-in hold time	t _{HD:DAT}	0	−	μs	
Start condition hold time	t _{HD:STA}	0.6	−	μs	
Clock HIGH period	t _{HIGH}	0.6	−	μs	
Noise suppression time constant at SCL, SDA inputs	t _I	−	50	ns	
Clock LOW period	t _{LOW}	1.3	−	μs	
SDA and SCL rise time	t _R	−	0.3	μs	2
SCL clock frequency	f _{SCL}	−	400	kHz	
Data-in setup time	t _{SU:DAT}	100	−	ns	
Start condition setup time	t _{SU:STA}	0.6	−	μs	3
Stop condition setup time	t _{SU:STO}	0.6	−	μs	
WRITE cycle time	t _{WRC}	−	10	ms	4

- Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
 2. This parameter is sampled.
 3. For a restart condition, or following a WRITE cycle.
 4. The SPD EEPROM WRITE cycle time (t_{WRC}) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

Table 14: Serial Presence-Detect Matrix

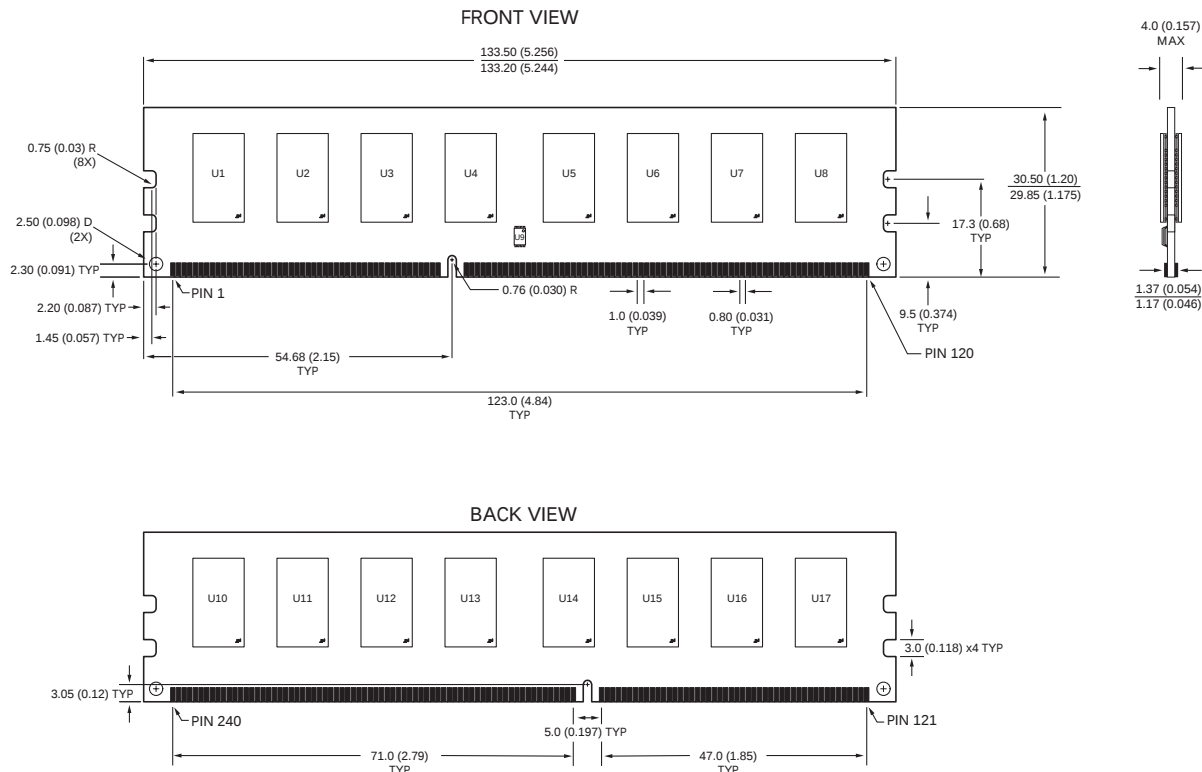
Byte	Description	Entry (Version)	2GB	4GB
0	CRC coverage EEPROM device size Number of SPD bytes written	Bytes 0–116 256 bytes 176 bytes	92	92
1	SPD revision	Rev 1.0	10	10
2	DRAM device type (technology)	DDR3 SDRAM	0B	0B
3	Module type (form factor)	UDIMM	02	02
4	SDRAM device density and internal banks	1Gb/8 banks 2Gb/8 banks	02 –	– 03
5	SDRAM device addressing (row and column counts)	(14,10) (15,10)	11 –	– 19
6	Reserved	0	00	00
7	Module organization (module ranks, SDRAM device width)	2 ranks, x 8 I/O	09	09
8	Module memory bus width	No ECC, 64-bit	03	03
9	Fine time base (FTB) dividend/divisor	5/2	52	52
10	Medium time base (MTB) dividend	1	01	01
11	Medium time base (MTB) divisor	8	08	08
12	SDRAM device minimum cycle time (t_{CK} [MIN])	-1G4/-1G3/-1G1/-1G0 -80C/-80B	0F 14	–/–/0F/0F 14
13	Reserved	0	00	00
14	CAS latencies supported, low byte	-1G4 -1G3 -1G1 -1G0 -80C -80B	34 54 1C 14 06 04	– – 1C 14 06 04
15	CAS latencies supported, high byte	0	00	00
16	MIN CAS latency time (t_{AA} [MIN])	-1G4 -1G3 -1G1 -1G0 -80C -80B	6C 78 69 78 64 78	– – 69 78 64 78
17	MIN write recovery time (t_{WR} [MIN])		78	78
18	MIN RAS# to CAS# delay time (t_{RCD} [MIN])	-1G4 -1G3 -1G1 -1G0 -80C -80B	6C 78 69 78 64 78	– – 69 78 64 78
19	MIN row active-to-row active delay time (t_{RRD} [MIN])	-1G4/-1G3/-1G1/-1G0 -80C/-80B	30 50	–/–/30/30 50
20	MIN row precharge delay time (t_{RP} [MIN])	-1G4 -1G3 -1G1 -1G0 -80C -80B	6C 78 69 78 64 78	– – 69 78 64 78
21	Upper nibble for t_{RAS} and t_{RC}		11	11
22	MIN active-to-precharge delay time (t_{RAS} [MIN]), LSB	-1G4/-1G3 -1G1/-1G0/-80C/-80B	20 2C	– 2C

Table 14: Serial Presence-Detect Matrix (continued)

Byte	Description	Entry (Version)	2GB	4GB
23	MIN active-to-active/refresh (t_{RC} [MIN]), LSB	-1G4 -1G3 -1G1 -1G0 -80C -80B	8C 98 95 A4 90 A4	– – 95 A4 90 A4
24	MIN refresh recovery delay time (t_{RFC} [MIN]), LSB	1Gb 2Gb	70 –	– 00
25	MIN refresh recovery delay time (t_{RFC} [MIN]), MSB	1Gb 2Gb	03 –	– 05
26	MIN internal WRITE-to-READ command delay time (t_{WTR} [MIN])		3C	3C
27	MIN internal READ-to-PRECHARGE command delay time (t_{RTP} [MIN])		3C	3C
28	MIN four active window delay time (t_{FAW} [MIN]) upper nibble	-1G4/-1G3 -1G1/-1G0/-80C/-80B	00 01	– 01
29	MIN four activate window delay time (t_{FAW} [MIN]), LSB	-1G4/-1G3 -1G1/-1G0 -80C/-80B	F0 2C 40	– 2C 40
30	SDRAM device output drivers supported		82	82
31	SDRAM device thermal refresh options		05	05
32–59	Reserved, general section		00	00
60	Module NOM height	30mm	0F	0F
61	Module MAX thickness	Dual rank, 4.0mm	11	11
62	Reference raw card used	UDIMM R/C B	01	01
63	Address mapping from edge connector to DRAM devices	Mirrored	01	01
64–116	Reserved	0	00	00
117	Module manufacturer ID (continuation code)		80	80
118	Module manufacturer ID (manufacturer's ID code)		2C	2C
119	Module manufacturing location	1–12	01-0C	01-0C
120–121	Module manufacturing date	–	Variable data	Variable data
122–125	Module serial number	–	Variable data	Variable data
126, 127	CRC (cyclic redundancy check)	-1G4 -1G3 -1G1 -1G0 -80C -80B	9E23 7D3C 4408 27FD D3AD DC51	– – DBDE B82B 4C76 4387
128–145	Module part number (ASCII)	–	Variable data	Variable data
146	Module revision code, SDRAM device die revision	–	Variable data	Variable data
147	Module revision code, PCB revision	–	Variable data	Variable data
148	DRAM device manufacturer ID (continuation code)		80	80
149	DRAM device manufacturer ID (manufacturer's ID code)		2C	2C
150–175	Reserved for manufacturer-specific data		00	00
176–255	Reserved for customer-specific data		FF	FF

Module Dimensions

Figure 3: 240-Pin DDR3 UDIMM



- Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
 2. The dimensional diagram is for reference only.



8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900

prodmktg@micron.com www.micron.com Customer Comment Line: 800-932-4992

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This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.