USB375x

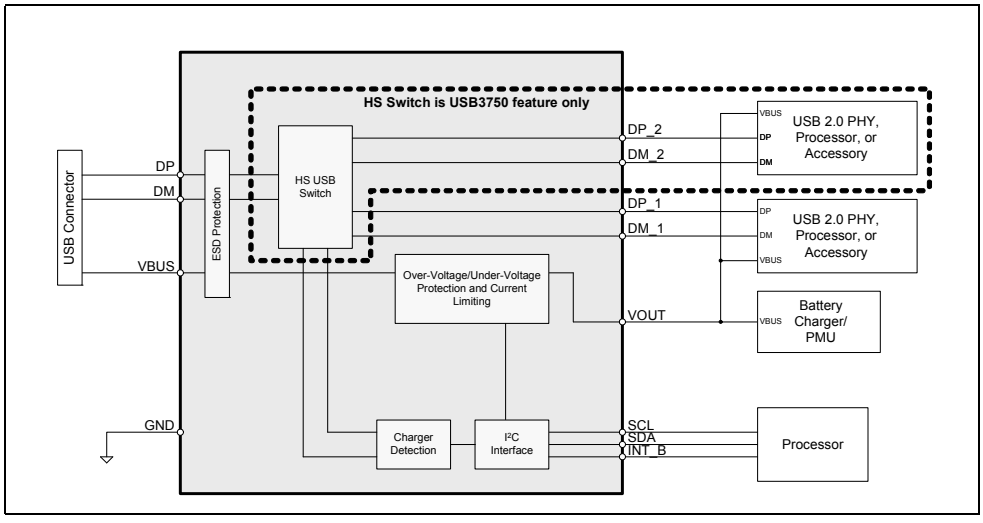
USB 2.0 Protection IC with Battery Charger Detection

PRODUCT FEATURES

Datasheet

- **VBUS** Over-Voltage Protection
  - Protects internal circuits from VBUS up to 9V
  - Over-Voltage/Under-Voltage Lockout opens VBUS switch
  - Interrupt to indicate Over-Voltage/Under-Voltage Lockout
  - Integrated Low R_{DSON} FET
- USB Port ESD Protection (**DP**/**DM**/**VBUS**)
  - ±15kV (air discharge)
  - ±15kV (contact discharge)
  - IEC 61000-4-2 level 4 ESD protection without external devices
- High Speed USB Mux for multiplexing the USB lanes between different functions (USB3750 only)
  - Switch the USB connector between two different functions
  - High bandwidth USB switch passes HS USB signals
- Provides USB Battery Charger Detection for:
  - USB-IF Battery Charging compliant Dedicated Charging Ports (DCP)
  - USB-IF Battery Charging compliant Charging Downstream Port (CDP)
  - Standard Downstream Port (SDP); i.e. USB host or downstream hub port
  - Dedicated SE1 type chargers
- Dead Battery Provision Support (USB375x-1 only)
  - Allows 100mA trickle charging from VBUS when attached to a Standard Downstream Port (SDP) while not enumerated
  - Built-in 100mA current limiting option
- SMSC RapidCharge Anywhere™ Provides:
  - 3-times the charging current through a USB port over traditional solutions
  - USB-IF Battery Charging 1.2 compliance to any portable device
  - Charging current up to 1.5Amps via compatible USB host or dedicated charger
  - Dedicated Charging Port (DCP), Charging (CDP) & Standard (SDP) Downstream Port support
- flexPWR® Technology
  - Extremely low current design ideal for battery powered applications
  - Maximizes power delivered to the system
- Industrial Operating Temperature -40°C to +85°C

USB375x Block Diagram



DATASHEET

Order Numbers:

ORDER NUMBER	PACKAGE TYPE	PACKAGE SIZE
USB3750A-1-A4-TR (see Note 1)	16 pin, QFN lead-free RoHS compliant package	3.0mm x 3.0mm
USB3751A-1-A4-TR (see Note 2)		
USB3751A-2-A4-TR (see Note 3)		

Note 1 Provides HS mux and support for 100mA dead battery current limiting.

Note 2 Provides support for 100mA dead battery current limiting.

Note 3 Does not provide support for 100mA dead battery current limiting.

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

Please contact your SMSC sales representative for additional documentation related to this product such as application notes, anomaly sheets, and design guidelines.

0.1 Reference Documents

- Universal Serial Bus Specification, Revision 2.0
- USB Battery Charging Specification, Revision 1.1

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Chapter 1 General Description

The USB375x integrates many features that have historically been discrete devices in a mobile product. This device provides significant VBUS protection for the entire system, robust USB interface ESD protection, a USB 2.0 compliant High Speed switch, and USB-IF Battery Charger Detection (revision 1.1) capabilities that are essential to the latest mobile products.

Several advanced features allow the USB375x to be optimized for portable applications and to reduce both eBOM part count and printed circuit board (PCB) area. Outstanding ESD robustness eliminates the need for external ESD protection devices.

In addition to the integrated ESD protection on the USB interface, the USB375x provides VBUS Over-Voltage Protection (OVP).

The USB375x integrated battery charger detection circuitry supports USB-IF Battery Charger Detection. Battery charger detection will begin automatically whenever VBUS rises above the UVLO threshold, and can also be completed manually through the I^2C interface. The USB375x can detect a range of USB battery chargers including a Standard Downstream Port (SDP), a Charging Downstream Port (CDP), and a Dedicated Charging Port (DCP). For more information on USB battery charger detection, please see the USB Battery Charging Specification, Revision 1.1.

The I^2C interface gives processor control over the USB Switch, charger detection, OVLO settings, and status of the USB375x. In addition, custom charger detection can be implemented through the I^2C interface.

The USB375x family is enabled with SMSC's RapidCharge Anywhere™ which supports USB-IF Battery Charging 1.1 for any portable device. RapidCharge Anywhere™ provides three times the charging current through a USB port over traditional solutions which translate up to 1.5Amps via compatible USB host or dedicated charger. In addition, this provides a complete USB charging ecosystem between device and host ports such as Dedicated Charging Port (DCP), Charging (CDP) and Standard (SDP) Downstream Ports.

Chapter 2 Pin Layout

2.1 Pin Diagram

The USB375x is available in a QFN (3 x 3 mm) package. The USB3750 pin diagram is detailed in Figure 2.1. The USB3751 pin diagram is detailed in Figure 2.2.

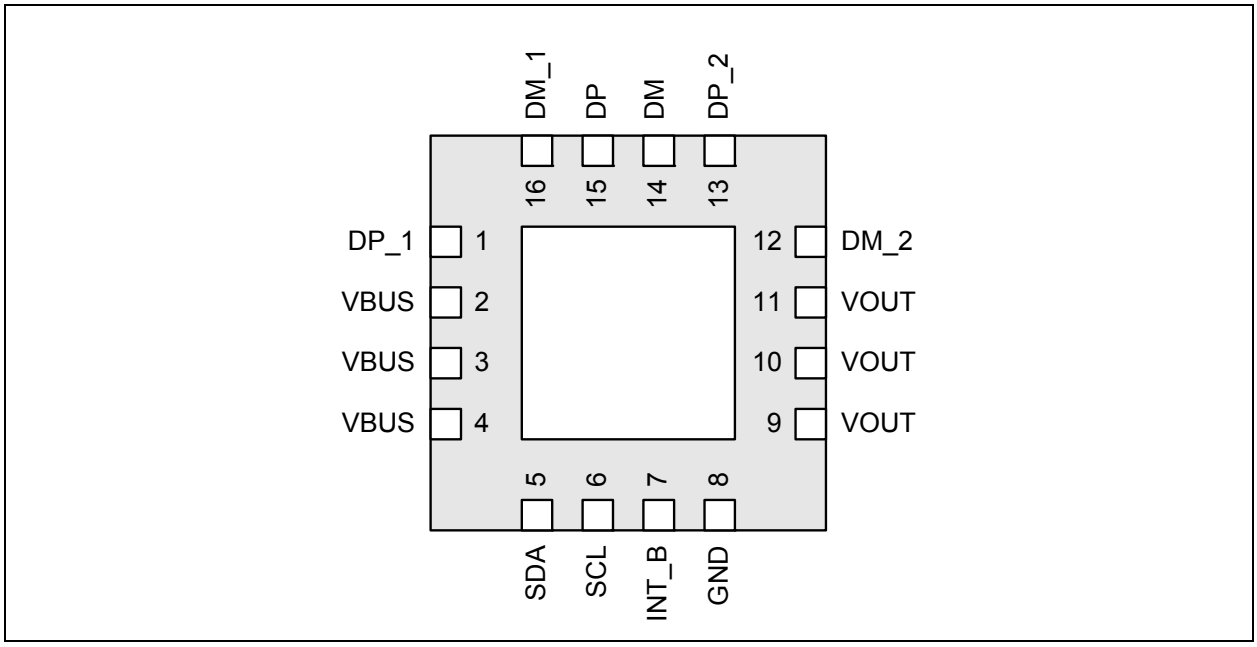


Figure 2.1 QFN Package Diagram (USB3750)

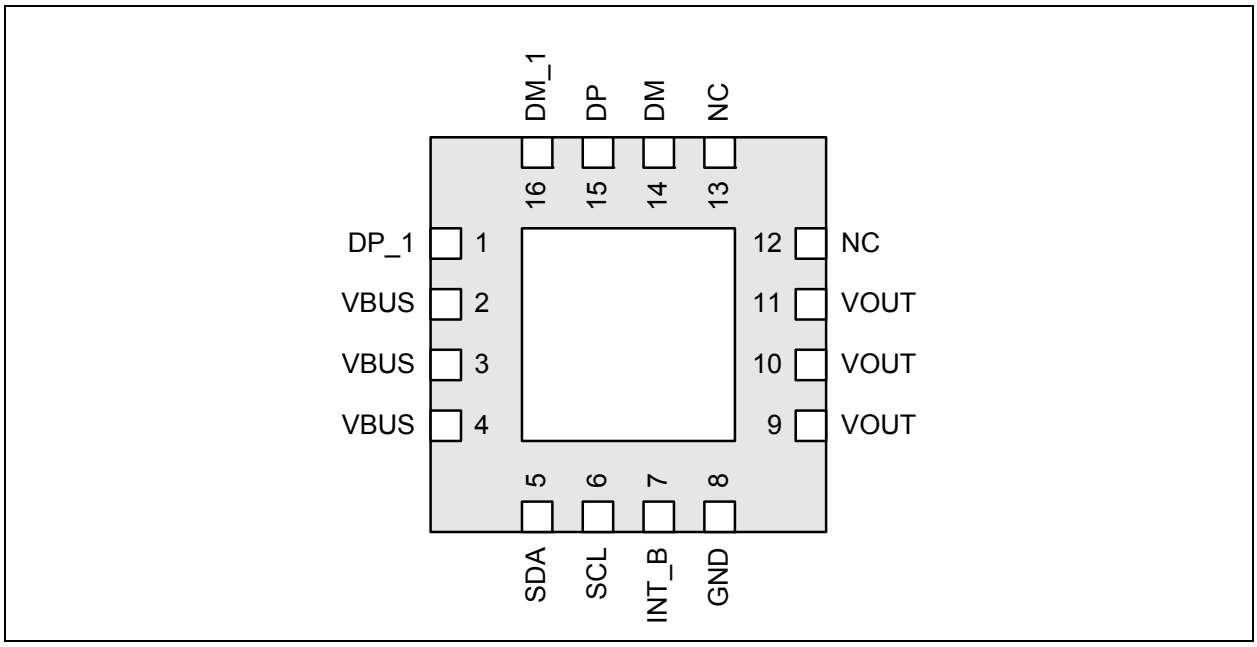


Figure 2.2 QFN Package Diagram (USB3751)

2.2 Ball/Pin Definitions

The following table details the ball/pin definitions for the package diagrams above.

BALL PIN	NAME	TYPE/ DIRECTION	DESCRIPTION
15	**DP**	Analog	USB Mux Output
14	**DM**	Analog	
1	**DP_1**	Analog	USB Mux Input 1
16	**DM_1**	Analog	
13	**DP_2**	Analog	USB Mux Input 2 (USB3750 Only) USB3751 should leave these pins unconnected.
12	**DM_2**	Analog	
8	**GND**	Analog	Ground. The QFN package flag should also connected to ground.
6	**SCL**	Input	I^2C Clock input. This pin is an open drain output and requires a 10Kohm pull-up.
5	**SDA**	Open Drain/ IO	Bi-Directional I^2C data. This pin is an open drain output and requires a 10Kohm pull-up.
7	**INT_B**	Open Drain/ Output	Open Drain Interrupt. This pin is an open drain output that is pulled low when an interrupt occurs. A 10Kohm pull-up is required on this pin.
9	**VOUT**	Analog	Overvoltage switch output. This pin is connected to VBUS when the overvoltage protection switch is enabled. It is also the output of the 100mA current limit. The three **VOUT** pins must be connected together. When **VBUS** is between UVLO and OVLO **VOUT** is connected to **VBUS**. When **VBUS** is below UVLO or above OVLO the USB375x will tri-state.
10			
11			
2	**VBUS**	Analog	VBUS pin of the USB connector. The three **VBUS** pins must be connected together. When the OVP switch is closed, the **VBUS** pin will be isolated from **VOUT**. When the OVP switch is open, **VBUS** will be connected to **VOUT**. The USB375x is powered from this pin.
3			
4			

Chapter 3 Electrical Specifications

3.1 Absolute Maximum Ratings

Table 3.1 Absolute Maximum Ratings

DESCRIPTION		RATING	UNIT
VBUS Voltage to **GND**		-0.3 to 9.0	V
VOUT Voltage to **GND**		-0.3 to 7.5	V
Any other pin to **GND**		-0.3 to 5.5	V
Operating Temperature Range		-40 to +85	C
Storage Temperature Range		-55 to +150	C
ESD Rating	HBM	8,000	V
	IEC-61000-4-2	15,000 (Air) 15,000 (Contact)	V
ESD Rating (SDA, SCL, INT_B)	HBM	1,500	V

Stresses beyond the Absolute Maximum Ratings may damage the USB375x.

3.2 Electrical Specifications

Table 3.2 Electrical Specifications

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
V_{VBUS} = 5.0V, T_A = -40C to 85C, all typical values at T_A = 27C unless otherwise noted.						
VBUS Characteristics						
VBUS Operating range	V_{VBUS}	2		9	V	
VBUS Over Voltage Lockout	V_{OVLO}	6.2	6.5	6.9	V	
VBUS Under Voltage Lockout	V_{UVLO}	3.3	3.4	3.8	V	
VBUS Over Voltage Hysteresis	V_{OVLO}		100		mV	
VBUS Under Voltage Hysteresis	V_{UVLO}		100		mV	
Operating Current (OVP open)	I_{DD_OFF}		110		uA	$V_{VBUS} < V_{UVLO}$
Operating Current (OVP closed)	I_{DD_ON}	75	115	370	uA	$V_{UVLO} < V_{VBUS} < V_{OVLO}$
Operating Current (100mA Limit enabled)	I_{DD}	150	185	480	uA	$V_{UVLO} < V_{VBUS} < V_{OVLO}$

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
VBUS Switch Characteristics						
Overvoltage Switch ON Resistance	R_{ON_VBUS}		70		mohm	QFN package
Overvoltage Switch Current				1.8	A	$V_{UVLO} < V_{VBUS} < V_{OVLO}$
Overvoltage Switch OFF Leakage	I_{OFF_VBUS}			1	uA	VBUS = 5.0V; VOUT = 0V
VBUS Resistance to Ground	R_{VBUS}	100			Kohm	
VBUS Capacitance	C_{VBUS}	1.0			uF	
Charger Detection Characteristics 4.4 < **VBUS** < 5.5V						
DP and **DM** leakage				1	uA	0.0V < Vpin < 3.3V
Data Source Voltage	V_{DAT_SRC}	0.5		0.7	V	I_{DAT_SRC} > 250uA
Data Detect Voltage	V_{DAT_REF}	0.25		0.4	V	
Data Connect Detect Current Source	I_{DP_SRC}	7		13	uA	
Data Sink Current	I_{DAT_SINK}	50		150	uA	
DP/DM Single Ended RX Threshold	V_{SE_RX}	0.8		1.95	V	4.75V < VBUS < 5.25V
SE1 High Current Charger RX Threshold	V_{SE_RXH}	2.1		2.56	V	4.75V < VBUS < 5.25V
DP/DM Pull Down Resistors	R_{PD}	14.25		24.8	Kohm	
USB Mux Characteristics (USB3750 Only)						
USB Mux On Resistance	R_{ON_USB}			10	ohm	0V < Vin < 3.3V
				2.5		0V < Vin < 0.4V
USB Mux Off Leakage	I_{OFF_USB}			0.85	uA	0V < Vin < 3.3V
On Capacitance	C_{ON_USB}			9	pF	
Off Capacitance	C_{OFF_USB}			6.5	pF	
Off Isolation				-35	dB	R_L = 50 ohm, F = 250MHz
Crosstalk				-40	dB	R_L = 50 ohm, F = 250MHz
Bandwidth (-3dB)	BW			1000	MHz	R_L = 50 ohm, C_L = 0pF
				800		R_L = 50 ohm, C_L = 5pF
				500		R_L = 50 ohm, C_L = 10pF
Control Signal Characteristics						
Input Logic High Threshold	V_{IN_H}	1.4			V	VBUS > UVLO

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
Input Logic Low Threshold	V_{IN_L}			0.4	V	VBUS > UVLO
Output Drive Strength	V_{OUT_L}			0.4	V	VBUS > UVLO, 4.0mA sink current
Control Signal Leakage Current			1		nA	0 < Vpin < **VOUT**
Timing Characteristics						
Clock Accuracy	T_{CLK}	0.5	1	2	mS	Oscillator Accuracy
Soft POR Reset Time	T_{SOFT_POR}			20	mS	Time to autoclear Soft POR.
UVLO and OVLO Release Timer	$T_{VLO\_RELEASE}$	3		6.5	mS	
UVLO and OVLO Engage Time	T_{VLO_ENGAGE}	0.5		1.7	mS	
Data Contact Detect Timeout	T_{DCD_TOUT}			900	mS	
Vdat_src and Idat_sink Enable Time	T_{VDPSRC_ON}	40	80	160	mS	
Delay from Vdat_det to OVP switch enable	T_{VDPSRC_HICRNT}	40	80	160	mS	
SE1 Charger Detection wait for SE1 timer	T_{CD_SE1}	40	80	160	mS	
Interrupt Self Clear Timer	T_{INT}	0.5	1	2	mS	

3.3 Timing Diagrams

3.3.1 UVLO and OVLO Timing

The timing diagram below shows the operation of the OVP switch as VBUS crosses the UVLO and OVLO thresholds. The behavior of the INT_B signal is also shown in Figure 3.1 below.

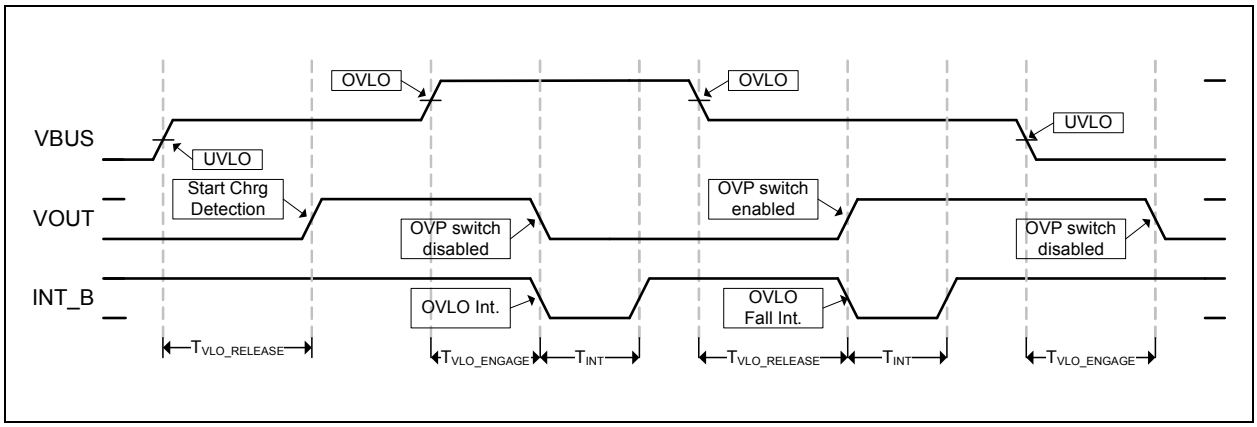


Figure 3.1 UVLO and OVLO Timing

3.3.2 Automatic Charger Detection Timing

The timing diagrams below illustrate the automatic charger detection timing that is followed when implementing the automatic charger detection flow charts shown in this section.

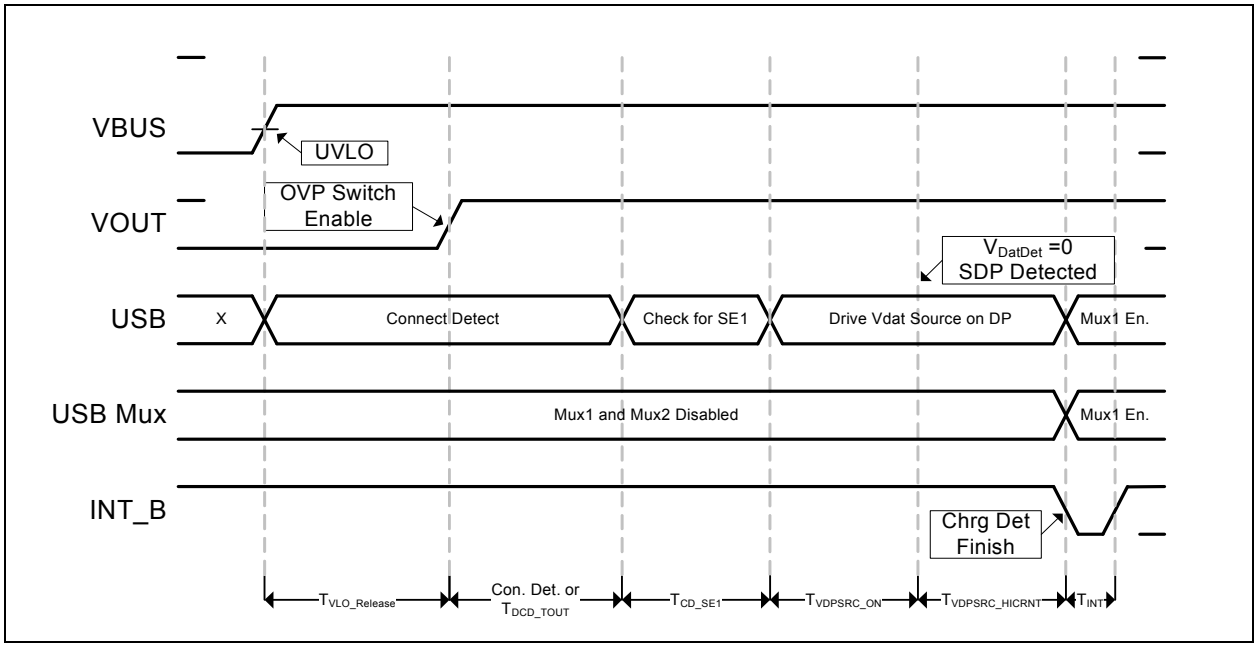


Figure 3.2 Charger Detection Timing SDP (USB3750-1)

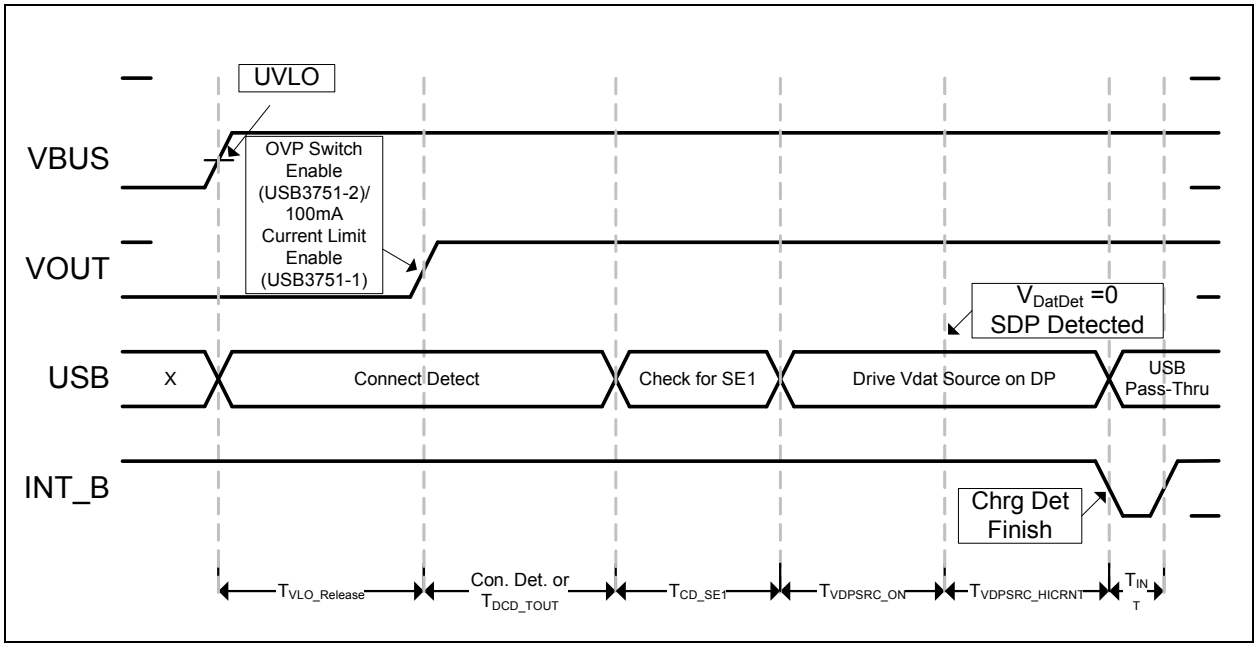


Figure 3.3 Charger Detection Timing SDP (USB3751-x)

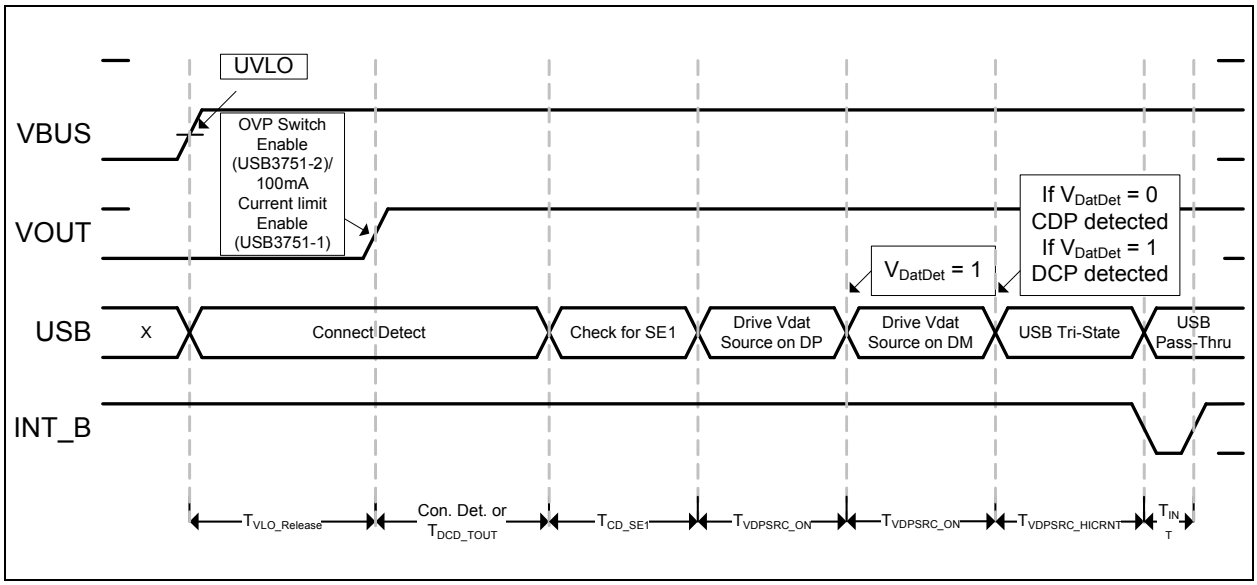


Figure 3.4 Charger Detection Timing DCP or CDP (USB3751-x)

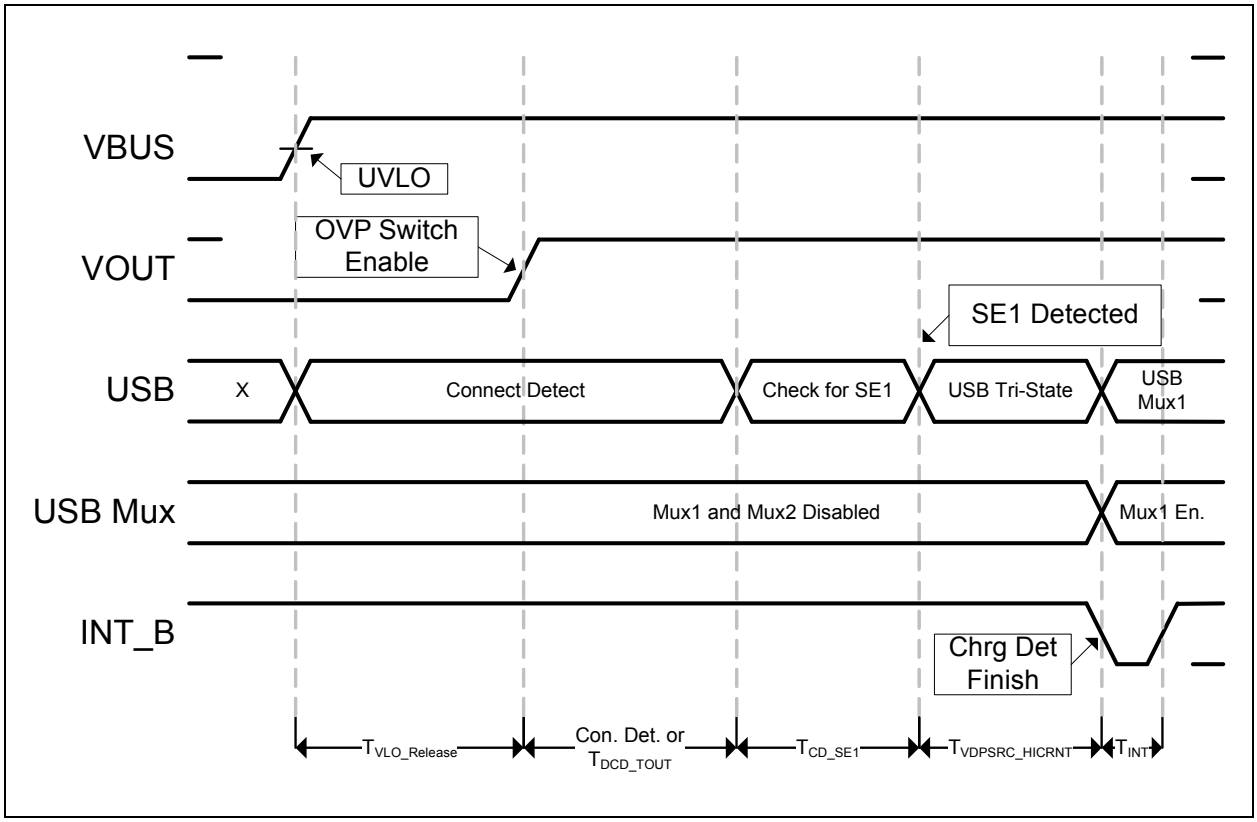


Figure 3.5 Charger Detection Timing SE1 Charger (USB3750-1)

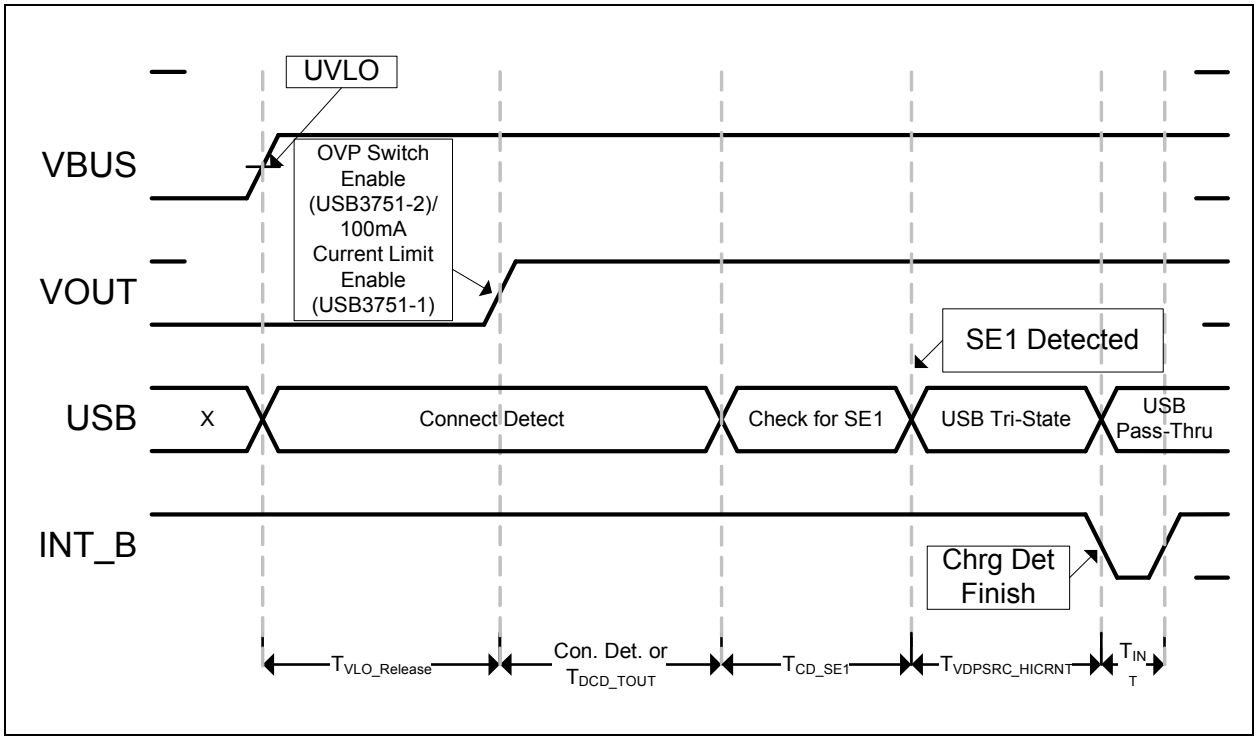


Figure 3.6 Charger Detection Timing SE1 Charger (USB3751-x)

Chapter 4 General Operation

The USB375x is an integrated USB protection device, battery charger detection device, and High Speed USB mux (USB3750 only). The USB375x is designed to protect a USB product from electrical overstress on the USB connector. The USB375x includes several features designed to improve the reliability and speed the design of products designed with a USB interface.

The USB3750 includes a high bandwidth HS USB mux. The mux allows high speed signals to pass through and still meet HS USB signaling requirements.

The USB375x will protect the system from ESD stress events on **VBUS**, **DP**, and **DM**. The USB375x provides ESD protection to the IEC-61000 ESD specification.

The low resistance VBUS overvoltage protection switch protects the internal circuitry from VBUS over voltage events. When VBUS is outside the safe operating range VBUS switch will automatically open.

The USB375x also includes the capability to detect various USB battery chargers, including those defined in the USB Battery Charging Specification, Revision 1.1.

To support the device dead battery conditions as defined in the USB Battery Charging Specification, Revision 1.1, the USB375x-1 has the ability to drive V_{DAT_SRC} on **DP** which allows a device with a dead battery to draw 100mA from a USB host. This will allow a device to charge a dead battery without violating the USB specifications. The USB375x-1 also includes a current limit to prevent the unconfigured current from exceeding 100mA. Note, this feature is not available with the USB375x-2.

The USB3750 block diagram is shown Figure 4.1 and the USB3751 block diagram is shown Figure 4.2.

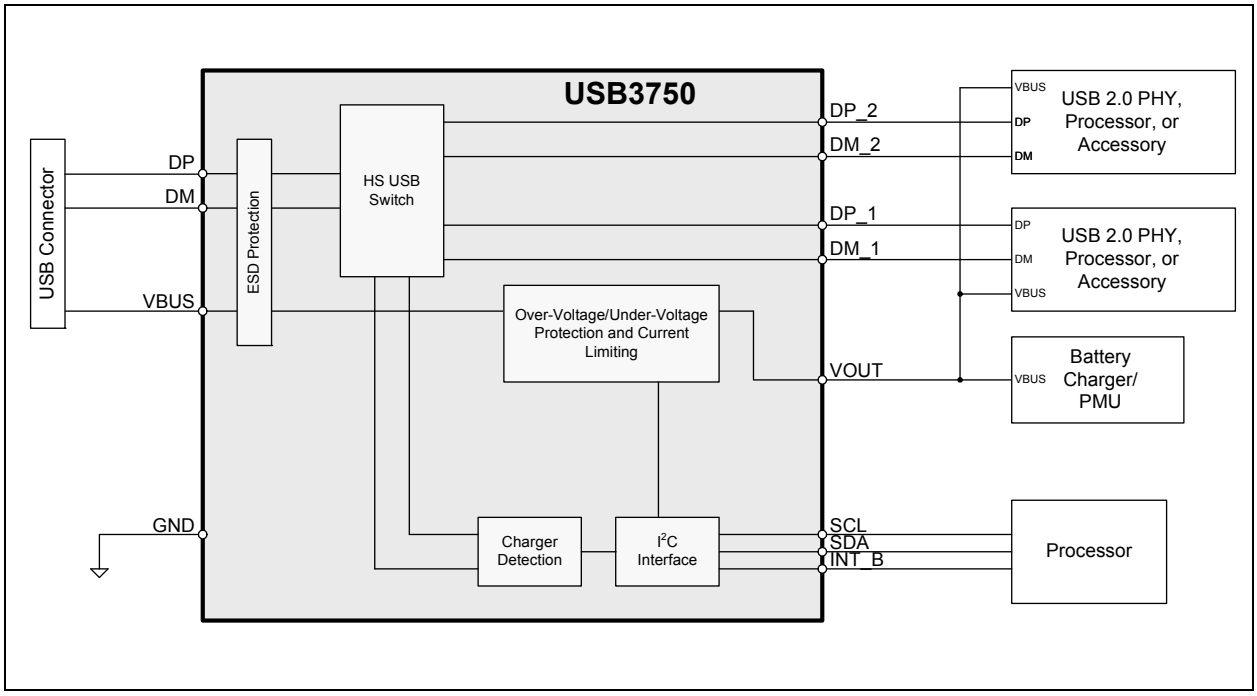


Figure 4.1 USB3750 Block Diagram

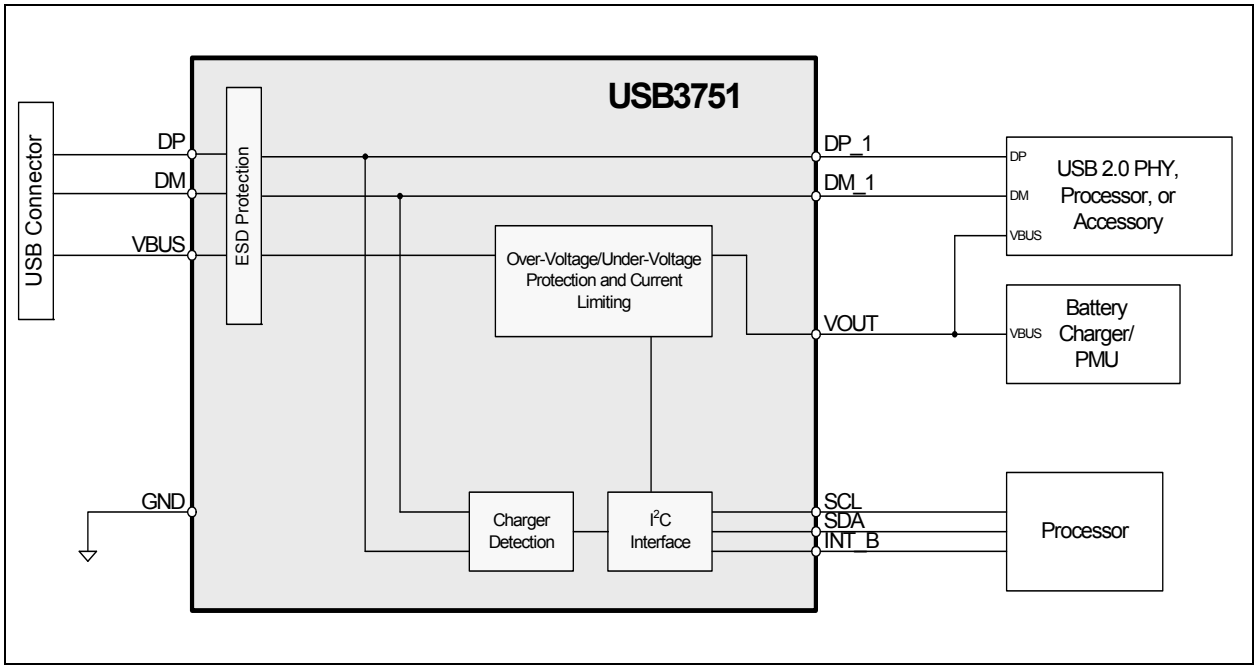


Figure 4.2 USB3751 Block Diagram

4.1 VBUS Protection Switch

The USB375x protects the entire system from errant VBUS voltages, whether over-voltage or under-voltage conditions. The device is able to dynamically monitor the VBUS voltage levels and take appropriate action by opening the integrated VBUS Protection Switch when these errant conditions occur. Specifically, when VBUS is below the Under Voltage Lock-Out (UVLO) level or above the Over Voltage Lock-Out (OVLO) level, the VBUS switch will open thereby disconnecting the VBUS pin from VOUT. See Section 3.3 for UVLO and OVLO timing diagrams. Manual control of the VBUS Switch, as well as switch configuration can be handled through the I2C interface. See Section 4.4.2 for I2C register descriptions.

4.1.1 100mA Current Limit (USB375x-1 Only)

The USB375x-1 provides a 100mA current limit feature which allows a portable system with a dead battery to still draw 100mA from a compliant host. When plugged into a Standard Downstream Port (SDP), the USB375x-1 will enable the 100mA current limit until the system controller enables the OVP switch in the I2C registers of the USB375x-1. When plugged into any other charger, the USB375x-1 will enable the 100mA current limit during charger detection, and will disable the 100mA current limit once charger detection has completed. Figure 4.6 details the charger detection flow of the USB375x-1.

4.2 Charger Detection

The USB375x includes the circuitry required to implement the USF-IF Battery Charging Specification (revision 1.1). The USB375x will automatically perform a charger detection upon start-up. The USB375x includes a state machine to provide the detection of a wide variety of USB charger detection methods listed in Table 4.1. When any of the USB chargers are plugged into the system, the USB375x will detect a charger plug in event, determine what type of charger it is, and write the type of charger information into the I2C register as shown in the following table. In addition, there are two methods to alert the system that a charger has been detected by the USB375x. The first was through the I2C register as mentioned above. The second is through the INT_B pin. When a compliant charger is plugged in and detected, the USB375x will automatically drive the INT_B signal low. Figure 4.4 details the automatic charger detection flow of the USB3750-1, Figure 4.5 details the automatic charger detection flow of the USB3751-1, and Figure 4.6 details the automatic charger detection flow of the USB3751-2.

Table 4.1 Valid Chargers

USB CHARGER TYPE	**DP/DM PROFILE**	**I^2C REG 0 BITS[7:5]** (*ChargerType)*
DCP (Dedicated Charging Port, defined in Battery Charging 1.1 specification)	Shorted < 200ohm	001
CDP (Charging Downstream Port, defined in Battery Charging 1.1 specification)	V_{DP} reflected to V_{DM}	010 (*EnhancedChrgDet* = 1)
SDP (Standard Downstream Port) USB Host or downstream hub port	15Kohm pull-down on **DP** and **DM**	011
SE1 Charger Low Current Charger	DP = 2.0V DM = 2.0V	100 (SE1ChrgDet =1)
SE1 Charger High Current Charger	DP = 2.0V DM = 2.7V	101 (SE1ChrgDet =1)

4.2.1 Charger Detection Circuitry

The charger detection circuitry shown Figure 4.3 is used to detect the type charger attached to the USB connector.

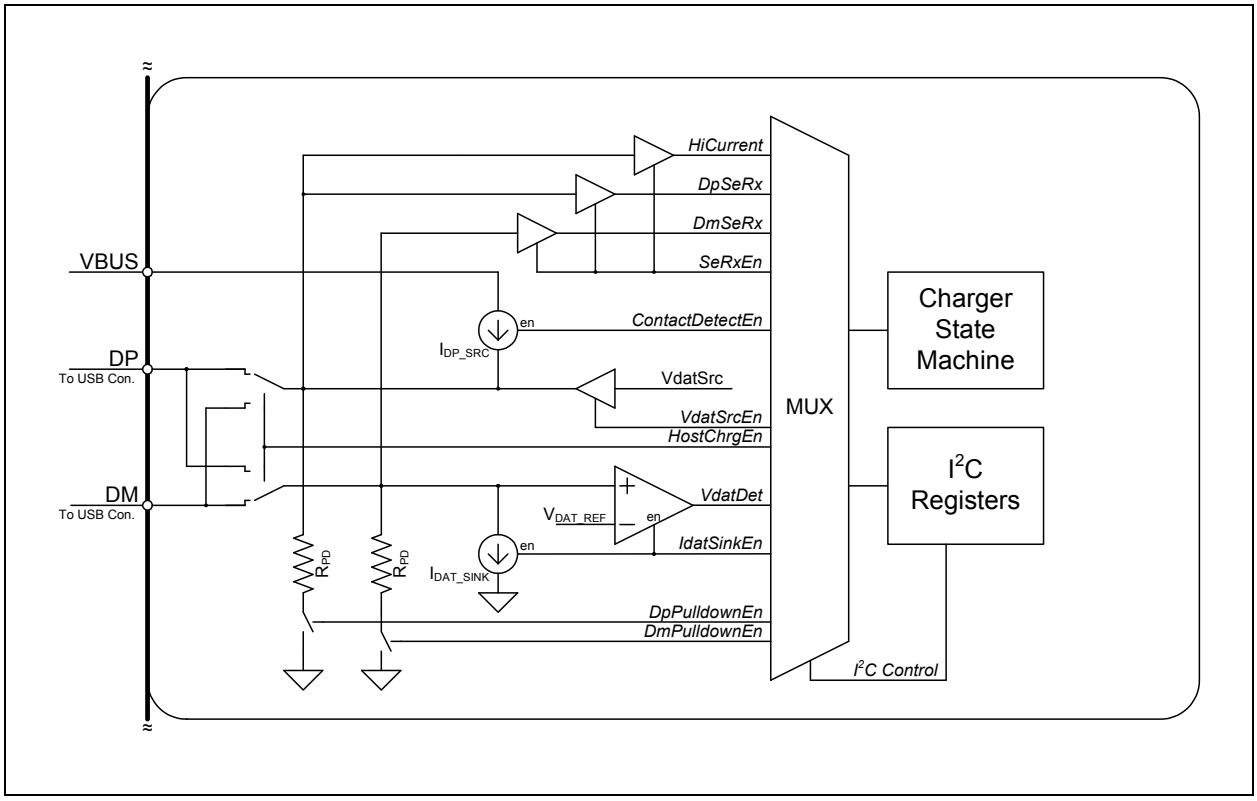


Figure 4.3 USB Charger Detection Block Diagram

Note: The *italic names* in the Figure 4.3 correspond to bits in the I²C register set.

The *VdatDet* output is qualified with the Linestate[1:0] value. If the Linestate is not equal to 00b the *VdatDet* signal will not assert.

For the USB3750, *EnableMux1* or *EnableMux2* should not be set while charger detection operations are performed. During the automatic charger detection *EnableMux1* or *EnableMux2* will be disabled. These will need to be disabled by the I²C master if a custom charger detection is performed through I²C.

4.2.2 Automatic Charger Detection

Automatic charger detection will be begin after VBUS crosses the UVLO threshold, and will follow the flow charts shown below in Figure 4.4 and Figure 4.6. The flow chart timing can be found in Section 3.3.2. When automatic charger detection has completed, the INT_B signal will go low, and the type of charger that was detected will be reflected in the *ChargerType* bits of I^2C REG 0 BITS [7:5].

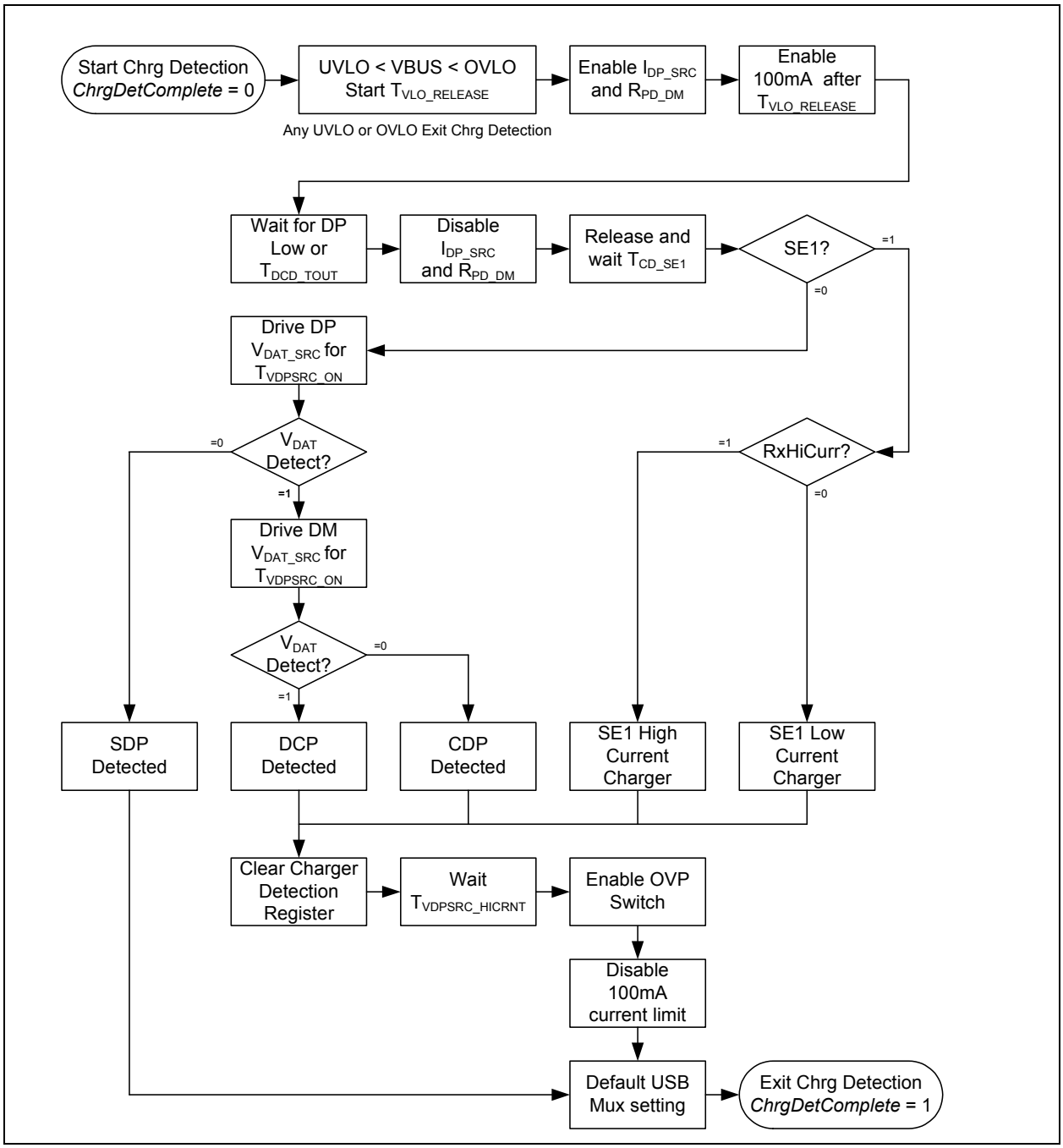


Figure 4.4 Charger Detection Flow Chart (USB3750-1)

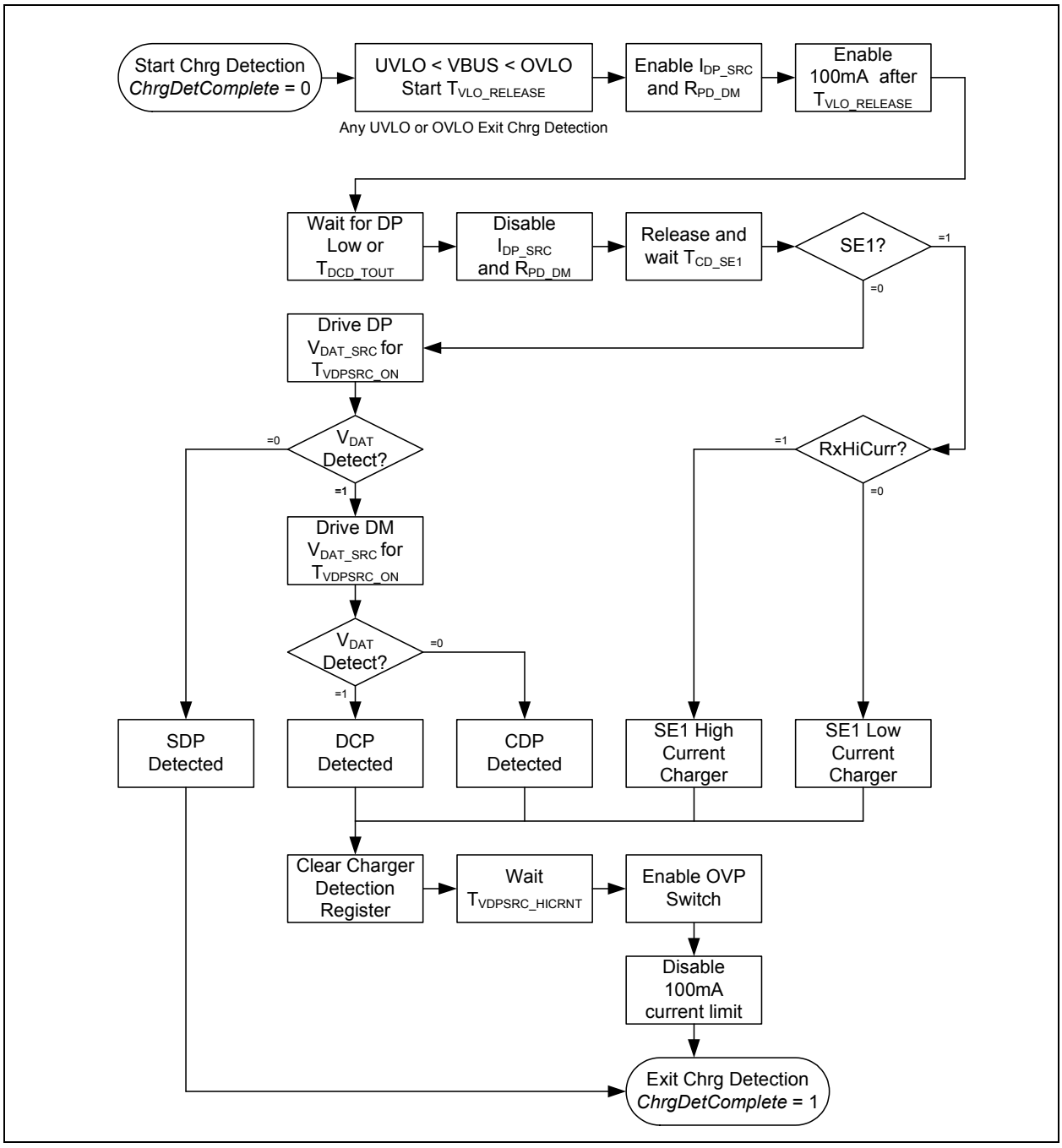


Figure 4.5 Charger Detection Flow Chart (USB3751-1)

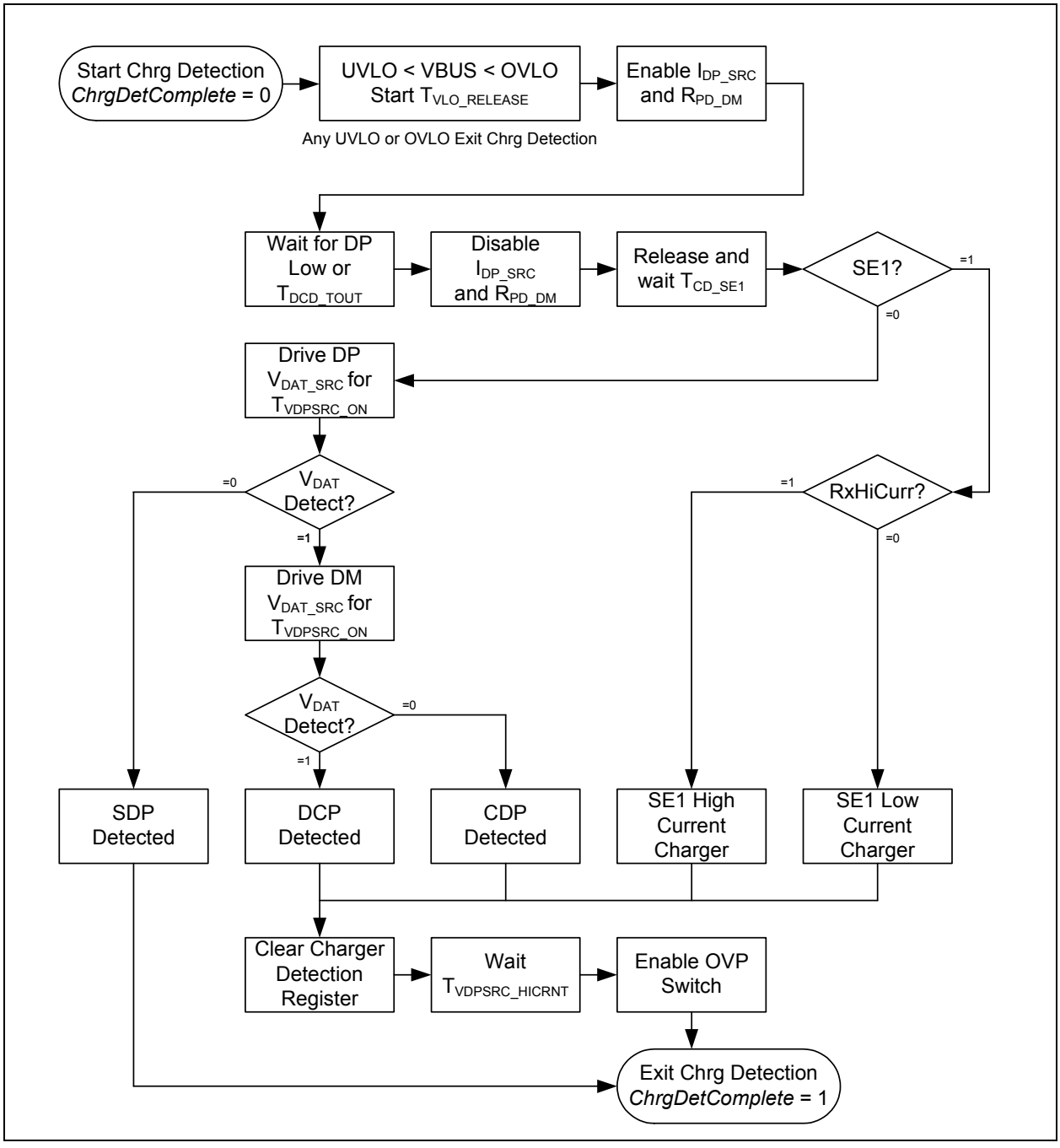


Figure 4.6 Charger Detection Flow Chart (USB3751-2)

4.3 USB Mux (USB3750 Only)

The USB mux is designed to pass High Speed USB signals to the USB connector, and allows for two USB inputs to be multiplexed into one USB output. Either switch path is enabled through the I2C interface, and the switch paths are disabled in the event of UVLO or OVLO.

The USB Mux is designed to pass USB signals from 0 to 3.3V. It is not designed to pass signals that go above 3.3V or below ground.

During power-up and charger detection the USB Mux switches will be disabled regardless of the *EnableMux1* and *EnableMux2* settings.

Once power-up and charger detection are complete *EnableMux1* is enabled by default.

4.4 USB375x Registers

All registers are reset when VBUS goes below UVLO. All registers are accessed through the I2C interface defined below.

4.4.1 I2C Interface

The SDA and SCL pins comprise the I2C interface of the USB375x. The I2C master controls all traffic to the USB375x. If the USB375x has a change in status it can assert the **INT_B** by pulling this line to ground. The USB375x **INT_B** line will stay low and then auto-clear after 1mS or until cleared by reading the Status Register. This prevents **INT_B** from masking other interrupts if the line is shared with other I2C devices.

SCL, **SDA**, and **INT_B** will be tri-stated until **VBUS** is above the UVLO. **VBUS** must be present to operate the I^2C interface.

SCL is an input only pad. **SDA** is bi-directional and can be configured as an input or an open drain output during I2C operations.

SDA, and **INT_B** are open collector when configured as an output. This requires an external pull-up resistor on **SDA** and **INT_B**.

The USB375x-1 requires I2C communications in order for the default USB path to be enabled. By default, the 100mA current limit is enabled. Only devices that draw <100mA will be enabled through the path as part of dead battery provision support. In order to bypass this limit, bits 0 (EnableOVP Switch) and 2 (OverideVBUS) in Register 1 (Configuration Register) need to be set via I2C.

4.4.2 I^2C Register Access

4.4.2.1 I^2C Read Command

The slave supports two types of reads, single reads, and continuous reads. In a single read the master asserts a NACK after the first read data. The format for a single read is shown in Figure 4.7. The read command has three phases. These three phases are device address phase, register address phase, and read data phase. Each phase is terminated by an ACK or NACK. The device address phase consists of the 7-bit slave address followed by a '1' to indicate a read. If the address matches the slave's address then the slave drives an ACK. The register address phase consists of an 8-bit register address. The slave will always ACK the register address. In the data phase the slave will return the

register read data. If the register address was a valid register than the slave will return the data, otherwise it will return 0xFF.

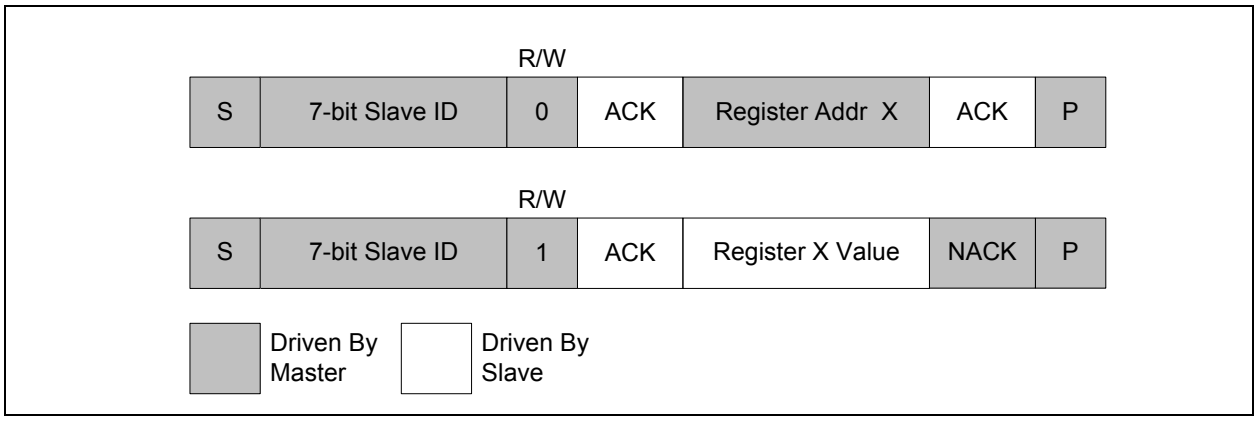


Figure 4.7 I²C Single Read

The continuous read command is similar to the single read command, however after the read data the master will drive an ACK and then provide another register address. The master will then wait for the read data as shown in Figure 4.8. The continuous read is terminated by the master by driving a NACK after the last read data and then asserting a STOP condition.

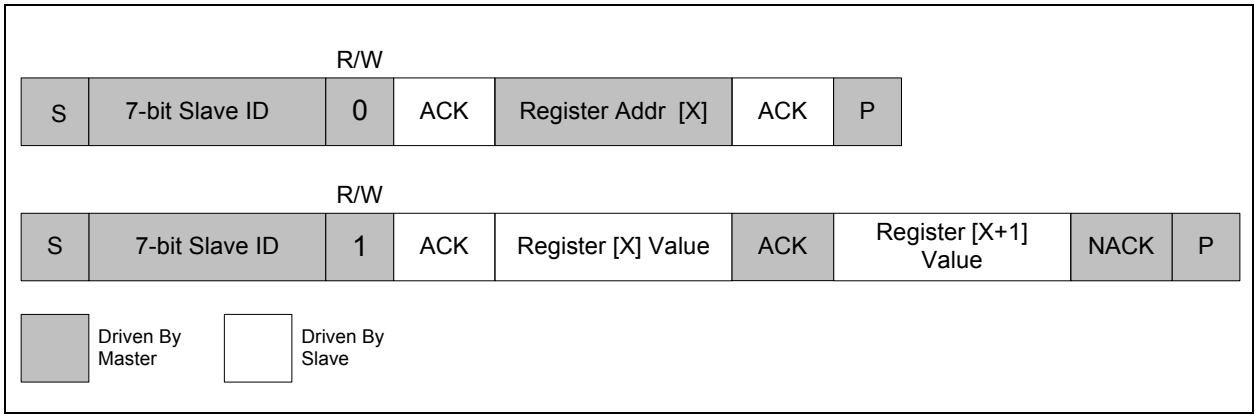


Figure 4.8 I²C Continuous Read

4.4.2.2 I²C Write Command

Similar to the read commands, the slave supports two types of write commands. The single write command is show in Figure 4.9. The slave will always ACK the write data. Only the lower 4 bits of the register address are decoded. Writes to undefined and read-only registers will be ignored.

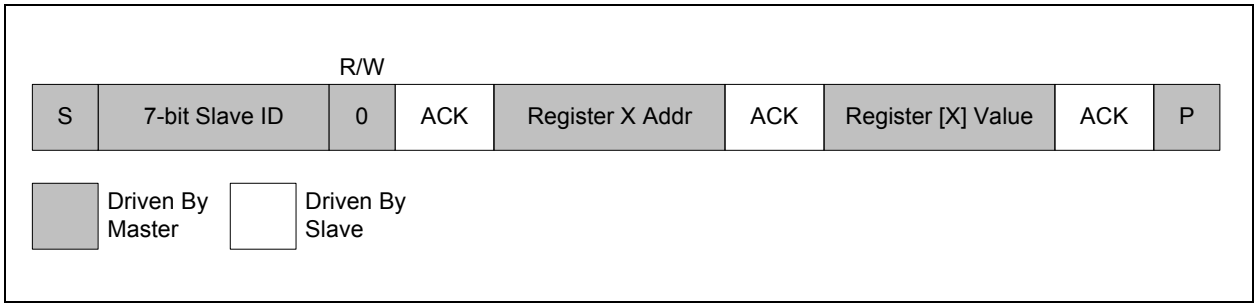


Figure 4.9 I²C Single Write

The continuous write is shown in Figure 4.10. In this case after the ACK of the write data, the master will drive the next register address. The continuous write will be terminated when the master asserts a STOP.

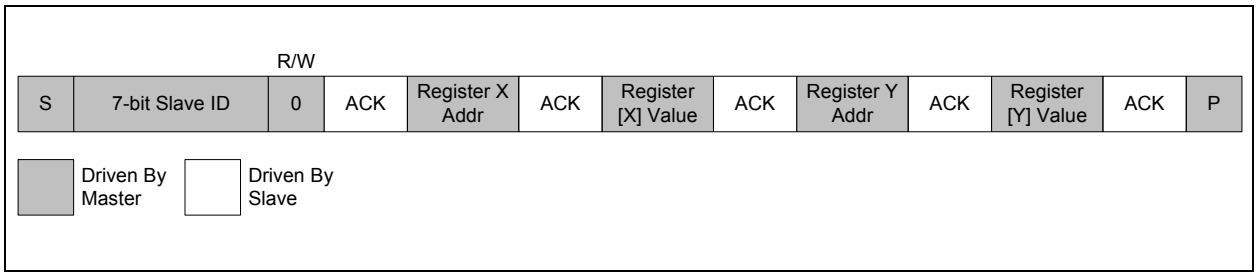


Figure 4.10 I²C Continuous Write

4.4.3 I²C Address

The default I2C address is 1101000. The two LSB are set by the OTP registers.

Table 4.2 I2C Address

MSB							LSB
1	1	0	1	0	0	0	R/W

4.4.4 Reg 0: Status Register

This register indicates the current status of the USB375x.

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
OVLO Status	0	rd	0	Over Voltage Lockout Comparator Status. Set to 0b when VBUS goes above the OVLO threshold.
OVLO Latch	1	rd	0	Set to 1b when an unmasked OVLO interrupt occurs on OVLO Status. Auto cleared when this register is read.
OVP SwitchStatus	2	rd	0	Indicates the status of the OVP switch. A 0b indicates the OVP switch is closed. A 1b indicates that the OVP switch is open.
CurrentLimitStatus	3	rd	0	Indicates the status of the 100mA Current Limit. A 1b indicates that the current limit is enabled.
ChrgDetComplete	4	rd	0	A 1b Indicates Charger Detection has completed.
ChargerType	7:5	rd	000	This register indicates the result of the automatic charger detection. 000 = ChargerDetection is not complete 001 = DCP 010 = CDP 011 = SDP 100 = SE1 Low Current Charger 101 = SE1 High Current Charger If *EnhancedChrgDet = 0* the USB375x is unable to distinguish between a DCP and a CDP and will return DCP as the *ChargerType*.

4.4.5 Reg 1: Configuration Register

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
EnableOVP Switch	0	r/w	0	The OVP switch will be enabled when this bit is set to 1b.
EnableCurrentLimit	1	r/w	0	Controls the 100mA current limit block. The 100mA current limit will be enabled when this bit is set to 1b and the OverrideCurrentLimit bit is also set to 1b.
OverideVBUS	2	r/w	0	When this bit is set to 1b the OVP switch is controlled by the *EnableOVP Switch* bit.
OverrideCurrentLimit	3	r/w	0	When this bit is set to 1b the current limit is controlled by the *EnableCurrentLimit* bit.
Reserved	4	r/w	0	Reserved
EnableMux1	5	r/w	1	When this bit is set to 1b the Mux 1 path is enabled (USB3750 Only)
EnableMux2	6	r/w	0	When this bit is set to 1b the Mux 2 path is enabled (USB3750 Only)
SoftPOR	7	r/w	0	Hardware reset. When this bit is set to 1b, the USB375x will reset and restart the POR sequence. This bit will autoclear in T_{SOFT_POR}. The USB375x registers should not be accessed until the T_{SOFT_POR} time has expired.

4.4.6 Reg 2: Battery Charger Register

These bits allow I2C control of the battery charger circuits. This will allow for custom defined charger detection algorithm to be implemented. By default the I2C control bit is off and this register is under control of the charger detection state machine. Once the charger detection state machine is complete the I2C master can set the *I^2C Control* register to control the charger detection circuits.

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
SeRxEn	0	r/w	0	Single Ended Receiver Enable. Wen this bit is set to 1b the single ended receivers will be enabled
ContactDetectEn	1	r/w	0	Contact Detect Current Source Enable. When this bit is set to 1b the I_{DP_SRC} current source shown in Figure 4.3 will be enabled.
VdatSrcEn	2	r/w	0	Vdat voltage source enable. When this bit is set to 1b the V_{datSrc} voltage source shown in Figure 4.3 will be enabled.
HostChrgEn	3	r/w	0	When this bit is set to 1b, the charger detection connections of DP and DM are swapped. The USB signal path is not reversed. This is required when differentiating between a Charging Downstream Port (CDP) and a Dedicated Charging Port (DCP).

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
IdatSinkEn	4	r/w	0	Idat current sink enable. When this bit is set to 1b the $I_{DATSINKEN}$ current source shown in Figure 4.3 will be enabled.
DpPulldownEn	5	r/w	0	DP 15K pull down resistor enable. When this bit is set to 1b the R_{PD} 15K pull down resistor on DP shown in Figure 4.3 will be enabled.
DmPulldownEn	6	r/w	0	DM 15K pull down resistor enable. When this bit is set to 1b the R_{PD} 15K pull down resistor on DM shown in Figure 4.3 will be enabled.
I^2C Control	7	r/w	0	When this bit is set to 0b the bits [6:0] are disconnected from the Battery Charger circuits. When this bit is set to 1b, bits [6:0] will control the charger detection circuits.

4.4.7 Reg 3: Battery Charger Status Register

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
VdatDet	0	rd	0	Indicates Vdat Det comparator output. A 1b indicates that the VdatDet comparator shown in Figure 4.3 has been tripped.
DpSeRx	1	rd	0	DP Single Ended Receiver Status. A 1b indicates that the DP signal is above the V_{SE_RX} threshold.
DmSeRx	2	rd	0	DM Single Ended Receiver Status. A 1b indicates that the DM signal is above the V_{SE_RX} threshold.
RxHiCurrent	3	rd	0	DM high current SE1 charger output. A 1b indicates that the DM signal is above the V_{SE_RXH} threshold.
Reserved	7:4	r	0000	Read Only.

Chapter 5 Application Notes

5.1 Application Diagram

Table 5.1 Component Values in Application Diagrams

REFERENCE DESIGNATOR	VALUE	DESCRIPTION	NOTES
R_{PU}	10 kΩ	Pull-up required for I2C and INT_B operation.	Pull up to I2C and INT_B power domain on SOC.
C_{VBUS}	1µF to 10µF	Capacitor to ground required by the USB Specification. SMSC recommends <1Ω ESR.	Place near the USB connector.
C_{SYS}	System dependent	System bulk capacitance	Optional. Not required for USB375x operation.

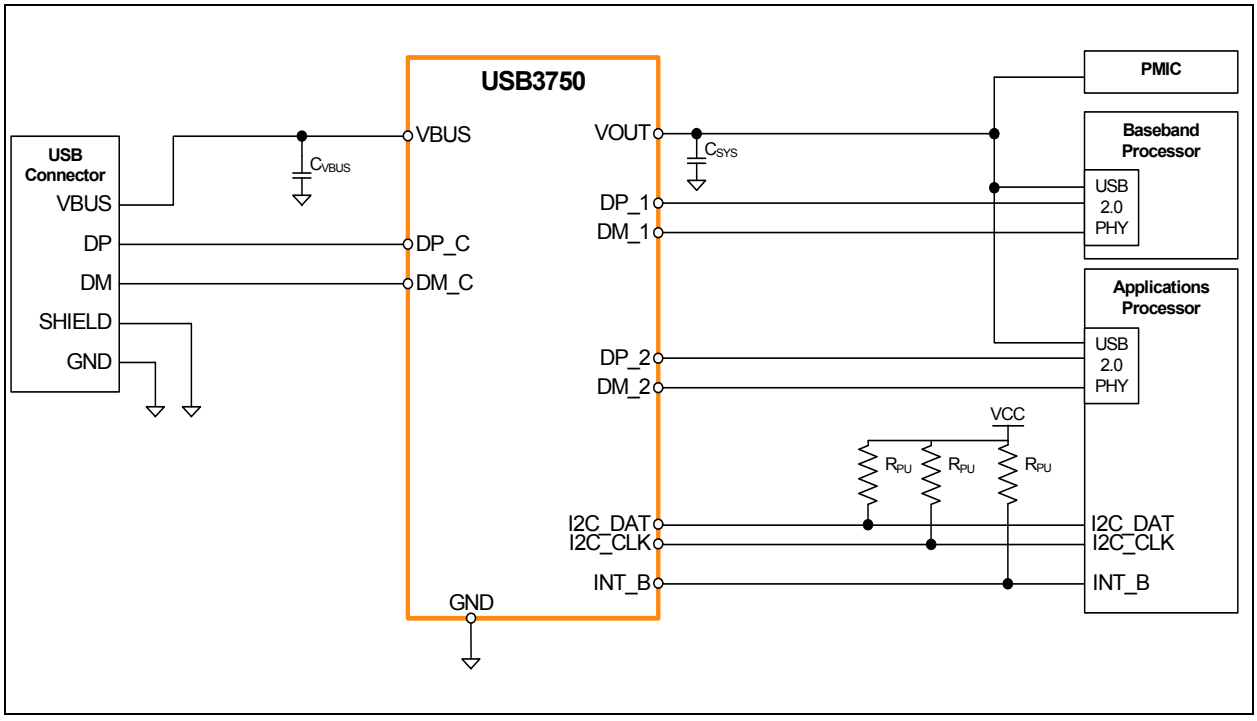


Figure 5.1 USB3750 Device Application Diagram

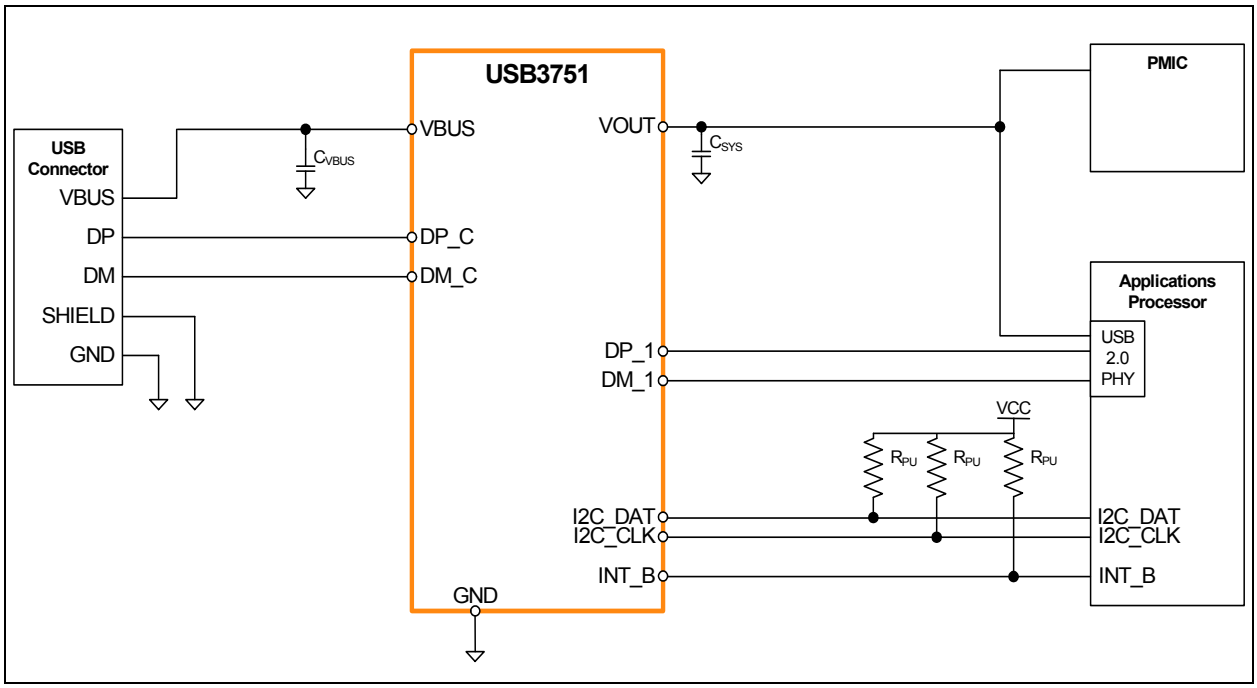


Figure 5.2 USB3751 Device Application Diagram

5.2 ESD Performance

The USB375x is protected from ESD strikes. By eliminating the requirement for external ESD protection devices, board space is conserved, and the board manufacturer is enabled to reduce cost. The advanced ESD structures integrated into the USB375x protect the device whether or not it is powered up.

5.2.1 Human Body Model (HBM) Performance

HBM testing verifies the ability to withstand the ESD strikes like those that occur during handling and manufacturing, and is done without power applied to the IC. To pass the test, the device must have no change in operation or performance due to the event. The USB375x HBM performance is detailed in Table 3.1.

5.2.2 EN/IEC 61000-4-2 Performance

The EN/IEC 61000-4-2 ESD specification is an international standard that addresses system-level immunity to ESD strikes while the end equipment is operational. In contrast, the HBM ESD tests are performed at the device level with the device powered down.

SMSC contracts with Independent laboratories to test the USB375x to EN/IEC 61000-4-2 in a working system. Reports are available upon request. Please contact your SMSC representative, and request information on 3rd party ESD test results. The reports show that systems designed with the USB375x can safely provide the ESD performance shown in Table 3.1 without additional board level protection.

In addition to defining the ESD tests, EN/IEC 61000-4-2 also categorizes the impact to equipment operation when the strike occurs (ESD Result Classification). The USB375x maintains an ESD Result Classification 1 or 2 when subjected to an EN/IEC 61000-4-2 (level 4) ESD strike.

Both air discharge and contact discharge test techniques for applying stress conditions are defined by the EN/IEC 61000-4-2 ESD document.

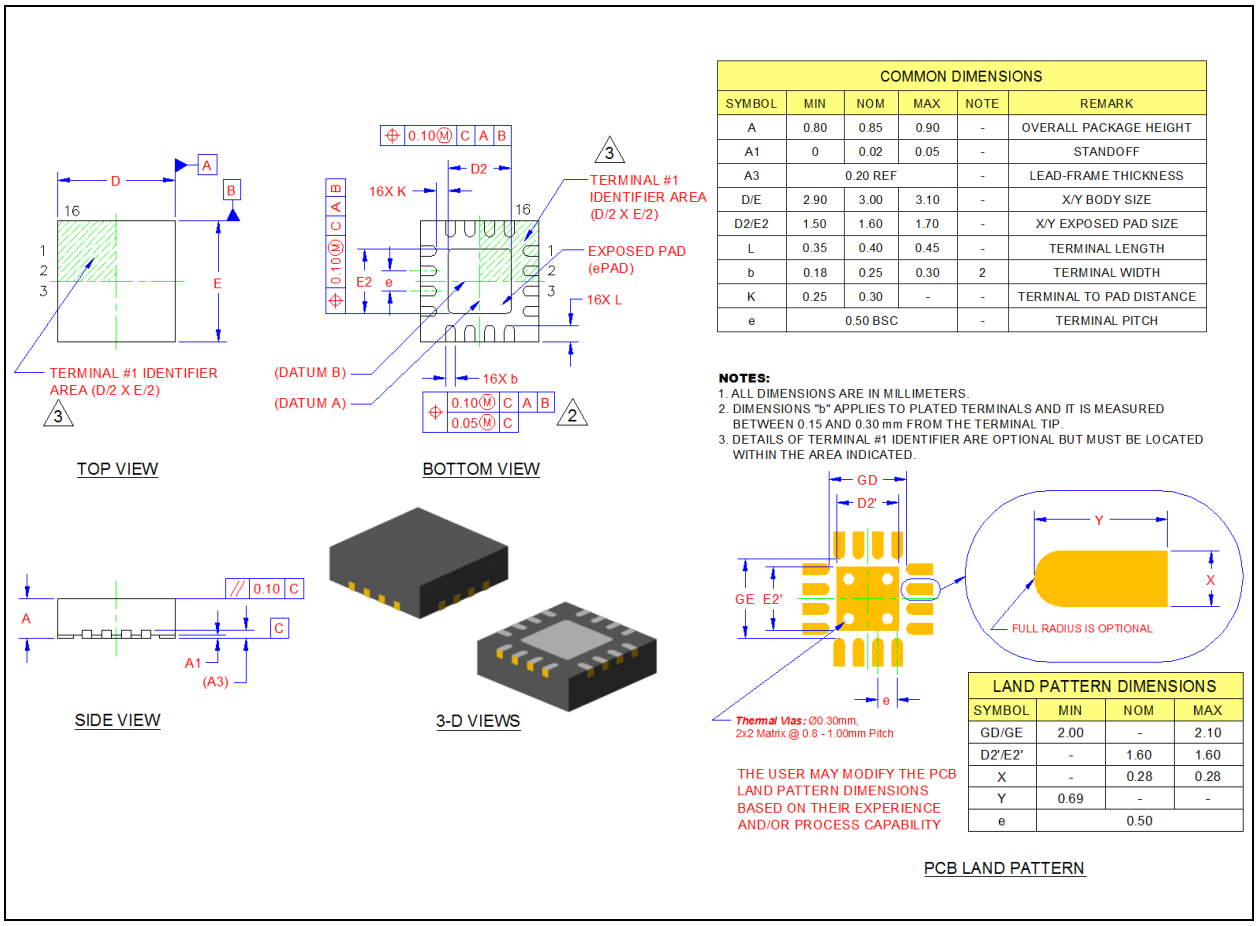
5.2.2.1 Air Discharge

To perform this test, a charged electrode is moved close to the system being tested until a spark is generated. This test is difficult to reproduce because the discharge is influenced by such factors as humidity, the speed of approach of the electrode, and construction of the test equipment.

5.2.2.2 Contact Discharge

The uncharged electrode first contacts the USB connector to prepare this test, and then the probe tip is energized. This yields more repeatable results, and is the preferred test method. The independent test laboratories contracted by SMSC provide test results for both types of discharge methods.

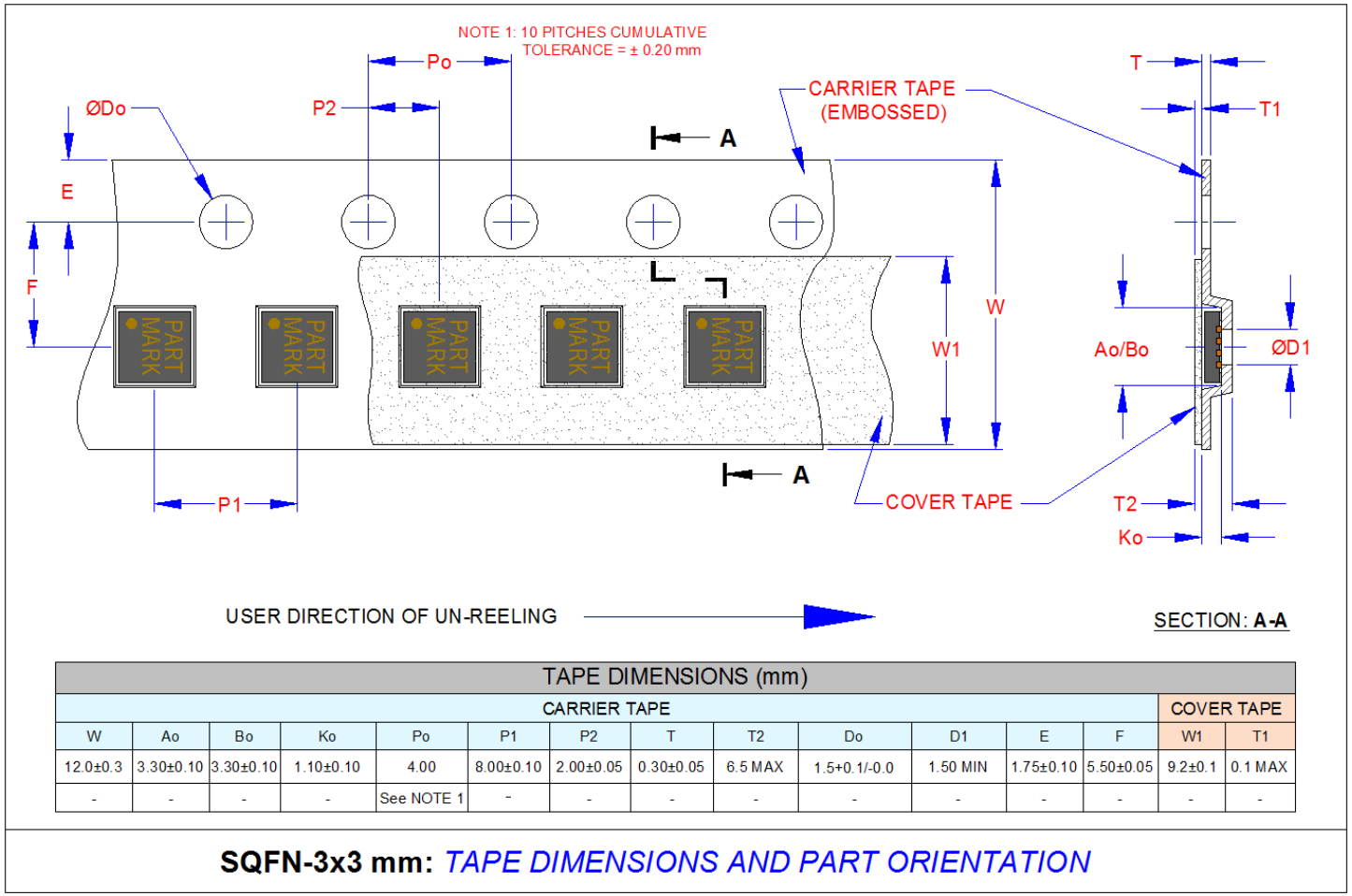
Chapter 6 Package Outline, Tape & Reel Drawings, Package Marking



COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.80	0.85	0.90	-	OVERALL PACKAGE HEIGHT
A1	0	0.02	0.05	-	STANDOFF
A3		0.20 REF		-	LEAD-FRAME THICKNESS
D/E	2.90	3.00	3.10	-	X/Y BODY SIZE
D2/E2	1.50	1.60	1.70	-	X/Y EXPOSED PAD SIZE
L	0.35	0.40	0.45	-	TERMINAL LENGTH
b	0.18	0.25	0.30	2	TERMINAL WIDTH
K	0.25	0.30	-	-	TERMINAL TO PAD DISTANCE
e		0.50 BSC		-	TERMINAL PITCH

LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	2.00	-	2.10
D2'/E2'	-	1.60	1.60
X	-	0.28	0.28
Y	0.69	-	-
e		0.50	

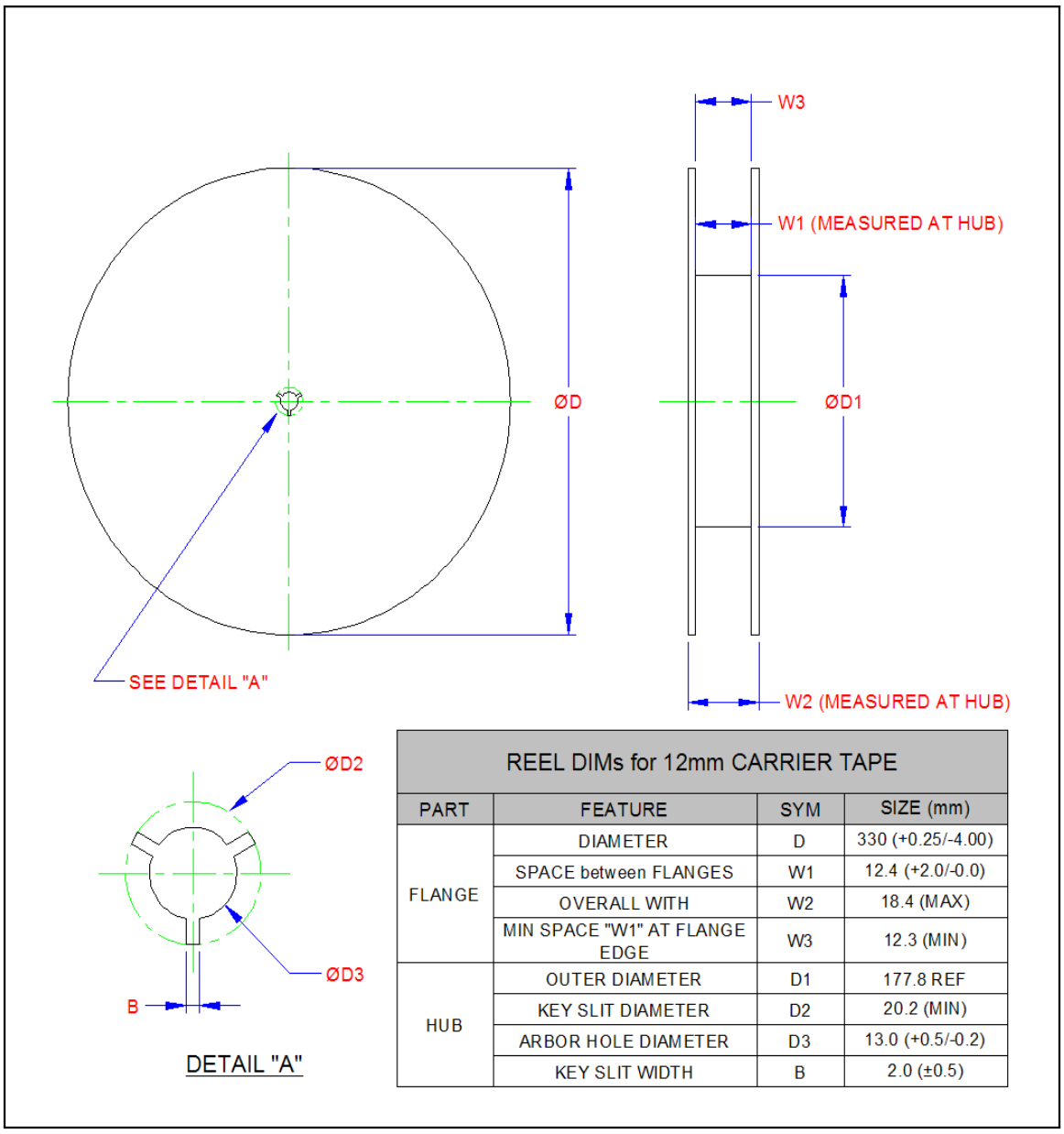
Figure 6.1 16-Pin Lead-free QFN Package Outline



TAPE DIMENSIONS (mm)														
CARRIER TAPE													COVER TAPE	
W	Ao	Bo	Ko	Po	P1	P2	T	T2	Do	D1	E	F	W1	T1
12.0±0.3	3.30±0.10	3.30±0.10	1.10±0.10	4.00	8.00±0.10	2.00±0.05	0.30±0.05	6.5 MAX	1.5+0.1/-0.0	1.50 MIN	1.75±0.10	5.50±0.05	9.2±0.1	0.1 MAX
-	-	-	-	See NOTE 1	-	-	-	-	-	-	-	-	-	-

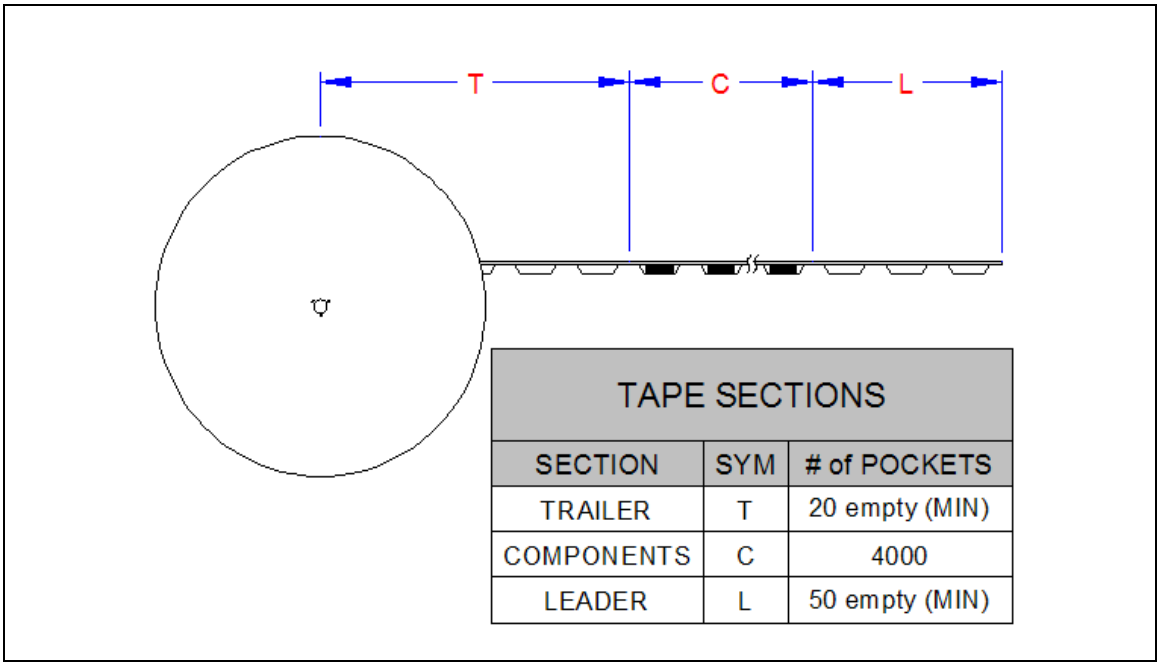
SQFN-3x3 mm: *TAPE DIMENSIONS AND PART ORIENTATION*

Figure 6.2 Tape and Reel Information



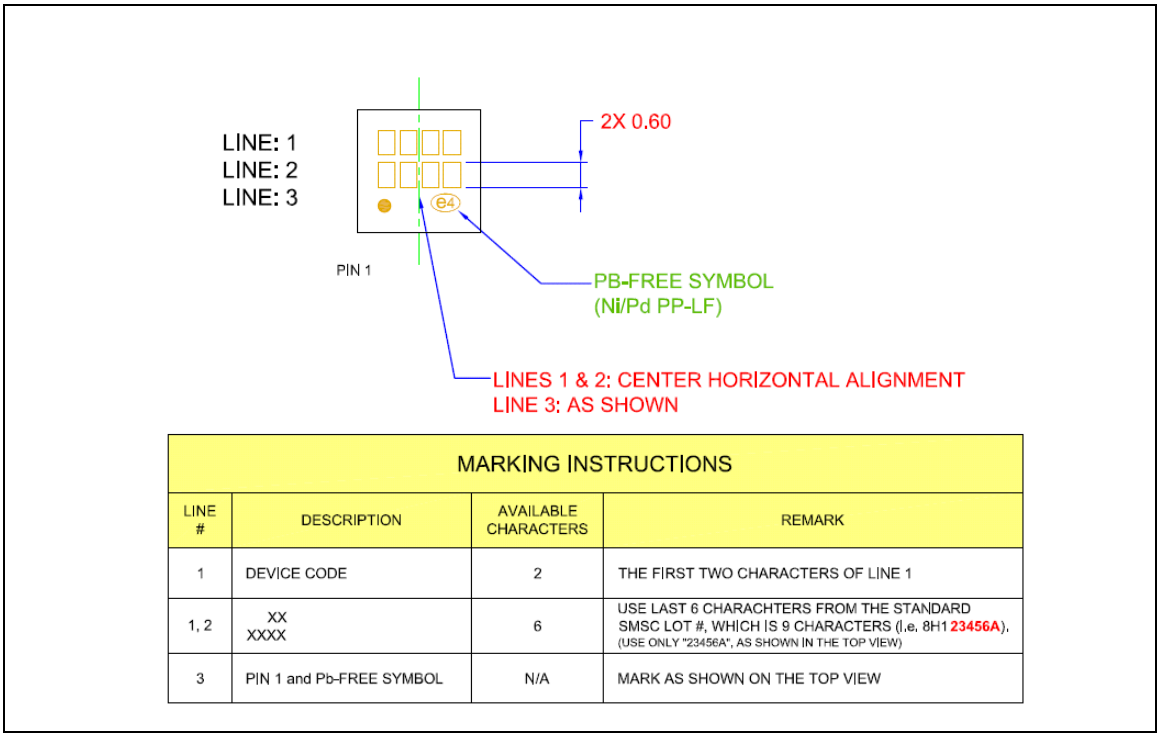
REEL DIMs for 12mm CARRIER TAPE			
PART	FEATURE	SYM	SIZE (mm)
FLANGE	DIAMETER	D	330 (+0.25/-4.00)
	SPACE between FLANGES	W1	12.4 (+2.0/-0.0)
	OVERALL WITH	W2	18.4 (MAX)
	MIN SPACE "W1" AT FLANGE EDGE	W3	12.3 (MIN)
HUB	OUTER DIAMETER	D1	177.8 REF
	KEY SLIT DIAMETER	D2	20.2 (MIN)
	ARBOR HOLE DIAMETER	D3	13.0 (+0.5/-0.2)
	KEY SLIT WIDTH	B	2.0 (±0.5)

Figure 6.3 Reel Dimensions



TAPE SECTIONS		
SECTION	SYM	# of POCKETS
TRAILER	T	20 empty (MIN)
COMPONENTS	C	4000
LEADER	L	50 empty (MIN)

Figure 6.4 Tape Sections



MARKING INSTRUCTIONS			
LINE #	DESCRIPTION	AVAILABLE CHARACTERS	REMARK
1	DEVICE CODE	2	THE FIRST TWO CHARACTERS OF LINE 1
1, 2	XX XXXX	6	USE LAST 6 CHARACHTERS FROM THE STANDARD SMSC LOT #, WHICH IS 9 CHARACTERS (I.e. 8H1 **23456A**). (USE ONLY "23456A", AS SHOWN IN THE TOP VIEW)
3	PIN 1 and Pb-FREE SYMBOL	N/A	MARK AS SHOWN ON THE TOP VIEW

Figure 6.5 Package Marking

Datasheet Revision History

Table 6.1 Customer Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.1 (02-12-13)	All	Misc. typos, etc.
	Section 4.4.1, "I2C Interface," on page 24	Added additional paragraph: “The USB375x-1 requires I2C communications in order for the default USB path to be enabled. By default, the 100mA current limit is enabled. Only devices that draw <100mA will be enabled through the path as part of dead battery provision support. In order to bypass this limit, bits 0 (EnableOVP Switch) and 2 (OverideVBUS) in Register 1 (Configuration Register) need to be set via I2C.”
Rev. 1.0 (09-02-11)	Initial Release	