3.3V 28Mbps-2.7Gbps AnyRate® CLOCK AND DATA RECOVERY WITH INTEGRATED CLOCK MULTIPLIER UNIT

SY87721L

FEATURES

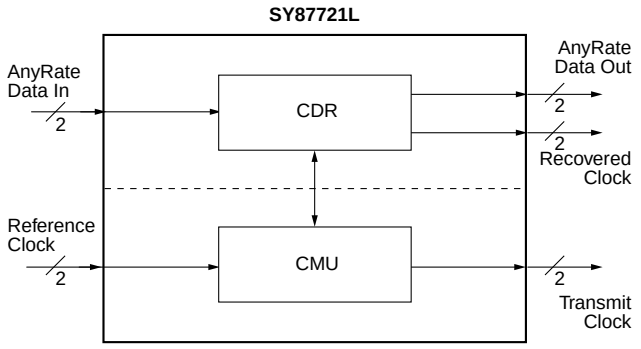
- **Recovers any data and clock from 28Mbps to 2.7Gbps**
  - **OC-1, OC-3, OC-12, OC-48, ATM**
  - **Gigabit Ethernet, Fast Ethernet**
  - **Fibre Channel, 2x Fibre Channel**
  - **P1394, Infiniband**
  - **SMPTE-259, SMPTE-292**
  - **Proprietary optical transport**
- **Integrated clock multiplier unit with low jitter generation**
- **Complies with Bellcore, ITU/CCITT and ANSI specifications**
- **Selectable mux for pass through; avoids jitter accumulation when switching through backplanes**
- **Available in 64-Pin EPAD-TQFP package**

DESCRIPTION

The SY87721L is a complete Clock Recovery and Data retiming integrated circuit for data rates from 28Mbps up to 2.7Gbps NRZ including SONET FEC data rates. Included in the device, is a fully integrated Clock Multiplier Unit (CMU) that is capable of generating frequencies that cover the same data rate range as the CDR. The device is ideally suited for SONET/SDH/ATM, Fibre Channel, and Gigabit Ethernet applications, as well as other high-speed data transmission applications.

Clock recovery and data retiming is performed by synchronizing the on-chip VCO directly to the incoming data stream. The VCO center frequency is controlled by the reference clock frequency and the selected divide ratio. On-chip clock generation is performed through the use of a frequency multiplier PLL with a byte rate or code group rate source as reference.

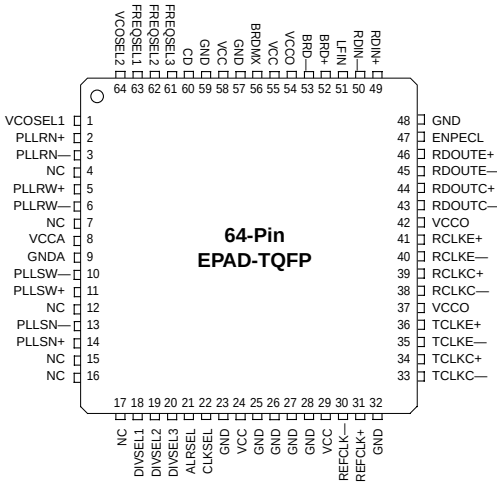
SIMPLIFIED BLOCK DIAGRAM



APPLICATIONS

- **SONET/SDH/ATM-based transmission systems, modules, and test equipment**
- **Transponders and section repeaters**
- **Multiplexers: access, add drop (ADM), and terminal (TM)**
- **Terabit routers and broadband cross-connects**
- **Fiber optic test equipment**

PACKAGE/ORDERING INFORMATION



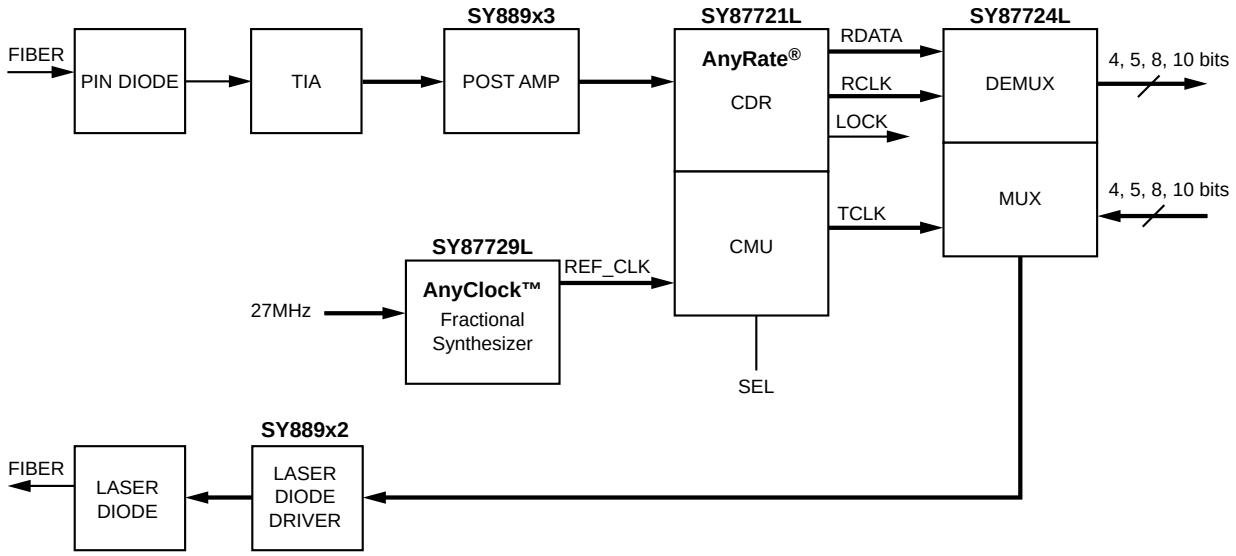
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY87721LHI	H64-1	Industrial	SY87721LHI	Sn-Pb
SY87721LHITR[2]	H64-1	Industrial	SY87721LHI	Sn-Pb
SY87721LHG[3]	H64-1	Industrial	SY87721LHG with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY87721LHG[2, 3]	H64-1	Industrial	SY87721LHG with Pb-Free bar-line indicator	Pb-Free NiPdAu

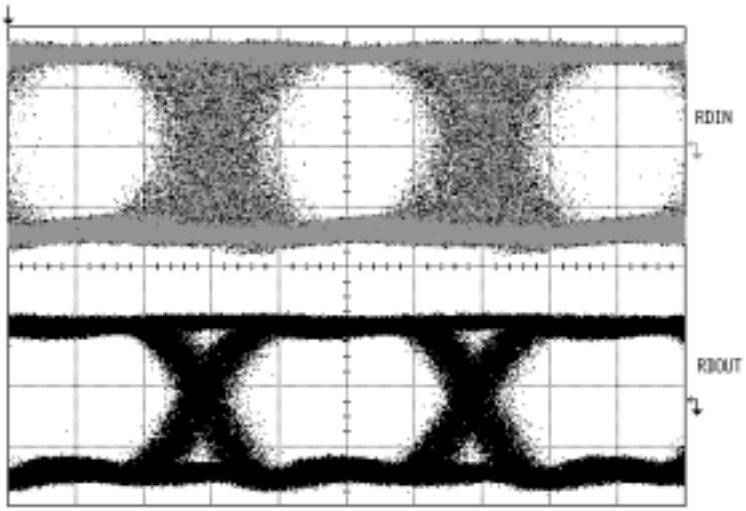
Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electricals only.
2. Tape and Reel.
3. Recommended for new designs.

SYSTEM BLOCK DIAGRAM

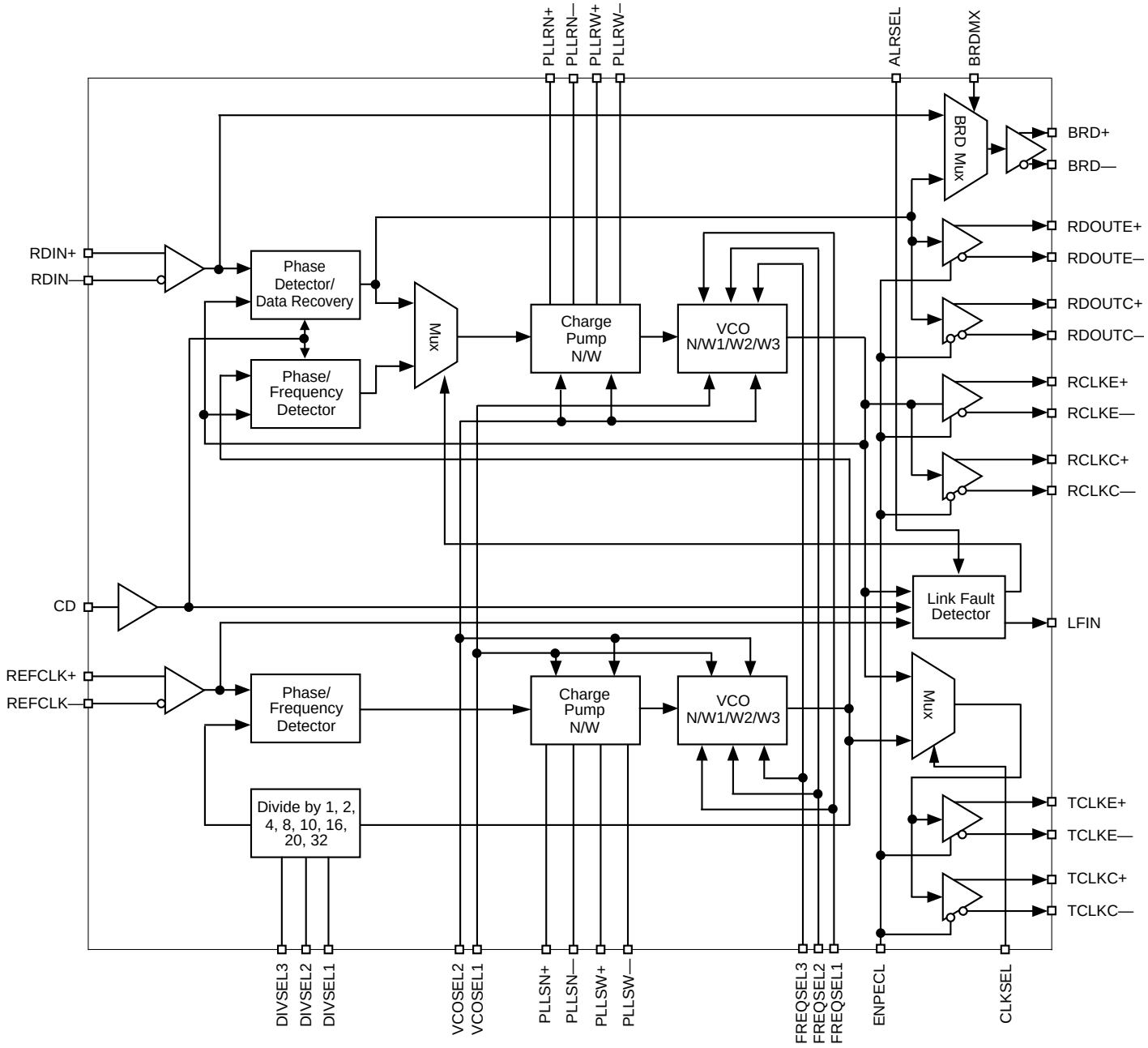


OC-48 EYE DIAGRAM



Time (100ps/div)

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

INPUTS

BRDMX [BRD Mux] – PECL Input

This signal indicates what data appears at the BRD± output. When logic HIGH, BRD± is a direct copy of what appears at RDOUTC±. When logic low, BRD± is a copy of what appears at RDIN±. Unlike RDOUTC±, BRD± conveys valid data even when ENPECL is logic LOW. Please refer to Table 1.

BRDMX (Input)	BRD± (Output)
0	RDIN±
1	RDOUTC±

Table 1. BRDMX Truth Table

RDIN± [Serial Data Input] – Differential PECL Input

This differential input accepts the receive serial data stream. An internal receive PLL recovers the embedded clock (RCLK) and data (RDOUT) information. The incoming data rate can be within one of ten frequency ranges, or can be one of five specific frequencies, depending on the state of the FREQSEL and VCOSEL pins. The RDIN– pin has an internal 75KΩ resistor tied to V_{CC}.

REFCLK± [Reference Clock] – Differential PECL Input

This input is used as the reference for the internal frequency synthesizer and the "training" frequency for the receiver PLL to keep it centered in the absence of data coming in on the RDIN input. The input frequency to REFCLK is limited to 340MHz or less, depending on the setting on the DIVSEL signals. The REFCLK– pin has an internal 75KΩ resistor tied to V_{CC}.

CD [Carrier Detect] – PECL Input

This input controls the recovery function of the Receive PLL and can be driven by the carrier detect output of optical modules or from external transition detection circuitry. When this input is HIGH, the input data stream (RDIN) is recovered normally by the Receive PLL. When this input is LOW, the data on the RDOUT output will be internally forced to a constant LOW, the Link Fault Indicator output LFIN forced LOW, and the clock recovery PLL forced to lock onto the synthesized clock frequency generated from REFCLK.

VCOSEL1, VCOSEL2 [VCO Select] – TTL Inputs

These inputs select the output clock frequency range via either one of three PLLs, or a SONET/SDH specific PLL. Only the selected PLL is enabled. All other PLLs are disabled. Refer to Table 3 for more details.

FREQSEL1, ..., FREQSEL3 [Frequency Select] – TTL Inputs

These inputs select the post divide ratio of the VCO. Refer to Table 3 for more details.

DIVSEL1, ..., DIVSEL3 [Divider Select] – TTL Inputs

These inputs select the ratio between the output clock frequency (RCLK/TCLK) and the REFCLK input frequency as shown in Table 4. Please note that the divide by 32 selection, "011", is only available for use when FREQSEL are set to "000."

DIVSEL1	DIVSEL2	DIVSEL3	REFCLK Multiplier
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	32
1	0	0	8
1	0	1	10
1	1	0	16
1	1	1	20

Table 2(1). Reference Clock Multiplier Truth Table

Note:

1. Some combinations of FREQSEL and DIVSEL result in undefined behavior. Refer to Table 3 for more details.

CLKSEL [Clock Select] – TTL Input

This input is used to select either the recovered clock of the receiver PLL (CLKSEL = HIGH) or the clock of the frequency synthesizer (CLKSEL = LOW) to the TCLK outputs. Do not use for skew matching.

ENPECL [Enable ECL] – TTL Input

This input, when HIGH (ENPECL = 1), enables the differential PECL outputs TCLKE±, RDOUTE±, and RCLKE±. It also disables the CML outputs, by setting TCLKC+, RDOUTC+, and RCLKC+ logic HIGH and setting TCLKC–, RDOUTC–, and RCLKC– logic LOW.

When set LOW (ENPECL = 0), this signal enables the differential CML outputs TCLKC±, RDOUTC±, and RCLKC±. It also disables the PECL outputs by setting TCLKE+, RDOUTE+, and RCLKE+ logic HIGH and setting TCLKE–, RDOUTE– and RCLKE– logic LOW.

ALRSEL [Auto Lock Range Select] – TTL Input

This pin defines the frequency difference, and the frequency difference hysteresis at which 'in-lock' and 'out of lock' conditions are declared. Please refer to the "AC Characteristics" for more details.

OUTPUTS

BRD± [Buffered Recovered Data] – Differential CML Output

The signal is either a buffered RDIN± or RDOUTC±, depending on the state of the BRDMX input. This allows a user to selectively bypass the CDR or not, as warranted by architecture. This CML output has a voltage swing of 400mV loaded.

LFIN [Link Fault Indicate] – O.C. TTL Output

This output indicates the status of the input data stream RDIN. Active HIGH indicates that the internal clock recovery PLL has locked onto the incoming data stream. LFIN will go HIGH if CD is HIGH and RDIN is within the frequency range of the Receive PLL (as per ALRSEL). LFIN is an asynchronous output.

RDOUTE± [Receive Data Out] – Differential PECL Output

These ECL 100K outputs (+3.3V referenced) represent the recovered data from the input data stream (RDIN). It is specified on the rising edge of RCLK.

RDOUTC± [Receive Data Out] – Differential CML Output

This is the CML version of RDOUTE±.

RCLKE± [Receive Clock Out] – Differential PECL Output

These ECL 100K outputs (+3.3V referenced) represent the recovered clock used to sample the recovered data (RDOUT).

RCLKC± [Receive Clock Out] – Differential CML Output

This is the CML version of RCLKE±.

TCLKE± [Transmit Clock Out] – Differential PECL Output

These ECL 100K outputs (+3.3V referenced) represent either the recovered clock (CLKSEL = HIGH) used to sample the recovered data (RDOUT) or the transmit clock of the frequency synthesizer (CLKSEL = LOW).

TCLKC± [Transmit Clock Out] – Differential CML Output

This is the CML version of TCLKE±.

PLLSN+, PLLSN– [Clock Synthesis Loop Filter]

External loop filter pins for the clock synthesis narrow band PLL.

PLLSW+, PLLSW– [Clock Synthesis Loop Filter]

External loop filter pins for the clock synthesis wide band PLL.

PLLRN+, PLLRN– [Clock Recovery Loop Filter]

External loop filter pins for the clock recovery narrow band PLL.

PLLRW+, PLLRW– [Clock Recovery Loop Filter]

External loop filter pins for the clock recovery wide band PLL.

OTHERS

VCC	Supply Voltage
VCCO	Output Supply Voltage
VCCA	Analog Supply Voltage
GND	Ground
GNDA	Analog Ground
NC	These pins are for factory test, and are to be left unconnected during normal use.

DESCRIPTION

General

The SY87721L is a complete clock and data recovery circuit, capable of handling NRZ data rates from 28MHz through to 2.7GHz. A reference PLL is used as a frequency synthesizer, both to multiply a reference clock to the desired transmit rate, and to train the recovery PLL in preparation for actual data recovery.

Link Fault Algorithm

The SY87721L includes a Link Fault Detection circuit. This circuit provides the following functions: Under Loss-of-Lock (LOL) conditions, which can occur when the Carrier Detect (CD) input is active HIGH, the output of the RCLK approximates the output of the TCLK, within a lock range as specified by the state of ALRSEL.

Under Loss-of-Signal (LOS) conditions, enabled by driving the Carrier Detect (CD) input to inactive logic LOW, the output of the RCLK becomes an exact copy of the TCLK output. This is the result of forcing the recovery PLL to lock to the synthesized reference.

Under LOL and LOS conditions, the LFIN output is an inactive logic LOW.

SY87721L follows a prescribed procedure, to acquire and recover the clock of the incoming data stream. This procedure is triggered either by a falling edge on CD, or by the recovered clock PLL indicating a frequency error, compared to the synthesized reference, of greater than 500ppm or 4,500ppm, as selected by ALRSEL. With the CD input set active HIGH, the algorithm begins by phase and frequency training the recovery PLL to the synthesized reference. Once the recovery PLL is within the specified lock range, determined by the state of ALRSEL, the SY87721L will switch from a phase-frequency comparison with the synthesized reference, to a phase-only comparison with the incoming data stream. When the recovery PLL is locked to this incoming data stream (that is, after phase step recovery), then data recovery may proceed and LFIN asserts. Once locked and accepting data, the LFIN signal may de-assert should the data input frequency deviate too far from the synthesized reference frequency.

VCO Selection

SY87721L sports four complete VCO circuits. Depending on the application and the frequency range, any one of these four perform data recovery.

As indicated by the VCO selection table, there are three general purpose VCOs each covering one of three frequency ranges. However, to extend the range of the device, the output of the VCO may be divided down.

In the case of the two highest frequency general purpose VCOs (VCOSEL = 1, 0 or 0,1), this divisor is always set to 1. For the lowest frequency VCO, the FREQSEL pins select which divisor, and hence, which range of frequencies the VCO will work over.

In addition, for SONET/SDH applications, there is a narrow band, extremely low jitter PLL. It also uses the FREQSEL divisor to choose the correct SONET/SDH frequency.

The valid modes of operation are shown in Table 3.

VCOSEL1	VCOSEL2	FREQSEL1	FREQSEL2	FREQSEL3	Range (MHz)
0	0	0	0	0	2488 (OC48)–2700
0	0	0	0	1	1244-1350
0	0	0	1	0	622 (OC12)–675
0	0	1	0	0	311–337
0	0	1	1	0	155 (OC3)–168
0	1	0	0	0	1800–2700
1	0	0	0	0	1250–1800
1	1	0	0	0	650–1300(1)
1	1	0	0	1	325–650(2)
1	1	0	1	0	163–325
1	1	0	1	1	109–216
1	1	1	0	0	82–162
1	1	1	0	1	55–108
1	1	1	1	0	41–81
1	1	1	1	1	28–54

Table 3 (3). Frequency Range Selection Truth Table

Notes:

1. REFCLK multiplier of 1 or 2 is not allowed in this range.
2. REFCLK multiplier of 1 is not allowed in this range.
3. Combinations of VCOSEL and FREQSEL other then those in this table result in undefined behavior, and should not be used.

LOOP FILTER COMPONENTS

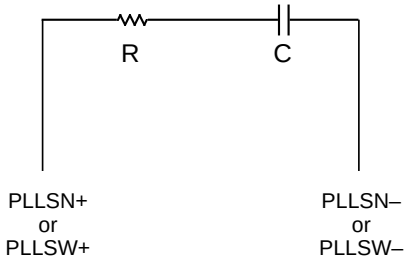


Figure 1. Narrow Band and Wide Band Synthesizer Loop Filter

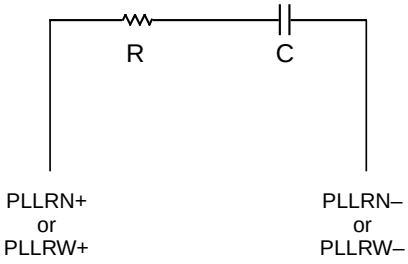


Figure 2. Narrow Band and Wide Band CDR Loop Filter

PLL	R	C
PLLSN+, PLLSN–	1.2kΩ	1µF
PLLRN+, PLLRN–	390Ω	1µF
PLLSW+, PLLSW–	845Ω	1µF
PLLRW+, PLLRW–	455Ω	1µF

Table 4. Synthesizer and Clock Recovery Loop Filter Values

CML OUTPUT DIAGRAM(1)

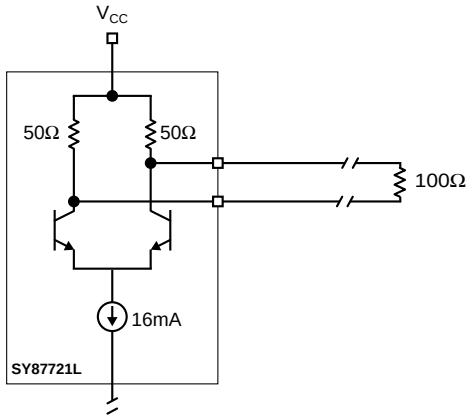
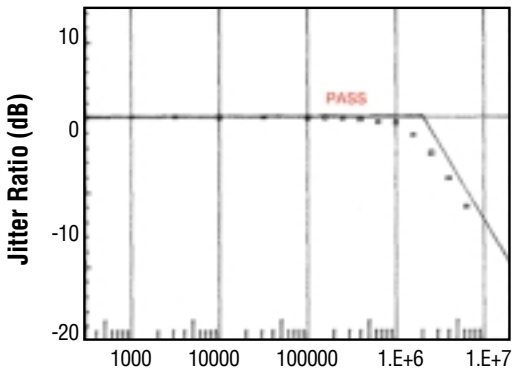


Figure 3. 50Ω Load CML Output

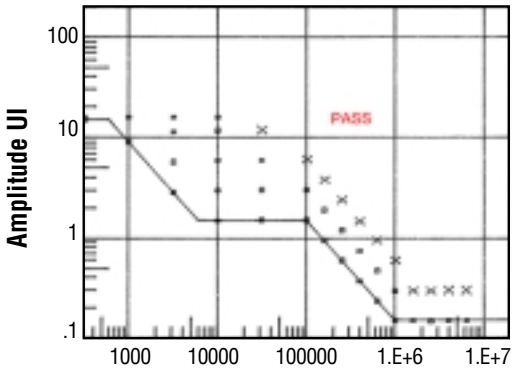
NOTE:

1. V_{OSW} is defined as $|V_{OH}–V_{OL}|$ on any one pin (either the true or the complement pin). As opposed to the single-ended swing, differential swing, V_{OSW} (true pin) + V_{OSW} (complement pin) is double the V_{OSW} value.

OC-48 JITTER TRANSFER AND TOLERANCE



OC-48 Jitter Transfer



OC-48 Jitter Tolerance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter		Rating	Unit
V_{CC}	Power Supply Voltage		–0.5 to +5.0	V
V_{IN}	Input Voltage		–0.5 to V_{CC}	V
I_{OUT}	ECL Output Current	– Continuous – Surge	50 100	mA
I_{CMLOUT}	CML Output Current		30	mA
	Lead Temperature (soldering, 20 sec.)		+260	°C
T_{store}	Storage Temperature Range		–65 to +150	°C
T_A	Operating Temperature Range		–40 to +85	°C
θ_{JA}	Package Thermal Resistance[2] (Junction-to-Ambient)	– 0lfpm – 200lfpm – 500lfpm	22.3 17.2 15.1	°C/W °C/W °C/W

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Jedec standard test boards with die attach pad soldered to pcb. Tested at 1W.

DC ELECTRICAL CHARACTERISTICS

V_{CC} =V_{CCO} = V_{CCA} = 3.3V ±5%; GND = GNDA = 0V; T_A = –40°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{CC}	Power Supply Voltage	3.15	3.3	3.45	V	
I_{CC}	Power Supply Current	—	360	450	mA	

100K PECL DC ELECTRICAL CHARACTERISTICS

V_{CC} =V_{CCO} = V_{CCA} = 3.3V ±5%; GND = GNDA = 0V; T_A = –40°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IH}	Input HIGH Voltage	V_{CC} – 1.165	—	V_{CC} – 0.880	V	
V_{IL}	Input LOW Voltage	V_{CC} – 1.810	—	V_{CC} – 1.475	V	
I_{IL}	Input LOW Current	–0.5	—	—	µA	V_{IN} = V_{IL}(Min)
V_{OH}	Output HIGH Voltage	V_{CC} – 1.075	—	V_{CC} – 0.830	V	50Ω to V_{CC} –2V
V_{OL}	Output LOW Voltage	V_{CC} – 1.860	—	V_{CC} – 1.570	V	50Ω to V_{CC} –2V

Note:

1. All PECL inputs have an internal 75kΩ resistor to V_{EE}. In addition, the complement inputs of all differential PECL inputs have a 75kΩ resistor to V_{CC}. Thus, unconnected PECL inputs behave like static logic LOW.

CML DC ELECTRICAL CHARACTERISTICS

V_{CC} =V_{CCO} = V_{CCA} = 3.3V ±5%; GND = GNDA = 0V; T_A = –40°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	V_{CC} – 0.050	—	V_{CC}	V	No Load
V_{OL}	Output LOW Voltage	—	—	V_{CC} – 0.65	V	No Load
V_{OSW}	Output Voltage Swing	—	0.4	—	V	50Ω to V_{CC}

Note:

1. V_{OSW} is defined as $|V_{OH}–V_{OL}|$ on any one pin (either the true or the complement pin). As opposed to the single-ended swing, differential swing, V_{OSW} (true pin) + V_{OSW} (complement pin) is double the V_{OSW} value.

TTL DC ELECTRICAL CHARACTERISTICS

V_{CC} =V_{CCO} = V_{CCA} = 3.3V ±5%; GND = GNDA = 0V; T_A = –40°C to +85°C

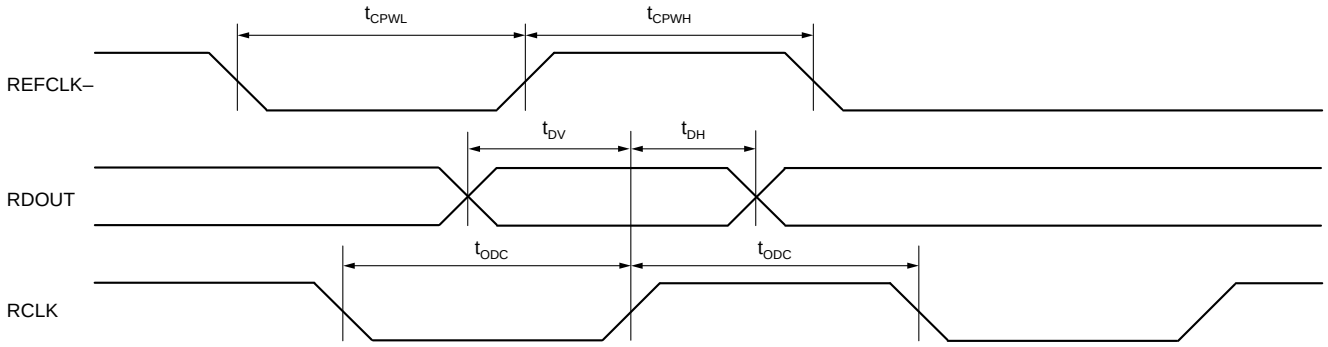
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0	—	—	V	
V_{IL}	Input LOW Voltage	—	—	0.8	V	
I_{IH}	Input HIGH Current	— —	— —	+20 +100	µA µA	V_{IN} = 2.7V, V_{CC} = 3.45V V_{IN} = V_{CC}, V_{CC} = 3.45V
I_{IL}	Input LOW Current	–300	—	—	µA	V_{IN} = 0.5V, V_{CC} = Max.
I_{OLK}	Output Leakage Current	—	—	500	µA	V_{OUT} = V_{CC}
V_{OL}	Output LOW Voltage	—	—	0.5	V	I_{OL} = 4mA

AC ELECTRICAL CHARACTERISTICS

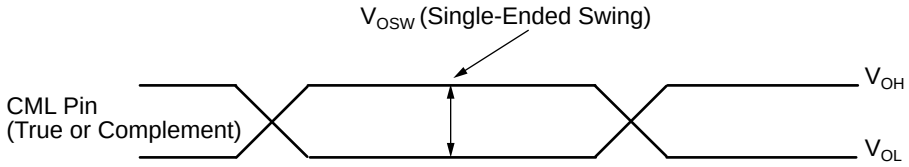
V_{CC} =V_{CCO} = V_{CCA} = 3.3V ±5%; GND = GNDA = 0V; T_A = –40°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
	TCLK Output Jitter	—	—	0.01	UI rms	REFCLK Multiplier ≤16 VCOSEL = 0, 0
	Frequency Difference, LFIN shows Out of Lock	500	1500	—	ppm	ALRSEL High
	Frequency Difference, LFIN shows Out of Lock	4500	6500	—	ppm	ALRSEL Low
	RDIN Maximum Data Rate	2.7	—	—	Gbps	
	REFCLK Maximum Frequency	—	—	340	MHz	
t_{CPWH}	REFCLK Pulse Width High	1.2	—	—	ns	
t_{CPWL}	REFCLK Pulse Width Low	1.2	—	—	ns	
t_{IRF}	REFCLK Input Rise/Fall Time (20% to 80%)	—	—	1.0	ns	
t_{ODC}	Output Duty Cycle (RCLK/TCLK)	45	—	55	% of UI	
t_{RE} t_{FE}	ECL Output Rise/Fall Time (20% to 80%)	—	—	600	ps	50Ω to V_{CC}–2V
t_{RC} t_{FC}	CML Output Rise/Fall Time (20% to 80%)	—	—	120	ps	50Ω Load
t_{DV}	Data Valid	100	—	—	ps	
t_{DH}	Data Hold	100	—	—	ps	

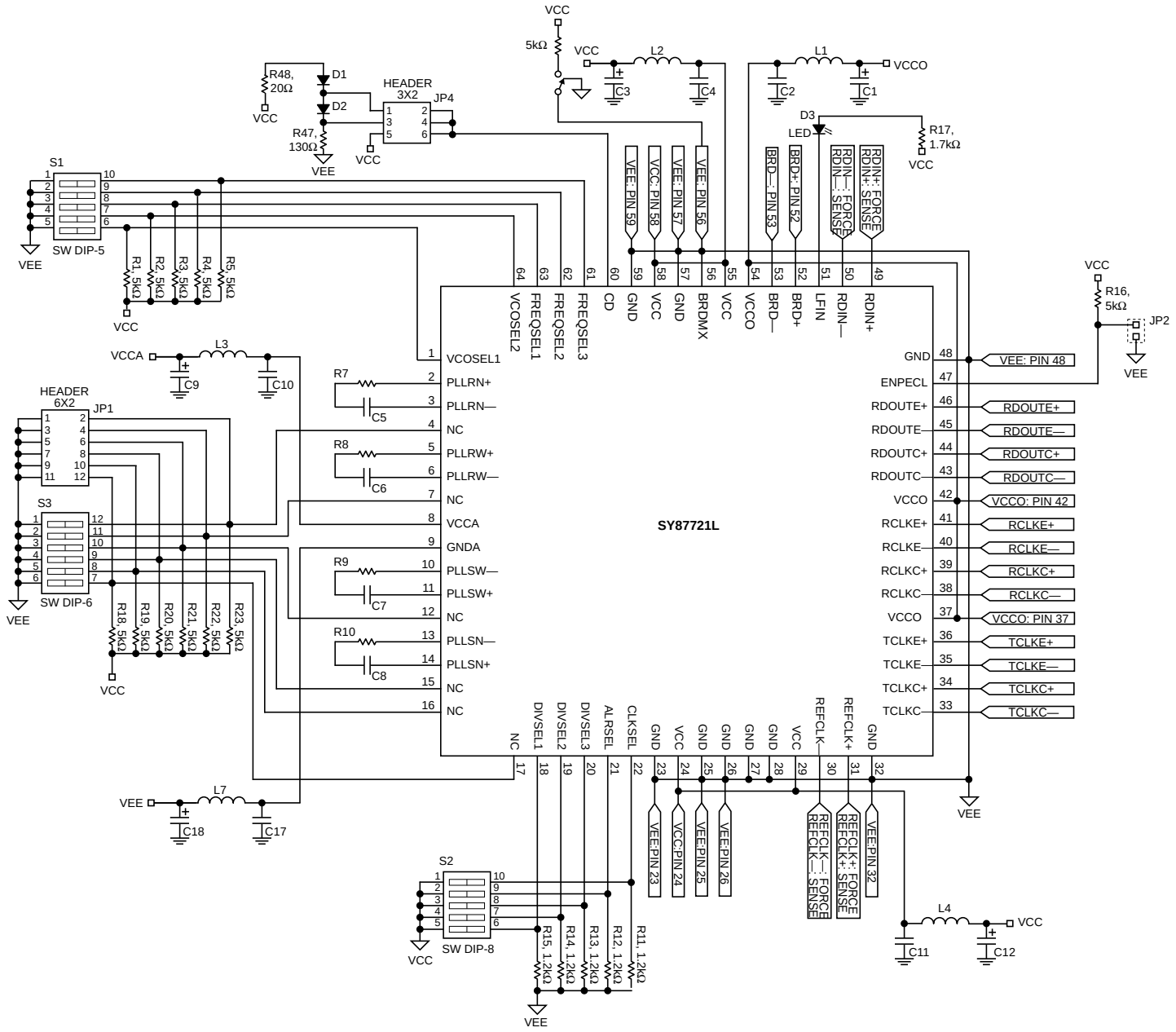
TIMING WAVEFORMS



CML V_{OSW} DIAGRAM



EVALUATION BOARD SCHEMATIC

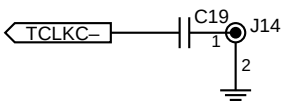


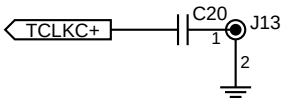
Notes:

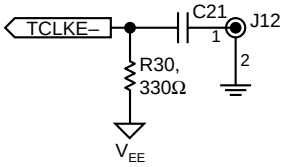
1. C11, C17, C10, C4, C2 = 0.1µF
2. C18, C12, C9, C3, C1 = 1µF
3. C2, C4, C10, C11, and C17 need to be located right at device pin. If vias to power GND used—use overlapping multiple vias to lower inductance.

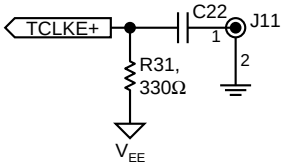
EVALUATION BOARD I/O TERMINATION SCHEMES

TCLK OUTPUTS

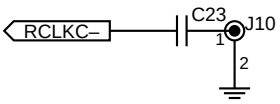


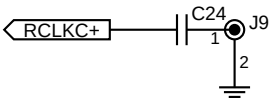


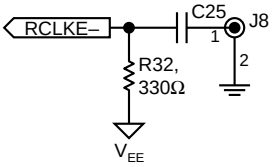


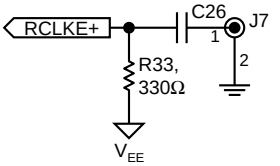


RCLK OUTPUTS

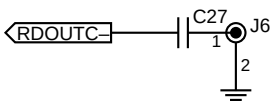


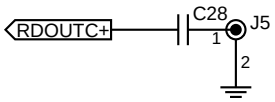


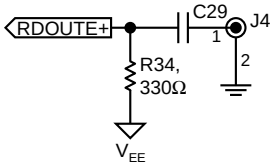


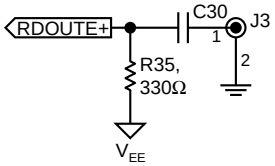


RDOUT OUTPUTS

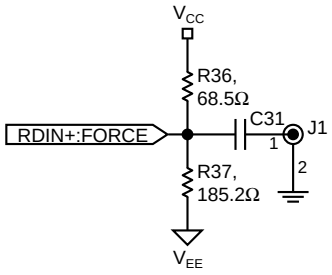


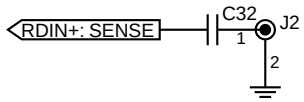


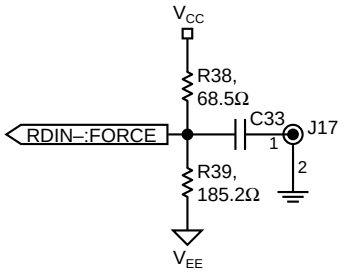


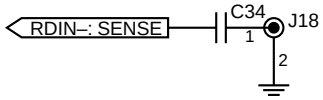


RDIN INPUTS





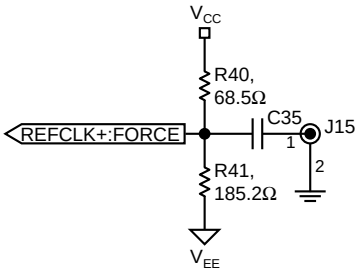


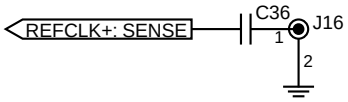


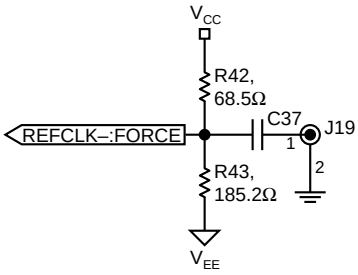
Notes:

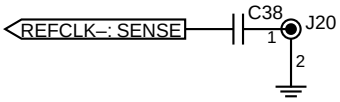
1. For AC coupling, include capacitors C19 thru C31, C33, C35 and C37.
2. If DC coupling, remove resistors R36 thru R43.

REFCLK INPUTS

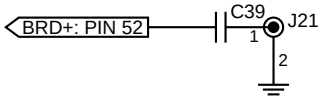


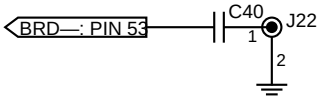


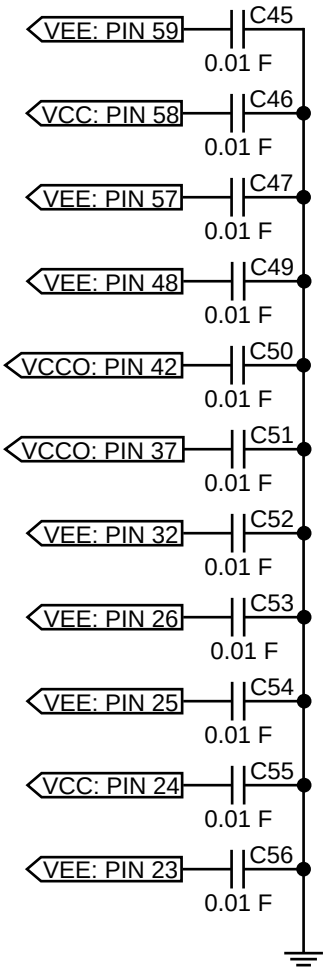




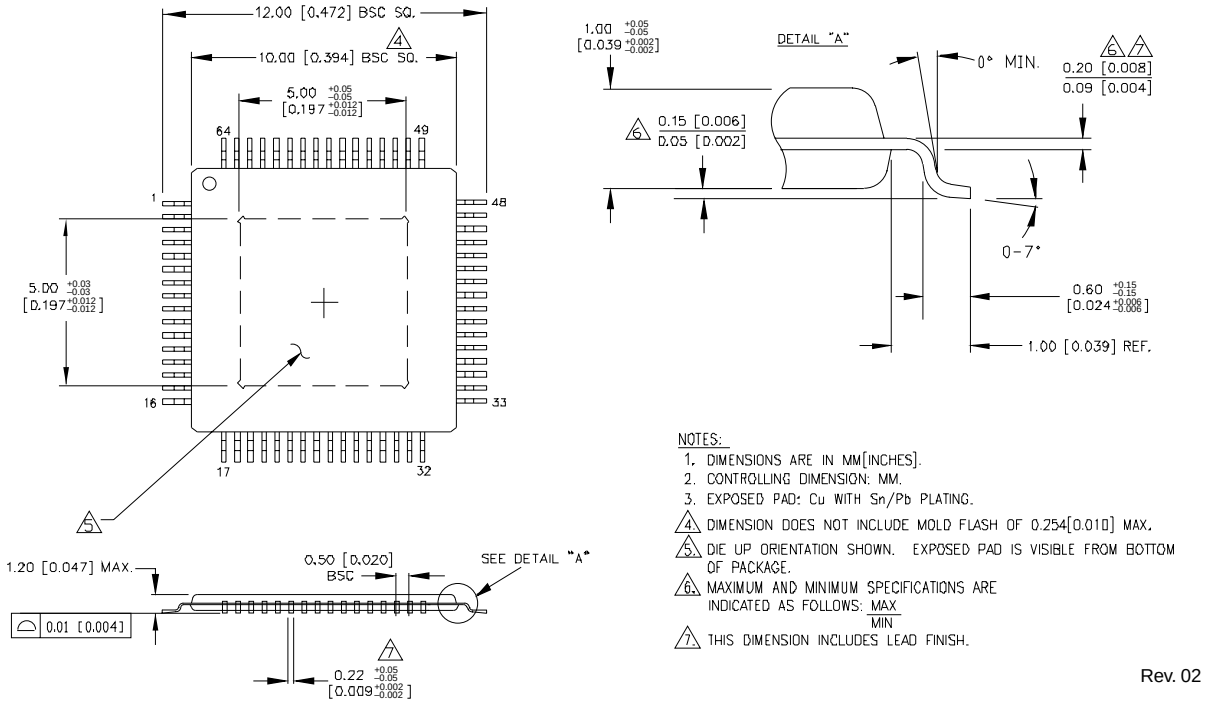
BRD OUTPUTS





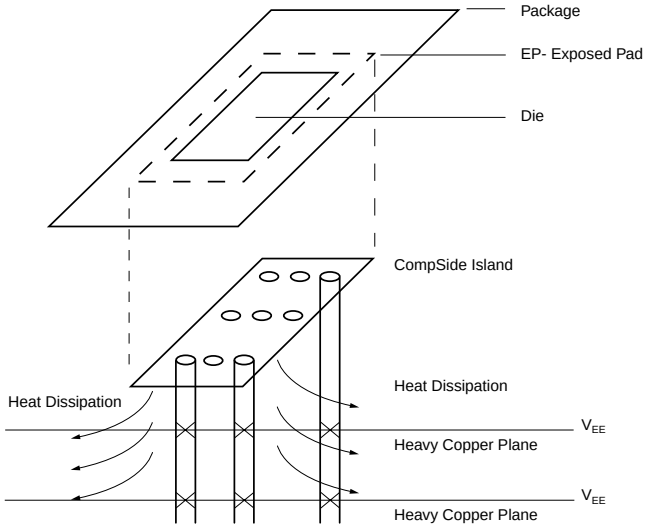


64 LEAD EPAD-TQFP (DIE UP) (H64-1)



NOTES:
1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. EXPOSED PAD: Cu WITH Sn/Pb PLATING.
4. DIMENSION DOES NOT INCLUDE MOLD FLASH OF 0.254[0.010] MAX.
5. DIE UP ORIENTATION SHOWN. EXPOSED PAD IS VISIBLE FROM BOTTOM OF PACKAGE.
6. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX / MIN
7. THIS DIMENSION INCLUDES LEAD FINISH.

Rev. 02



PCB Thermal Consideration for 64-Pin EPAD-TQFP Package

APPENDIX A

Layout and General Suggestions

1. Establish controlled impedance stripline, microstrip, or co-planar construction techniques.
2. Signal paths should have, approximately, the same width as the device pads.
3. All differential paths are critical timing paths, where skew should be matched to within ±10ps.
4. Signal trace impedance should not vary more than ±5%. If in doubt, perform TDR analysis of all high-speed signal traces.
5. Maintain compact filter networks as close to filter pins as possible. Provide ground plane relief under filter path to reduce stray capacitance. Be careful of crosstalk coupling into the filter network.
6. Maintain low jitter on the REFCLK input. Isolate the XTAL oscillator from power supply noise by adequately decoupling. Keep XTAL oscillator close to device, and minimize capacitive coupling from adjacent signals.
7. Higher speed operation may require use of fundamental-tone (third-overtone typically have more jitter) crystal based oscillator for optimum performance. Evaluate and compare candidates by measuring TXCLK jitter.
8. Evaluate ASIC AND FPGA REFIN source clocks with suitable jitter analysis equipment, such as TDS11801 tektronix DSO oscilloscope, or Wavecrest DTS2077 Time Interval Analyzer.
9. All unused outputs require termination. NC, however, should be unconnected.

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