

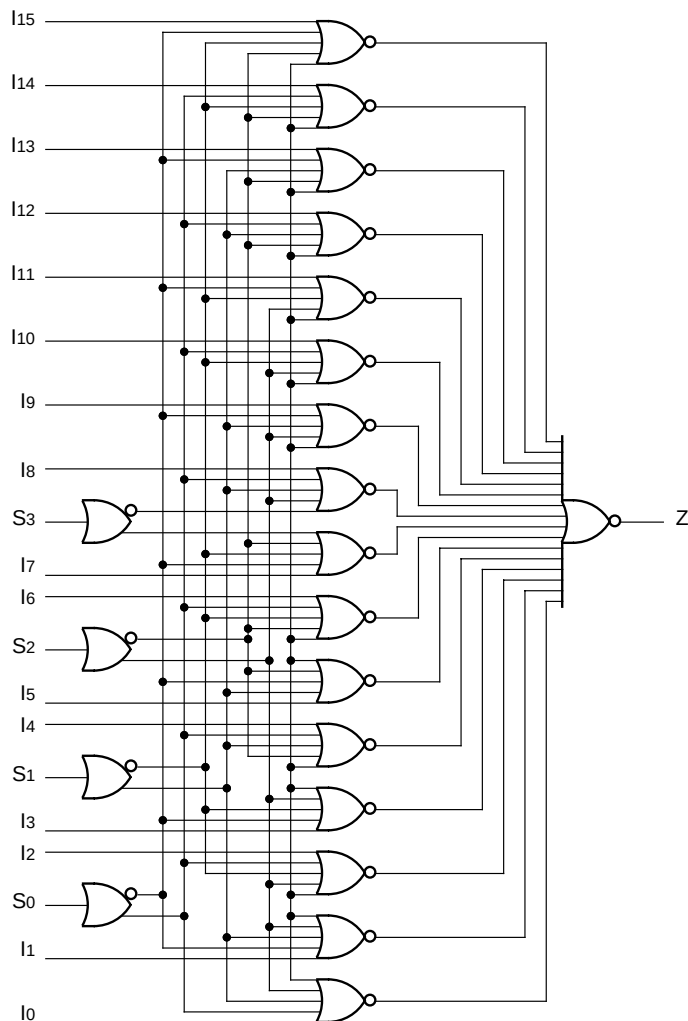
FEATURES

- Max. propagation delay of 1300ps
- IEE min. of -63mA
- Industry standard 100K ECL levels
- Extended supply voltage option:
V_{EE} = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75K Ω input pull-down resistors
- 70% faster than Fairchild
- 40% lower power than Fairchild
- Function and pinout compatible with Fairchild F100K
- Available in 24-pin CERPACK and 28-pin PLCC packages

DESCRIPTION

The SY100S364 is a 16-input multiplexer designed for use in high-performance ECL systems. The four Data Select inputs (S₀, S₁, S₂, S₃) determine the bit from the 16 inputs (I_n) that will be passed on to the output as shown in the Truth Table. The output data polarity is the same as the input. The inputs on the device have 75K Ω pull-down resistors.

BLOCK DIAGRAM



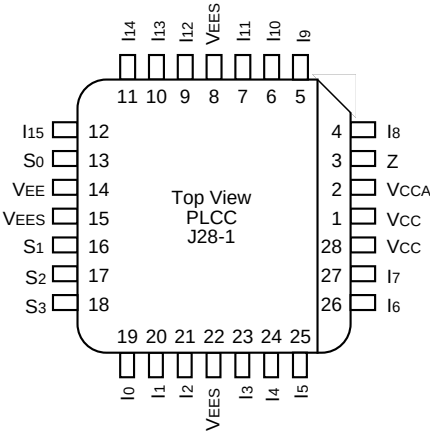
PACKAGE/ORDERING INFORMATION

Ordering Information

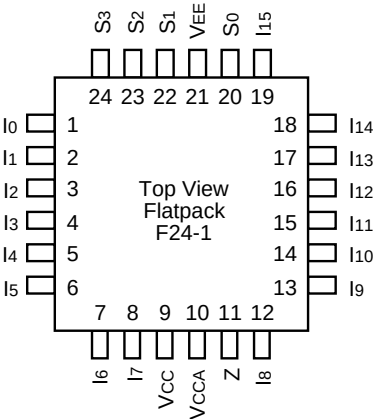
Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S364FC	F24-1	Commercial	SY100S364FC	Sn-Pb
SY100S364FCTR ⁽¹⁾	F24-1	Commercial	SY100S364FC	Sn-Pb
SY100S364JC	J28-1	Commercial	SY100S364JC	Sn-Pb
SY100S364JCTR ⁽¹⁾	J28-1	Commercial	SY100S364JC	Sn-Pb
SY100S364JZ ⁽²⁾	J28-1	Commercial	SY100S364JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S364JZTR ^(1, 2)	J28-1	Commercial	SY100S364JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

- 1. Tape and Reel.
- 2. Pb-Free package is recommended for new designs.



28-Pin PLCC (J28-1)



24-Pin Cerpack (F24-1)

PIN NAMES

Pin	Function
I ₀ – I ₁₅	Data Inputs
S ₀ – S ₃	Select Inputs
Z	Data Output
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

TRUTH TABLE⁽¹⁾

Select Inputs				Output
S ₀	S ₁	S ₂	S ₃	Z
L	L	L	L	I ₀
H	L	L	L	I ₁
L	H	L	L	I ₂
H	H	L	L	I ₃
L	L	H	L	I ₄
H	L	H	L	I ₅
L	H	H	L	I ₆
H	H	H	L	I ₇
L	L	L	H	I ₈
H	L	L	H	I ₉
L	H	L	H	I ₁₀
H	H	L	H	I ₁₁
L	L	H	H	I ₁₂
H	L	H	H	I ₁₃
L	H	H	H	I ₁₄
H	H	H	H	I ₁₅

NOTE:

1. H = HIGH Voltage Level

L = LOW Voltage Level

DC ELECTRICAL CHARACTERISTICS

VEE = –4.2V to –5.5V unless otherwise specified; VCC = VCCA = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I _{IH}	Input HIGH Current I _n S ₀ , S ₁ S ₂ , S ₃	—	—	200 200 200	μA	V _{IN} = V _{IH} (Max.)
I _{EE}	Power Supply Current	–63	–45	–30	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS**CERPACK**

VEE = –4.2V to –5.5V unless otherwise specified; VCC = VCCA = GND

Symbol	Parameter	T _A = 0°C		T _A = +25°C		T _A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay I ₀ – I ₁₅ to Output	400	1400	400	1400	400	1400	ps	
t _{PLH} t _{PHL}	Propagation Delay S ₀ , S ₁ to Output	400	1900	400	1900	400	1900	ps	
t _{PLH} t _{PHL}	Propagation Delay S ₂ , S ₃ to Output	400	1700	400	1700	400	1700	ps	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

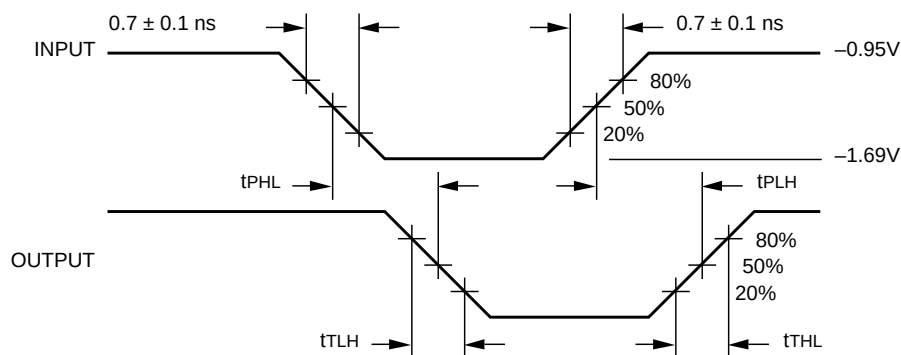
AC ELECTRICAL CHARACTERISTICS

PLCC

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay $I_0 - I_{15}$ to Output	400	1300	400	1300	400	1300	ps	
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	400	1800	400	1800	400	1800	ps	
t_{PLH} t_{PHL}	Propagation Delay S_2, S_3 to Output	400	1600	400	1600	400	1600	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

TIMING DIAGRAM

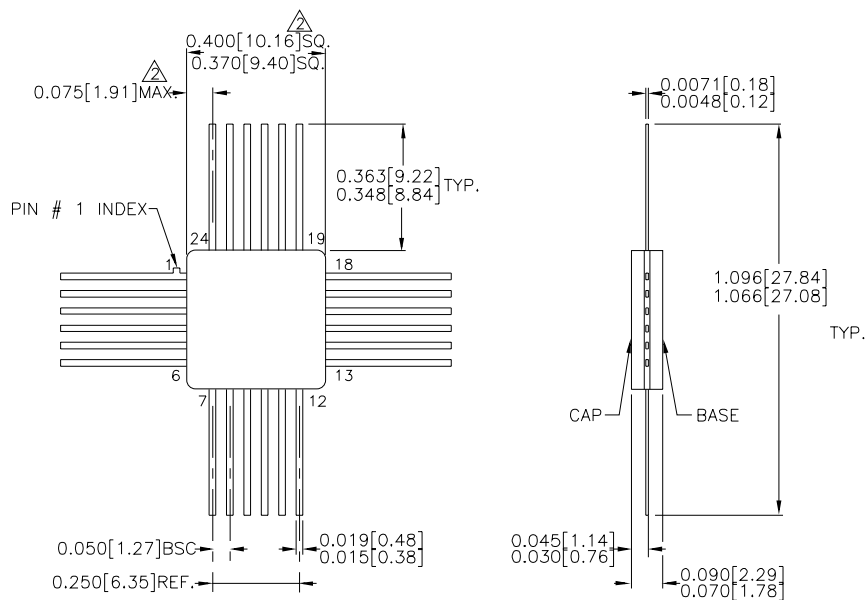


Propagation Delay and Transition Times

Note:

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

24-PIN CERPACK (F24-1)

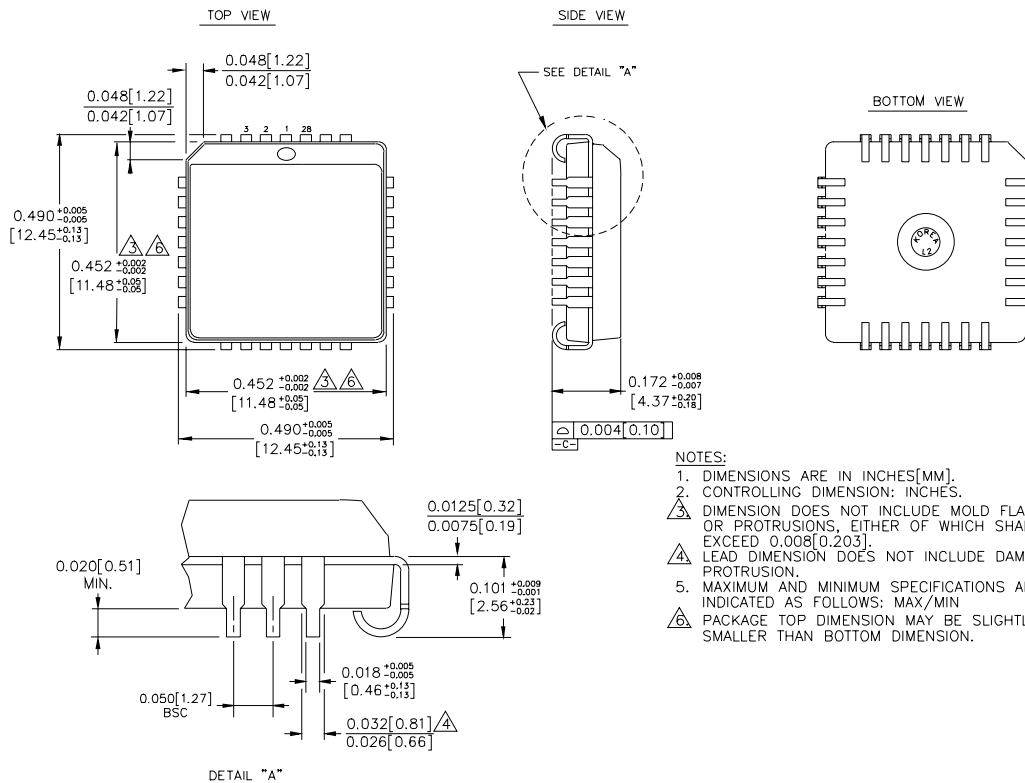


NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03

28-PIN PLCC (J28-1)



Rev. 03

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