

FEATURES

- Max. shift frequency of 700MHz
- Clock to Q delay max. of 1100ps
- S_n to $\overline{TC}$ speed improved by 50%
- S_n set-up and hold time reduced by more than 50%
- IEE min. of -170mA
- Industry standard 100K ECL levels
- Internal 75K Ω input pull-down resistors
- Extended supply voltage option:
 $V_{EE} = -4.2V$ to $-5.5V$
- Voltage and temperature compensation for improved noise immunity
- 50% faster than Fairchild 300K at lower power
- Function and pinout compatible with Fairchild F100K
- Available in 24-pin CERPAC and 28-pin PLCC packages

DESCRIPTION

The SY100S336A is functionally the same as the SY100S336, but has S_n to $\overline{TC}$ speed and S_n set-up and hold times significantly improved, allowing for higher clock frequency when used as a cascaded multi-stage counter.

The SY100S336A functions either as a modulo-16 up/down counter or as a 4-bit bidirectional shift register and is designed for use in high-performance ECL systems. Three Select inputs (S_n) are provided for determining the mode of operation. The Function Table lists the available modes of operation. In order to allow cascading for multistage counters, two Count Enable controls ($\overline{CEP}$, $\overline{CET}$) are provided. The $\overline{CET}$ input also functions as the Serial Data input (S_0) for a shift-up operation, while the D_3 input serves as the Serial Data input for the shift-down operation.

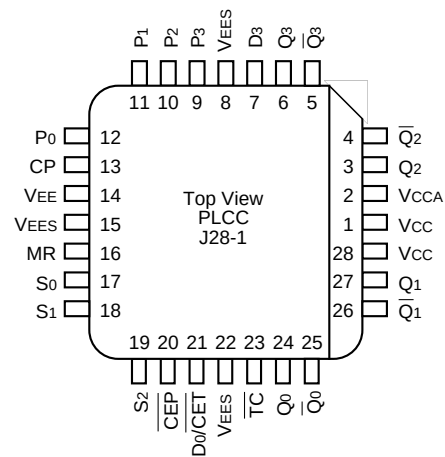
When the device is in the counting mode, the Terminal Count ($\overline{TC}$) goes to a logical LOW when the count reaches 15 for count-up or reaches 0 for count-down. When in the shift mode, the $\overline{TC}$ output simply repeats the Q_3 output.

The flexibility provided by the $\overline{TC}/Q_3$ output and the $D_0/\overline{CET}$ input allows these signals to be interconnected from one stage to the next higher stage for multistage counting or shift-up operations. The individual Presets (P_n) allow initialization of the counter by entering data in parallel to preset the counter. A logic HIGH on the Master Reset ($\overline{MR}$) overrides all other inputs and asynchronously clears the flip-flops. An additional synchronous Clear is provided, as well as a complement function which synchronously inverts the contents of the flip-flops. All inputs have 75K Ω pull-down resistors.

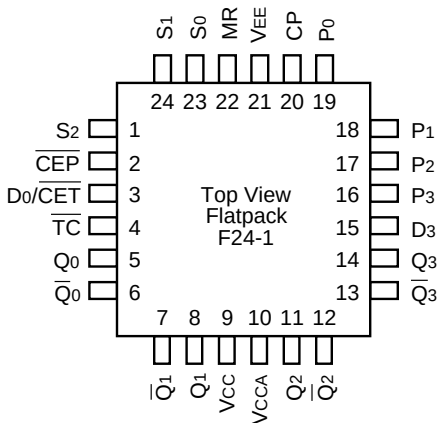
PIN NAMES

Pin	Function
CP	Clock Pulse Input
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)
$D_0/\overline{CET}$	Serial Data Input/Count Enable Trickle Input (Active LOW)
$S_0 - S_2$	Select Inputs
MR	Master Reset Input
V_{EES}	V_{EE} Substrate
V_{CCA}	V_{CCO} for ECL Outputs
$P_0 - P_3$	Preset Inputs
D_3	Serial Data Input
$\overline{TC}$	Terminal Count Output
$Q_0 - Q_3$	Data Outputs
$\overline{Q_0} - \overline{Q_3}$	Complementary Data Outputs

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)



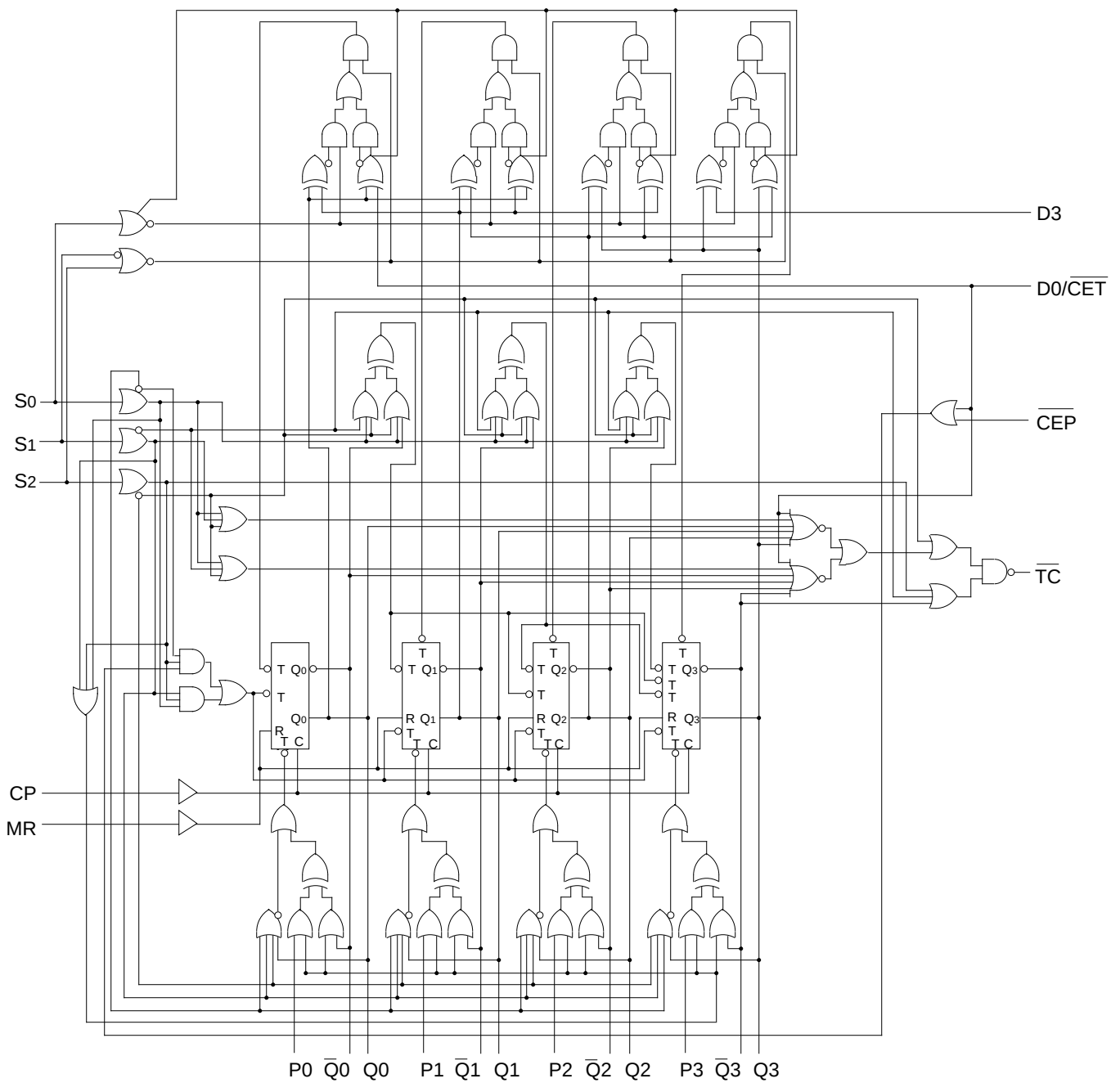
24-Pin Cerpack (F24-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S336AFC	F24-1	Commercial	SY100S336AFC	Sn-Pb
SY100S336AFCTR ⁽¹⁾	F24-1	Commercial	SY100S336AFC	Sn-Pb
SY100S336AJC	J28-1	Commercial	SY100S336AJC	Sn-Pb
SY100S336AJCTR ⁽¹⁾	J28-1	Commercial	SY100S336AJC	Sn-Pb
SY100S336AJZ ⁽²⁾	J28-1	Commercial	SY100S336AJZ with Pb-Free bar-line indicator	Matte-Sn
SY100S336AJZTR ^(1, 2)	J28-1	Commercial	SY100S336AJZ with Pb-Free bar-line indicator	Matte-Sn

- Notes:
1. Tape and Reel.
 2. Pb-Free package is recommended for new designs.

BLOCK DIAGRAM



TRUTH TABLE⁽¹⁾

Inputs								Outputs					
MR	S ₂	S ₁	S ₀	CEP	D ₀ /CET	D ₃	CP	Q ₀	Q ₁	Q ₂	Q ₃	TC	Mode
L	L	L	L	X	X	X	u	P ₀	P ₁	P ₂	P ₃	L	Preset (Parallel Load)
L	L	L	H	X	X	X	u	Q ₀	Q ₁	Q ₂	Q ₃	L	Invert
L	L	H	L	X	X	X	u	Q ₁	Q ₂	Q ₃	D ₃	D ₃	Shift Left
L	L	H	H	X	X	X	u	D ₀	Q ₀	Q ₁	Q ₂	Q ₃ *	Shift Right
L	H	L	L	L	L	X	u	(Q ₀₋₃) minus 1				①	Count Down
L	H	L	L	H	L	X	X	Q ₀	Q ₁	Q ₂	Q ₃	①	Count Down with CEP Not Active
L	H	L	L	X	H	X	X	Q ₀	Q ₁	Q ₂	Q ₃	H	Count Down with CET Not Active
L	H	L	H	X	X	X	u	L	L	L	L	H	Clear
L	H	H	L	L	L	X	u	(Q ₀₋₃) plus 1				≠	Count Up
L	H	H	L	H	L	X	X	Q ₀	Q ₁	Q ₂	Q ₃	≠	Count Up with CEP Not Active
L	H	H	L	X	H	X	X	Q ₀	Q ₁	Q ₂	Q ₃	H	Count Up with CET Not Active
L	H	H	H	X	X	X	X	Q ₀	Q ₁	Q ₂	Q ₃	H	Hold
H	L	L	L	X	X	X	X	L	L	L	L	L	Asynchronous Master Reset
H	L	L	H	X	X	X	X	L	L	L	L	L	
H	L	H	L	X	X	X	X	L	L	L	L	L	
H	L	H	H	X	X	X	X	L	L	L	L	L	
H	H	L	L	X	L	X	X	L	L	L	L	L	
H	H	L	H	X	X	X	X	L	L	L	L	H	
H	H	H	L	X	X	X	X	L	L	L	L	H	
H	H	H	H	X	X	X	X	L	L	L	L	H	

NOTE:

1. H = High Voltage Level

L = Low Voltage Level

X = Don't Care

u = LOW-to-HIGH Transition

① = L if Q₀ – Q₃ = LLLLH if Q₀ – Q₃ ≠ LLLL≠ = L if Q₀ – Q₃ = HHHHH if Q₀ – Q₃ ≠ HHHH* Before the clock, $\overline{\text{TC}}$ is Q₃; after the clock, $\overline{\text{TC}}$ is Q₂**DC ELECTRICAL CHARACTERISTICS**V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I _{IH}	Input HIGH Current, All Inputs	—	—	200	μA	V _{IN} = V _{IH} (Max.)
I _{EE}	Power Supply Current	–170	–120	–60	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERPACK

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{shift}	Shift Frequency	700	—	700	—	700	—	MHz	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n , $\bar{Q}_n$	450	1200	450	1200	450	1200	ps	
t_{PLH} t_{PHL}	Propagation Delay CP to $\bar{T}C$	600	1900	600	1900	600	1900	ps	
t_{PLH} t_{PHL}	Propagation Delay MR to Q_n , $\bar{Q}_n$	500	1400	500	1400	500	1400	ps	
t_{PLH} t_{PHL}	Propagation Delay MR to $\bar{T}C$	600	1900	600	1900	600	1900	ps	
t_{PLH} t_{PHL}	Propagation Delay $D_0/\bar{CET}$ to $\bar{T}C$	400	1200	400	1200	400	1200	ps	
t_{PLH} t_{PHL}	Propagation Delay S_n to $\bar{T}C$	400	1500	400	1500	400	1500	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t_s	Set-up Time D_3 P_n $D_0/\bar{CET}$ to $\bar{CEP}$ S_n MR (Release Time)	800 800 700 1000 900	— — — — —	800 800 700 1000 900	— — — — —	800 800 700 1000 900	— — — — —	ps	
t_h	Hold Time D_3 P_n $D_0/\bar{CET}$ to $\bar{CEP}$ S_n	200 200 200 -200	— — — —	200 200 200 -200	— — — —	200 200 200 -200	— — — —	ps	
$t_{pw} (H)$	Pulse Width HIGH, CP, MR	—	800	—	800	—	800	ps	

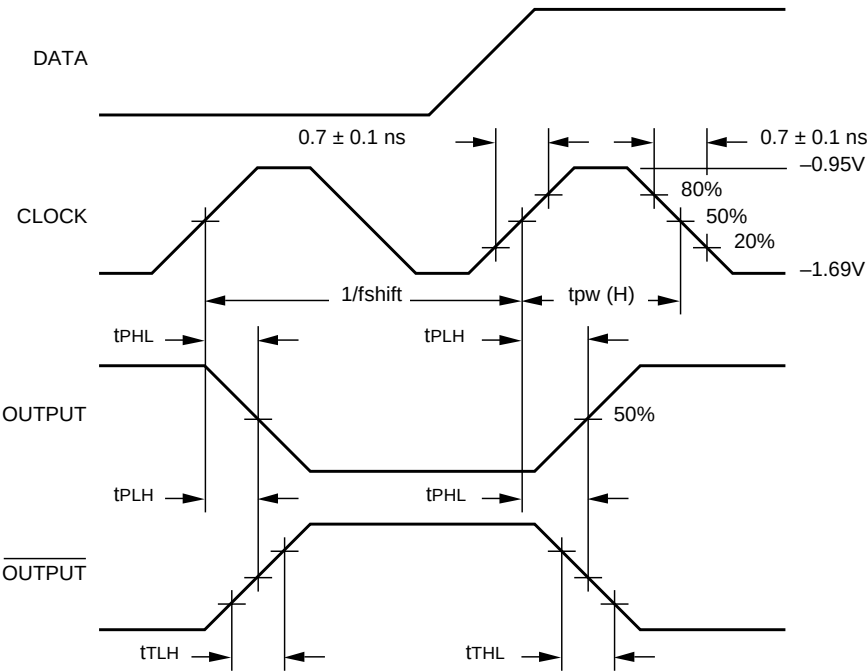
AC ELECTRICAL CHARACTERISTICS

PLCC

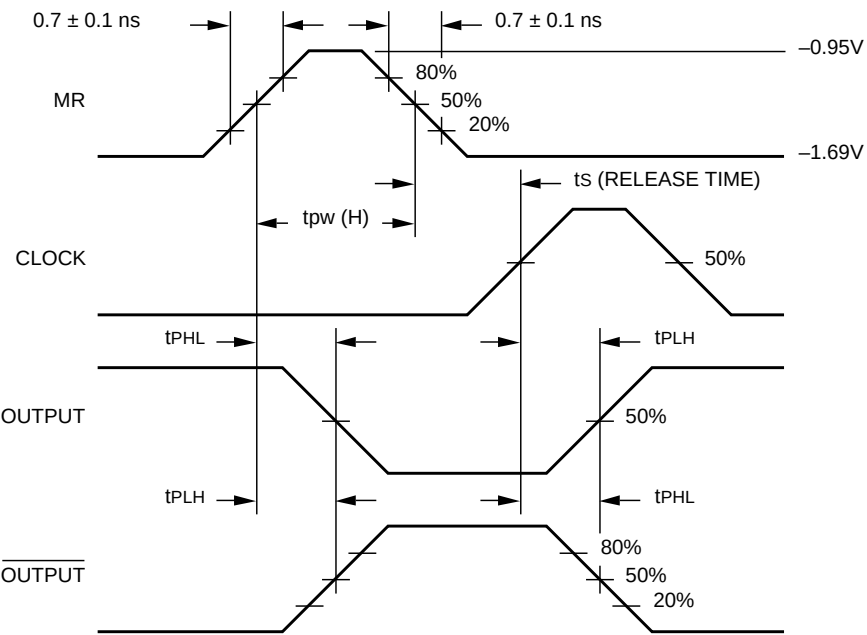
$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f _{shift}	Shift Frequency	700	—	700	—	700	—	MHz	
t _{PLH} t _{PHL}	Propagation Delay CP to Q _n , $\bar{Q}_n$	450	1100	450	1100	450	1100	ps	
t _{PLH} t _{PHL}	Propagation Delay CP to $\bar{TC}$	600	1800	600	1800	600	1800	ps	
t _{PLH} t _{PHL}	Propagation Delay MR to Q _n , $\bar{Q}_n$	500	1300	500	1300	500	1300	ps	
t _{PLH} t _{PHL}	Propagation Delay MR to $\bar{TC}$	600	1800	600	1800	600	1800	ps	
t _{PLH} t _{PHL}	Propagation Delay D ₀ / $\bar{CET}$ to $\bar{TC}$	400	1100	400	1100	400	1100	ps	
t _{PLH} t _{PHL}	Propagation Delay S _n to $\bar{TC}$	400	1500	400	1500	400	1500	ps	
t _{TLH} t _{THL}	Transition Time ³⁰⁰ 20% to 80%, 80% to 20%	900	300	900	300	900	300	ps	
t _s	Set-up Time							ps	
	D ₃	800	—	800	—	800	—		
	P _n	800	—	800	—	800	—		
	D ₀ / $\bar{CET}$ to $\bar{CEP}$	700	—	700	—	700	—		
	S _n	1000	—	1000	—	1000	—		
t _H	MR (Release Time)	900	—	900	—	900	—	ps	
	Hold Time								
	D ₃	200	—	200	—	200	—		
	P _n	200	—	200	—	200	—		
	D ₀ / $\bar{CET}$ to $\bar{CEP}$	200	—	200	—	200	—		
t _{pw} (H)	S _n	-200	—	-200	—	-200	—		
	Pulse Width HIGH, CP, MR	—	800	—	800	—	800	ps	

TIMING DIAGRAMS

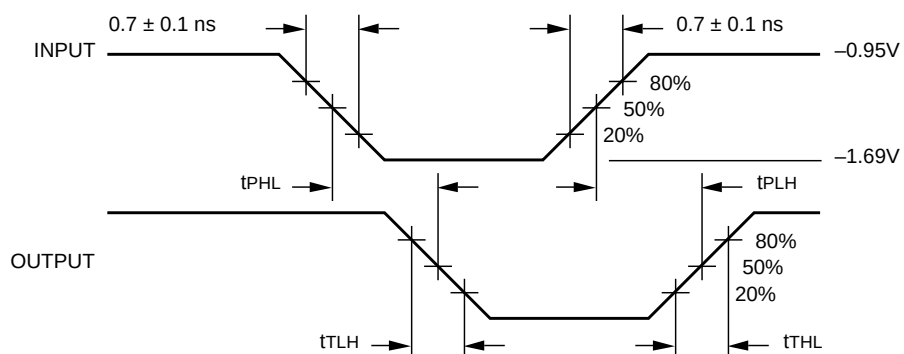


Propagation Delay (Clock) and Transition Times

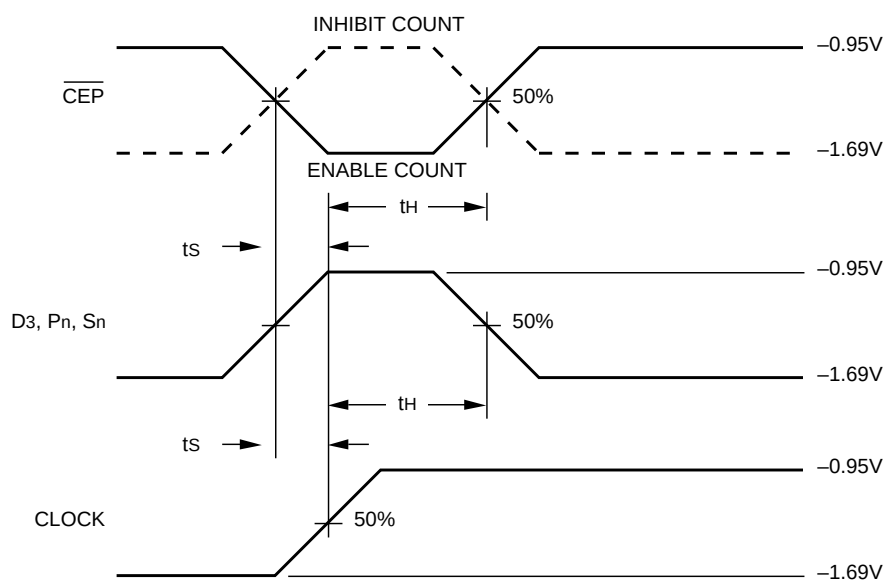


Propagation Delay (Reset)

TIMING DIAGRAMS



Propagation Delay (Serial Data, Selects)

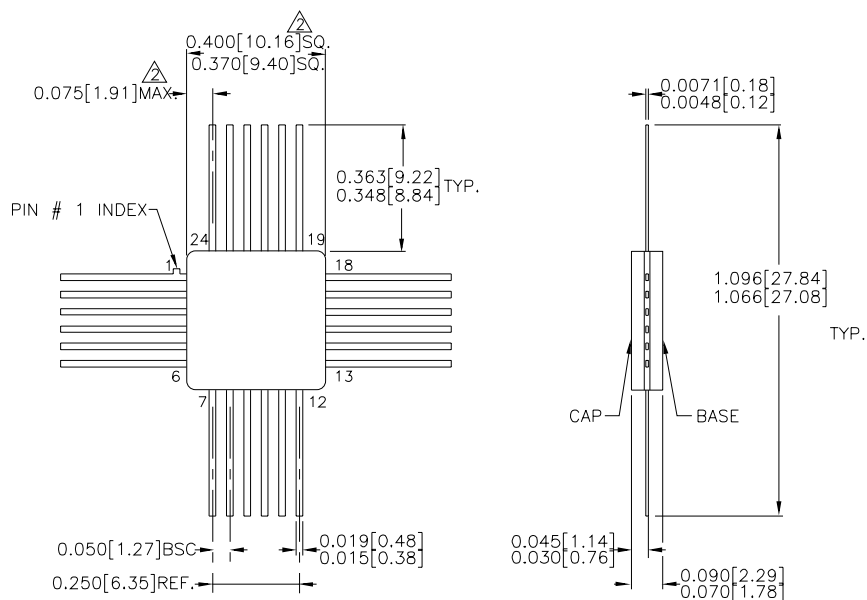


Set-up and Hold Time

Notes:

1. $V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$.
2. t_s is the minimum time before the transition of the clock that information must be present at the data input.
3. t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

24-PIN CERPACK (F24-1)

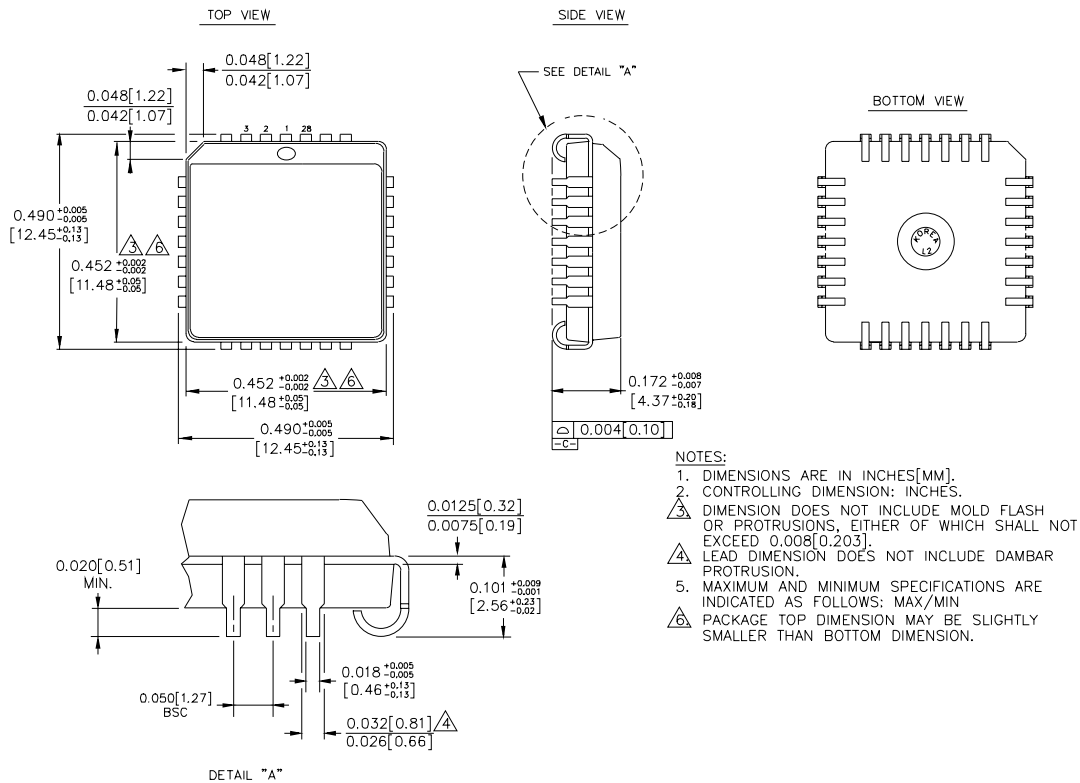


NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03

28-PIN PLCC (J28-1)



Rev. 03

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