

FEATURES

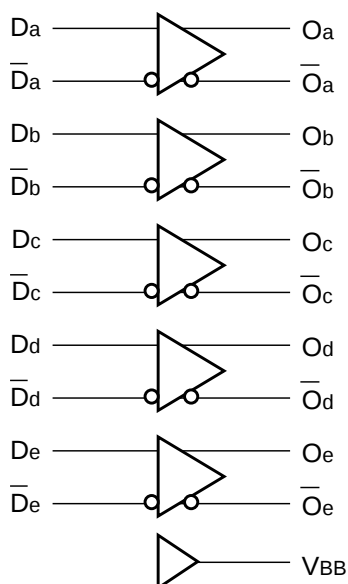
- Max. propagation delay of 900ps
- Differential outputs
- IEE min. of -60mA
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- VBB output for single-ended use
- More than twice as fast as Fairchild
- Function and pinout compatible with Fairchild F100K
- Available in 24-pin CERPAC and 28-pin PLCC packages

DESCRIPTION

The SY100S314 offers five differential line receivers with emitter follower outputs, designed for use in high-performance ECL systems. For single-ended operation, the VBB reference voltage is available. In the single-ended mode, the apparent input threshold of the true inputs is 30mV higher than the threshold of the complementary inputs.

Common mode rejection of +1.0V is achieved through the use of active current sources. If both the true and complement inputs are at the same potential between VEE and VCC, then the complementary outputs will take on a logic HIGH state. Unlike the other members of the Synergy 300K family, the inputs on this device do not have pull-down resistors.

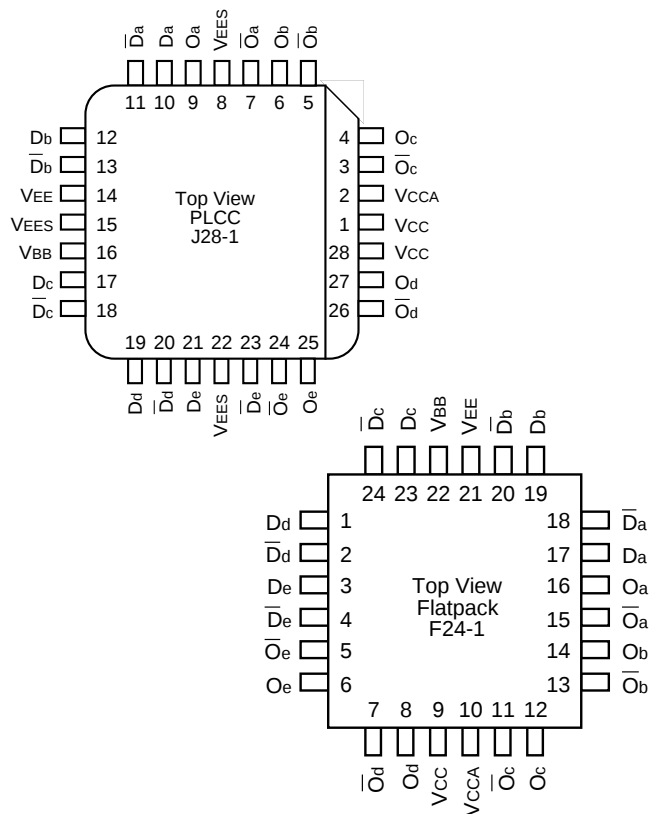
BLOCK DIAGRAM



PIN NAMES

Pin	Function
Da – De	Data Inputs
$\bar{D}a - \bar{D}e$	Inverting Data Inputs
Oa – Oe	Data Outputs
$\bar{O}a - \bar{O}e$	Complementary Data Outputs
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

PIN CONFIGURATIONS



LOGIC EQUATION

$O = D$

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{DIFF}	Input Voltage Differential	150	—	—	mV	Required for Full Output Swing
V_{CM}	Common Mode Voltage	—	—	1.0	V	Permissible $\pm V_{CM}$ with Respect to V_{BB}
I_{IH}	Input HIGH Current	—	—	50	μA	$V_{IN} = V_{IH} (Max.)$, $D_a - D_e = V_{BB}$, $\overline{D}_a - \overline{D}_e = V_{IL} (Min.)$
I_{CBO}	Input Leakage Current	-10	—	—	μA	$V_{IN} = V_{EE}$, $D_a - D_e = V_{BB}$, $\overline{D}_a - \overline{D}_e = V_{IL} (Min.)$
I_{EE}	Power Supply Current	-60	-45	-30	mA	$D_a - D_e = V_{BB}$, $\overline{D}_a - \overline{D}_e = V_{IL} (Min.)$

AC ELECTRICAL CHARACTERISTICS

CERPACK

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

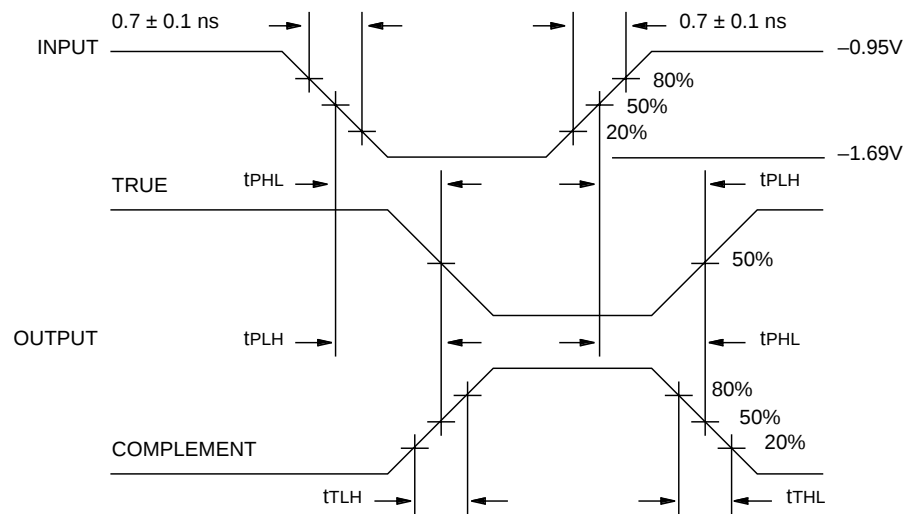
Symbol	Parameter	$T_A = 0^\circ C$		$T_A = +25^\circ C$		$T_A = +85^\circ C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	300	1000	300	1000	300	1000	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

PLCC

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^\circ C$		$T_A = +25^\circ C$		$T_A = +85^\circ C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	300	900	300	900	300	900	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

TIMING DIAGRAM



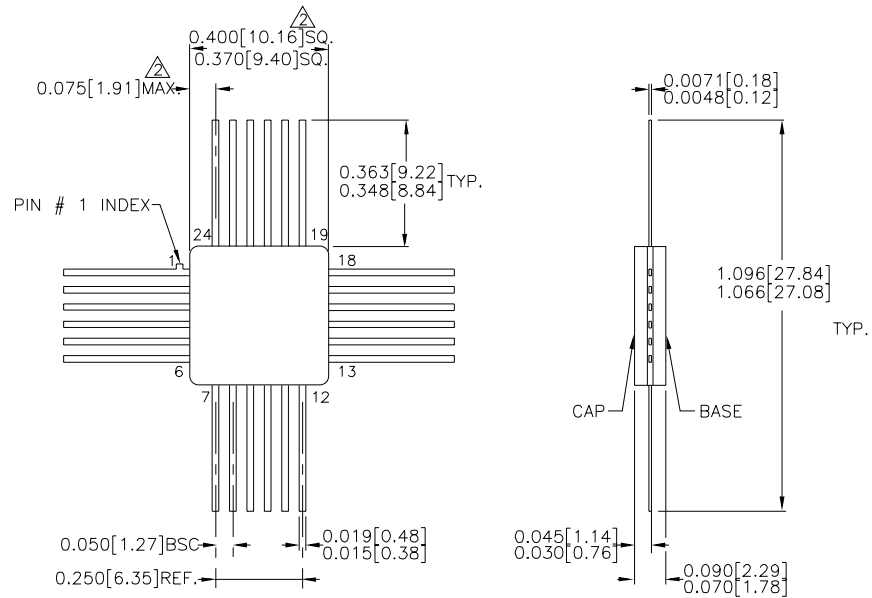
Propagation Delay and Transition Times

NOTE:
 $V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S314FC	F24-1	Commercial
SY100S314JC	J28-1	Commercial
SY100S314JCTR	J28-1	Commercial

24 LEAD CERPACK (F24-1)

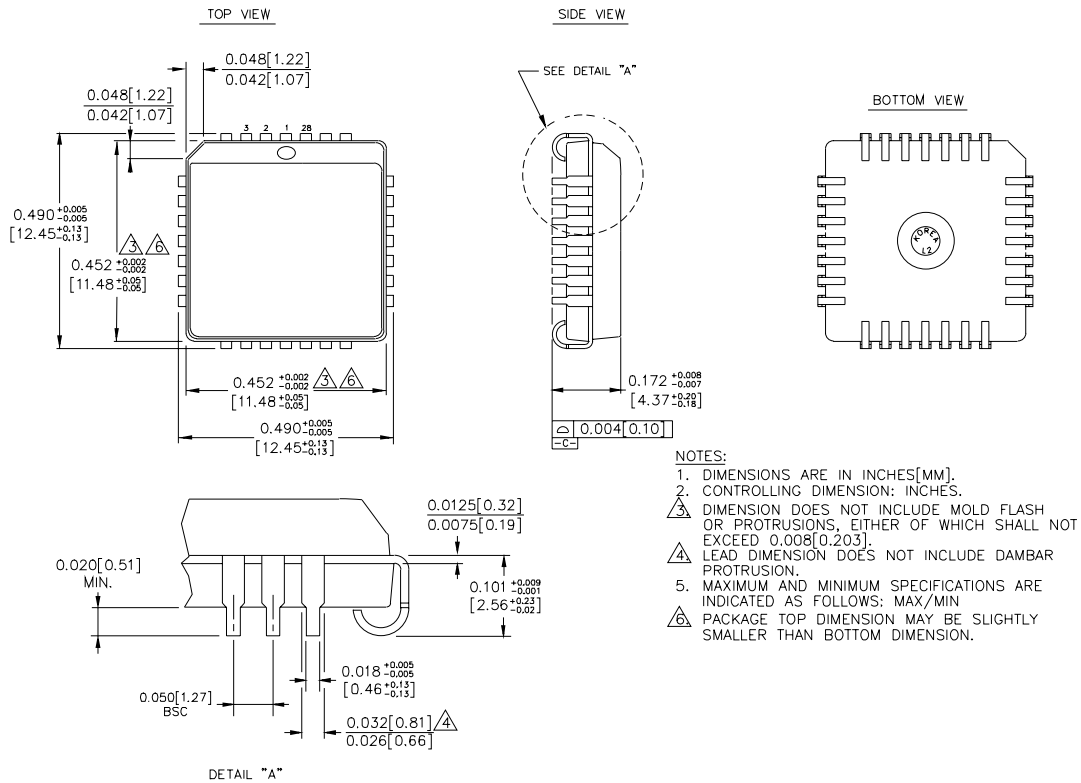


NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03

28 LEAD PLCC (J28-1)



Rev. 03

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