MIC24046-H

Pin-Programmable, 4.5V – 19V, 5A Step-Down Converter

General Description

Micrel's MIC24046-H is a pin-programmable, high-efficiency, wide-input range, 5A, synchronous step-down regulator. The MIC24046-H is perfectly suited for multiple-voltage rail application environments typically found in computing and telecommunication systems. It can be programmed by pin strapping various parameters, such as output voltage, switching frequency, and current-limit values. The pin-selectable switching frequency, valley-current-mode control technique, high-performance error amplifier, and external compensation allow for the best tradeoffs between high-efficiency and the smallest possible solution size.

The MIC24046-H is pin-out compatible with its I²C-programmable counterparts from the same family.

The MIC24046-H is available in a thermally-efficient, space-saving, 20-pin 3mm × 3mm QFN package with an operating junction temperature range of –40°C to +125°C.

Datasheets and support documentation are available on Micrel's website at: www.micrel.com.

Features

- 4.5V to 19V input voltage range
- 5A (maximum) output current
- High efficiency (>90%)
- Pin-selectable output voltages:
  - 0.7V, 0.8V, 0.9V, 1.0V, 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V
- ±1% output voltage accuracy
- Supports safe start-up with pre-biased output
- Pin-selectable current limit and switching frequency
- Internal soft-start and thermal shutdown protection
- Hiccup-mode short-circuit protection
- Available in a 20-pin 3mm × 3mm QFN package
- –40°C to +125°C junction temperature range

Applications

- Servers, data storage, routers, and base stations
- FPGAs, DSP, and low-voltage ASIC power
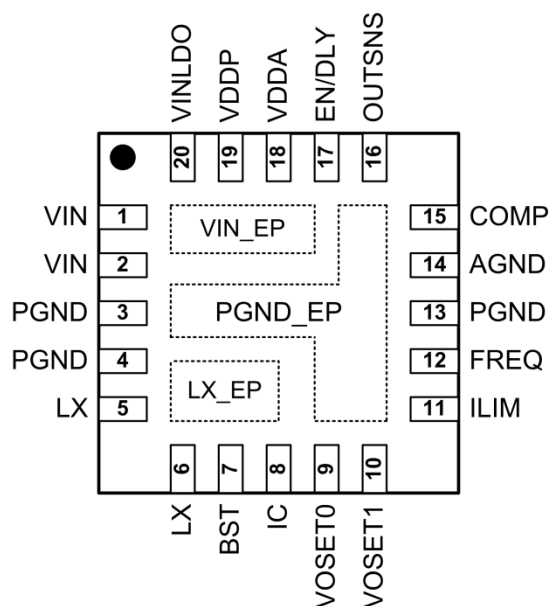
Typical Application
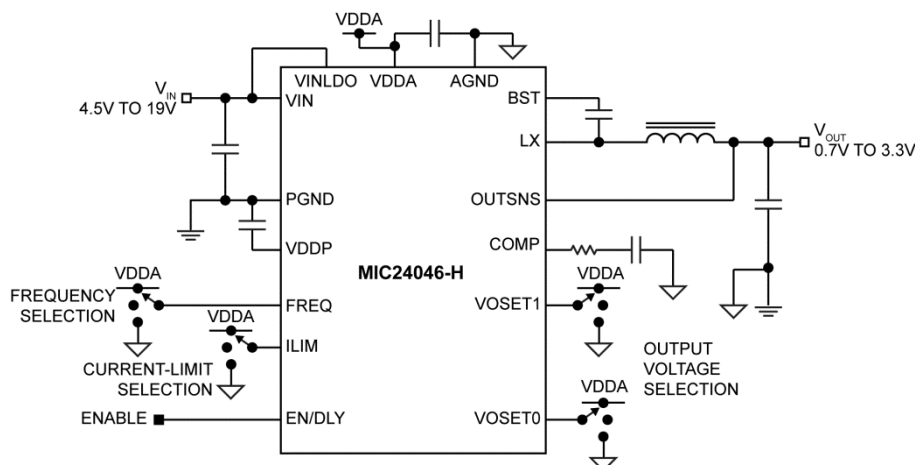
MIC24046-H 12VIN 5A DC-to-DC Converter

Ordering Information

Part Number	Junction Temperature Range	Package	Lead Finish
MIC24046-HYFL	–40°C to +125°C	20-Pin 3 mm × 3 mm QFN	Pb-Free

Pin Configuration

20-Pin 3mm × 3mm QFN (FL)
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1 – 2	VIN	Input Voltage for the Buck Converter Power Stage: These pins are the drain terminal of the internal high-side N-channel MOSFET. A 10µF minimum ceramic capacitor should be connected from VIN to PGND as close as possible to the device. A combination of multiple ceramic capacitors of different sizes is recommended.
3 – 4, 13	PGND	Low-Side MOSFET Source Terminal and Low-Side Driver Return: Connect the ceramic input capacitors to PGND as close as possible to the device.
5 – 6	LX	Switch Node: Drain (low-side MOSFET) and source (high-side MOSFET) connection of the internal power N-channel FETs. The external inductor (switched side) and bootstrap capacitor (bottom terminal) must be connected to these pins.
7	BST	Bootstrap: Supply voltage for the driver of the high-side N-channel power MOSFET. Connect the bootstrap capacitor (top terminal) to this pin.
8	IC	Internally Connected for test mode purposes. Connect to AGND or leave floating in normal operation.
9	VOSET0	Three-state Pin (Low, High, and High-Z) for Output Voltage Programming: Together with VOSET1, VOSET0 defines nine logic values corresponding to nine output voltage selections.
10	VOSET1	Three-State Pin (Low, High, and High-Z) for Output Voltage Programming: Together with VOSET0, VOSET1 defines nine logic values corresponding to nine output voltage selections.

Pin Description (Continued)

Pin Number	Pin Name	Pin Function
11	ILIM	Three-State (Low, High, and High-Z) Current-Limit Selection Pin.
12	FREQ	Three-State (Low, High, and High-Z) Switching Frequency Selection Pin.
14	AGND	Analog Ground: Quiet ground for the analog circuitry of the internal regulator and return terminal for the external compensation network.
15	COMP	Transconductance Error Amplifier Output: Connect a compensation network from this pin to AGND.
16	OUTSNS	Output Sensing: Connect this pin directly to the buck converter output voltage. This pin is the top side terminal of the internal feedback divider.
17	EN/DLY	Precision Enable/Turn-On Delay Input. The EN/DLY pin is first compared against a 507mV threshold to turn-on the on-board LDO regulator. The EN/DLY pin is then compared against a 1.21V (typical) threshold to initiate output power delivery. A 150mV typical hysteresis prevents chattering when power delivery is started. A 2µA (typical) current source pulls up the EN/DLY pin. Turn-on delay can be achieved by connecting a capacitor from EN/DLY to ground, while using an open-drain output to drive the EN/DLY pin.
18	VDDA	Output of the internal linear regulator and internal supply for analog control. A 1µF minimum ceramic capacitor should be connected from this pin to AGND; 2.2µF nominal value recommended.
19	VDDP	Internal Supply Rail for the MOSFET Drivers (fed by the VDDA pin): An internal resistor (10Ω) between pins VDDP and VDDA is provided in the regulator in order to implement an RC filter for switching noise suppression. A 1µF minimum ceramic capacitor should be connected from this pin to PGND; 2.2µF nominal value recommended.
20	VINLDO	Input of the Internal Linear Regulator: This pin is typically connected to the input voltage of the buck converter stage (VIN). If VINLDO and VIN are connected to different voltage rails, individually bypass VINLDO to ground with a 100nF ceramic capacitor.
PGND_EP	PGND	PGND Exposed Pad: Electrically connected to PGND pins. Connect with thermal vias to the ground plane to ensure adequate heat-sinking. Follow recommendations as illustrated in the *PCB Layout Recommendations* section
VIN_EP	VIN	VIN Exposed Pad: Electrically connected to VIN pins. If an input power distribution plane is available, connect with thermal vias to that plane to improve heat-sinking. Follow recommendations as illustrated in the *PCB Layout Recommendations* section
LX_EP	LX	LX Exposed Pad: Electrically connected to LX pins. Follow recommendations as illustrated in the *PCB Layout Recommendations* section

Absolute Maximum Ratings[1]

V_{VIN}, V_{VINLDO} to AGND .... −0.3V to +20V

V_{VDDP}, V_{VDDA} to AGND .... −0.3V to +6V

V_{VINLDO} to V_{VDDA} .... −0.3V to +20V

V_{VDDP} to V_{VDDA} .... −0.3V to +0.3V

V_{VOSETx}, V_{FREQ}, V_{ILIM}, to AGND .... −0.3V to +6V

V_{BST} to V_{LX} .... −0.3V to +6V

V_{BST} to AGND .... −0.3V to +26V

$V_{EN/DLY}$ to AGND .... −0.3V to V_{VDDA} + 0.3V, +6V

V_{COMP}, V_{OUTSNS} to AGND .... −0.3V to V_{VDDA} + 0.3V, +6V

AGND to PGND.. −0.3V to +0.3V

Junction Temperature .... +150°C

Storage Temperature (T_S) .... −65°C to +150°C

Lead Temperature (soldering, 10s) .... 260°C

ESD Rating[4]

    HBM 2kV

    MM 150V

Operating Ratings[2]

Supply Voltage (V_{VIN}, V_{VINLDO}) .... 4.5V to 19V

Externally Applied Analog and Drivers Supply Voltage

(V_{VINLDO} = V_{VDDA} = V_{VDDP}) .... 4.5V to 5.5V

Enable Voltage ($V_{EN/DLY}$) .... 0V to V_{VDDA}

Output Current 5A

Junction Temperature (T_J) .... −40°C to +125°C

Junction to Ambient Thermal Resistance

    20-pin 3mm x 3mm QFN ($θ_{JA}$)[3] .... 29°C/W

Electrical Characteristics[5]

V_{VIN} = V_{VINLDO} = 12V; C_{VDDA} = 2.2μF, C_{VDDP} = 2.2μF, T_A = 25°C, unless otherwise noted. **Bold** values indicate −40°C ≤ T_J ≤ +125°C.

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Units
VIN Supply							
VIN	Input Range			**4.5**		**19**	V
IVINQ	Disable Current	EN/DLY = 0V	T_A = T_J = 25°C		35	42	μA
			−40°C ≤ T_J ≤ +125°C			**56**	
IVINOp	Operating Current	EN/DLY > 1.28V, OUTSNS = 1.15 × $V_{OUT(NOM)}$, no switching, T_A = T_J = 25°C			5.6	7	mA
VDDA 5V Supply							
VDDA	Operating Voltage	EN/DLY > 0.58V, $I_{(VDDA)}$ = 0mA to 10mA		**4.8**	5.1	**5.4**	V
	Dropout Operation	V_{INLDO} = 4.5V, EN/DLY > 0.58V, $I_{(VDDA)}$ = 10mA		**3.6**	3.75		V
VDDA Undervoltage Lockout							
UVLO_R	VDDA UVLO Rising	V_{VDDA} Rising, EN/DLY > 1.28V		**3.1**	3.5	**3.9**	V
UVLO_F	VDDA UVLO Falling	V_{VDDA} Falling, EN/DLY > 1.28V		**2.87**	3.2	**3.45**	V
UVLO_H	VDDA UVLO Hysteresis				300		mV

Notes:

1. Exceeding the absolute maximum ratings may damage the device.

2. The device is not guaranteed to function outside operating range.

3. $θ_{JA}$ is measured on the MIC24046-H evaluation board.

4. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5kΩ in series with 100pF.

5. Specification for packaged product only.

Electrical Characteristics[5] (Continued)

$V_{VIN} = V_{VINLDO} = 12V$; $C_{VDDA} = 2.2\mu F$, $C_{VDDP} = 2.2\mu F$, $T_A = 25°C$, unless otherwise noted. **Bold** values indicate $-40°C \le T_J \le +125°C$.
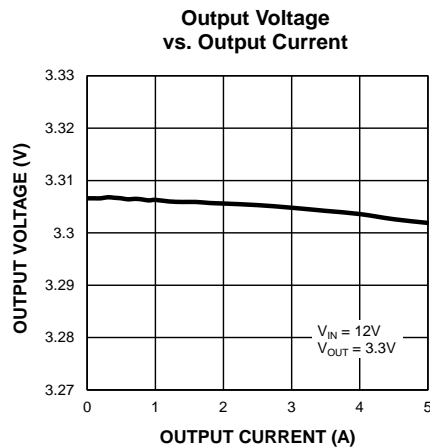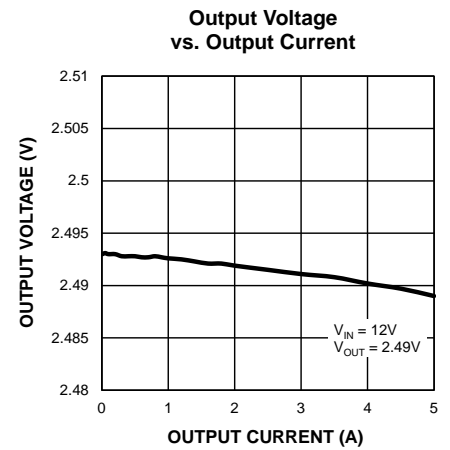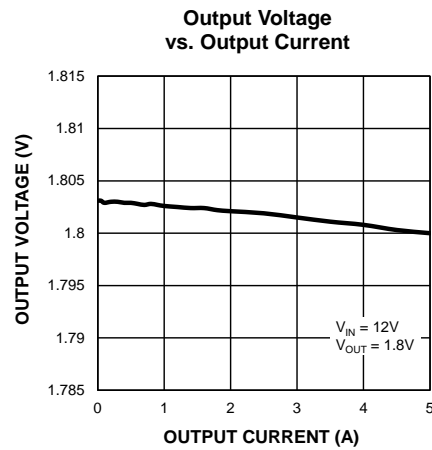
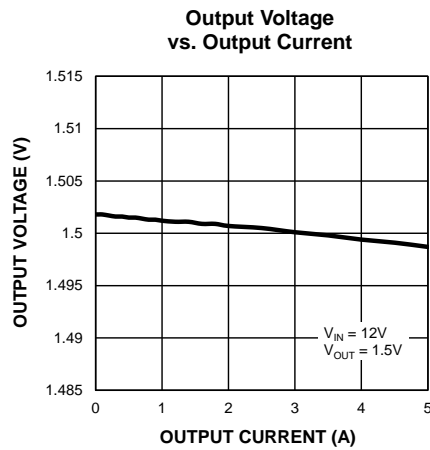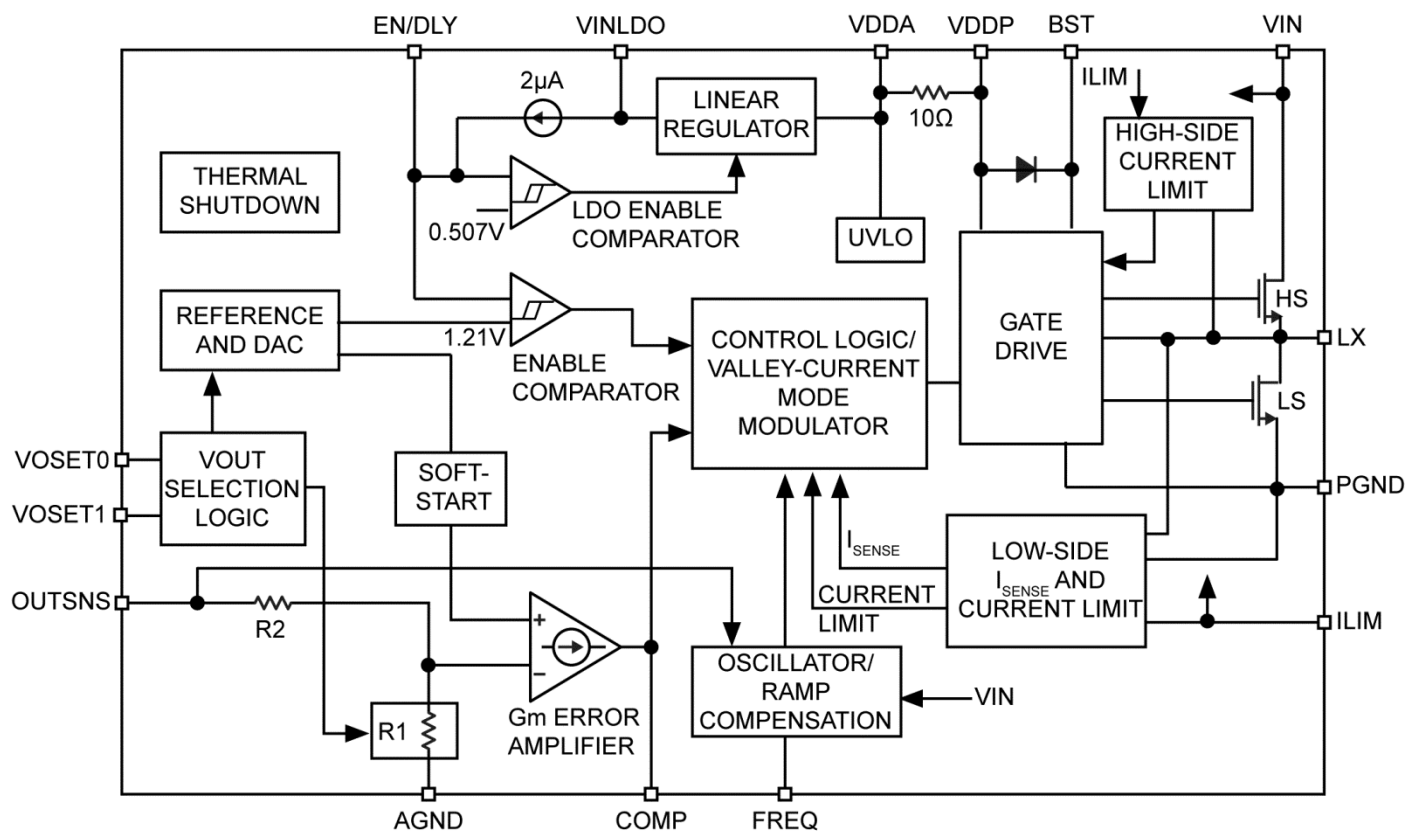| Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
EN/DLY Control						
EN_LDO_R	LDO Enable Threshold	Turns On VDDA LDO		507	**580**	mV
EN_LDO_F	LDO Disable Threshold	Turns Off VDDA LDO	**460**	491		mV
EN_LDO_H	LDO Threshold Hysteresis			16		mV
EN_R	EN/DLY Rising Threshold	Initiates power-stage operation	**1.14**	1.21	**1.28**	V
EN_F	EN/DLY Falling Threshold	Stops power-stage operation		1.06		V
EN_H	EN/DLY Hysteresis			150		mV
EN_I	EN/DLY Pull-Up Current	$T_A = T_J = 25°C$	1	2	3	µA
Switching Frequency						
f_{SZ}	Programmable Frequency (High Z)	FREQ = High Z (open)	**360**	400	**440**	kHz
f_{S0}	Programmable Frequency 0	FREQ = Low (GND)	**500**	565	**630**	kHz
f_{S1}	Programmable Frequency 1	FREQ = High (VDDA)	**700**	790	**880**	kHz
Overcurrent Protection						
I_{LIM_HS0}	HS Current Limit 0	ILIM = Low (GND)	**6.0**	7.1	**8.1**	A
I_{LIM_HS1}	HS Current Limit 1	ILIM = High (VDDA)	**8.1**	9.3	**10.3**	A
I_{LIM_HSZ}	HS Current Limit High Z	ILIM = High Z (open)	**9.3**	10.5	**11.9**	A
LEB	Top FET Current-Limit Leading Edge-Blanking Time			108		ns
I_{LIM_LS0}	LS Current Limit 0	ILIM = Low (GND)	**3.0**	4.6	**6.3**	A
I_{LIM_LS1}	LS Current Limit 1	ILIM = High (VDDA)	**4.0**	6.2	**7.9**	A
I_{LIM_LSZ}	LS Current Limit Hi Z	ILIM = High Z (Open)	**5.0**	6.8	**8.6**	A
IN_{HICC_DE}	OC Events Count for Hiccup	Number of subsequent cycles in current limit before entering hiccup overload protection.		15		Clock Cycles
t_{HICC_WAIT}	Hiccup Wait Time	Duration of the High-Z state on LX before new soft-start.		3 x Soft-Start Time		
Power Switches						
R_{BOTTOM}	Bottom FET ON resistance	$V_{VIN} = V_{VINLDO} = V_{VDDP} = V_{VDDA} = 5V$, $V_{BST}-V_{LX} = 5V$, $T_A = T_J = 25°C$		16	21	mΩ
R_{TOP}	Top FET ON resistance	$V_{VIN} = V_{VINLDO} = V_{VDDP} = V_{VDDA} = 5V$, $V_{BST}-V_{LX} = 5V$, $T_A = T_J = 25°C$		38	50	mΩ
Pulse-Width Modulation (PWM)						
$T_{ON(MIN)}$	Minimum LX ON Time	$T_A = T_J = 25°C$		26		ns
$T_{OFF(MIN)}$	Minimum LX OFF time	$V_{VIN} = V_{VINLDO} = V_{VDDA} = 5V$, $V_{OUTSNS} = 3V$, FREQ = Open (400kHz setting), $V_{VOSET0} = V_{VOSET1} = 0V$ (3.3V setting), $T_A = T_J = 25°C$	90	135	190	ns
D_{MIN}	Minimum Duty Cycle	$V_{OUTSNS} > 1.1 \times V_{OUT(NOM)}$		0		%

Electrical Characteristics[5] (Continued)

V_{VIN} = V_{VINLDO} = 12V; C_{VDDA}= 2.2µF, C_{VDDP} = 2.2µF, T_A = 25°C, unless otherwise noted. **Bold** values indicate −40°C ≤ T_J ≤ +125°C.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Gm Error Amplifier						
Gm_{EA}	Error-Amplifier Transconductance			1.5		mmho
A_{EA}	Error-Amplifier DC Gain			50000		V/V
I_{SR_SNK}	Error-Amplifier Source/Sink Current		−400		+400	µA
COMP_H	COMP Output Swing High			2.4		V
COMP_L	COMP Output Swing Low			0.8		V
Gm_{PS}	COMP-to-Inductor Current Transconductance	V_{OUT} = 1.2V, I_{OUT} = 4A		12.5		A/V
Output Voltage DC Accuracy						
OutErr12	Output Voltage Accuracy for Ranges 1 and 2	4.75V ≤ V_{IN} ≤ 19V, V_{OUT} = 0.7V to 1.8V T_A = T_J = −40°C to 125°C, I_{OUT} = 0A	−1		1	%
OutErr3	Output Voltage Accuracy for Range 3	4.75V ≤ V_{IN} ≤ 19V, V_{OUT} = 2.49V to 3.3V T_A = T_J = −40°C to 125°C, I_{OUT} = 0A	−1.5		1.5	%
LoadReg	Load Regulation	I_{OUT} = 0A to 5A		0.25		%
LineReg	Line Regulation	6V< V_{IN} < 19V, I_{OUT} = 2A		0.1		%
Internal Soft-Start						
SS_SR	Reference Soft-Start Slew Rate	V_{OUT} = 0.7V, 0.8V, 0.9V, 1.0V, 1.2V		0.45		V/ms
Thermal Shutdown						
T_{SHDN}	Thermal Shutdown			160		°C
T_{SHDN_HYST}	Thermal-Shutdown Hysteresis			25		°C
Efficiency						
η	Efficiency	V_{IN} = 12V, V_{OUT} = 0.9V, I_{OUT} = 2A f_S = f_{SZ} = 400kHz, L = 1.2µH, T_A = 25°C		82.3		%

Typical Characteristics

**Efficiency
vs. Output Current**

**Output Voltage
vs. Output Current**

**Output Voltage
vs. Output Current**

**Output Voltage
vs. Output Current**

**Output Voltage
vs. Output Current**

**Output Voltage
vs. Output Current**

**Output Voltage
vs. Output Current**
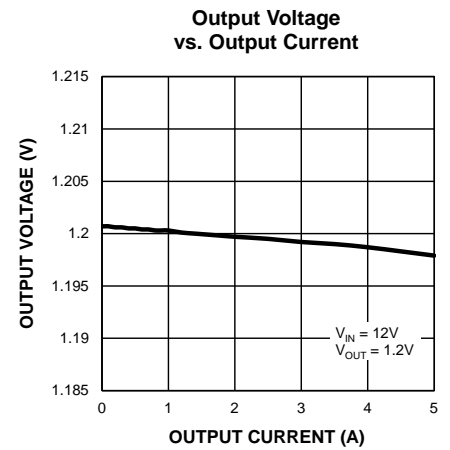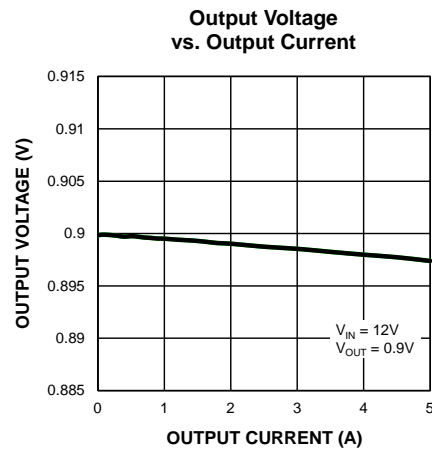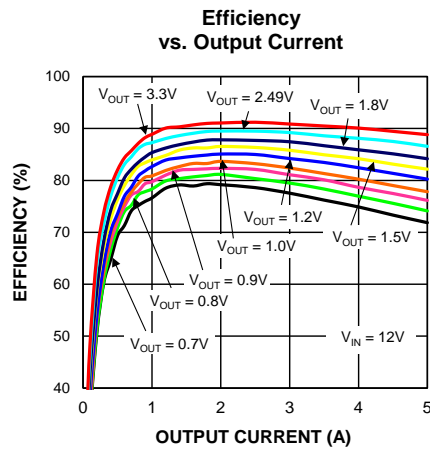
Functional Diagram

Functional Description

The MIC24046-H is a pin-programmable, 5A valley current-mode controlled regulator, with an input voltage range from 4.5V to 19V.

The MIC24046-H requires a minimal amount of external components. Only inductor, supply decoupling capacitors and compensation network are external. The flexibility in designing the external compensation allows the user to optimize the design across the entire input voltage and selectable output voltages range.

Theory of Operation

Valley current-mode control is a fixed-frequency, leading-edge-modulated PWM current mode control. As opposed to peak-current-mode, in valley current mode the clock marks the turn-off of the high-side switch, and the turn on of the low-side switch. After this instant, in the MIC24046-H the low-side switch current level is compared against the reference current signal from the error amplifier. As soon as the falling low-side switch current signal drops below the current reference signal, the high side switch is turned on. As a result, the inductor valley current is regulated to a level dictated by the output of the error amplifier.

As shown in the "Compensation Design" sub-section within the *Application Information* section, the feedback loop includes an internal programmable reference (REF_{DAC}) and output voltage sensing attenuator (R2/R1), removing the need for external feedback components and improving regulation accuracy. Output voltage feedback is achieved by connecting OUTSNS directly to the output. The high-performance transconductance error amplifier drives an external compensation network at the COMP pin. The voltage at COMP represents the reference current signal. The latter is fed to the valley current mode modulator, which also adds slope compensation to guarantee current-loop stability. Valley current-mode control requires slope compensation at duty cycles less than 50% for current-loop stability. The slope compensation circuit is internal, and it is automatically adapted in amplitude depending upon the frequency, output voltage range, and voltage differential ($V_{VIN} - V_{OUTSNS}$). Internal low-$R_{DS(ON)}$ power MOSFETs, the associated adaptive gate driver and internal bootstrap diode complete the power train.

Overcurrent protection and thermal shutdown protect the MIC24046-H from faults or abnormal operating conditions.

Internal LDO, Supply Rails (VIN, VINLDO, VDDA, VDDP)

VIN represents the power train input. These pins are the drain connection of the internal high-side MOSFET and should be bypassed to GND with a X5R or X7R 10µF (minimum) ceramic capacitor, placed as close as possible to the IC. A combination of ceramic capacitors of different sizes is recommended.

An internal LDO (input = VINLDO) provides a clean supply (5.1V typ.) for the analog circuits at pin VDDA. The internal LDO is typically powered from the same power rail fed at VIN; however VINLDO can also be higher or lower than VIN and can be connected to any other voltage within its recommended limits. VINLDO and VDDA should be locally bypassed (see *Pin Description*). A small series resistor (typically 2Ω-10Ω) can be used in combination with the VINLDO bypass capacitor to implement a RC filter for suppression of large high-frequency switching noise.

The internal LDO is enabled when the voltage at the EN/DLY pin exceeds about 0.51V and regulation takes place as soon as enough voltage has established between the VINLDO and VDDA pins. If an external 5V±10% is available it is possible to bypass the internal LDO by connecting VINLDO, VDDA and VDDP together at the external 5V rail, thus improving overall efficiency. An internal undervoltage lock-out circuit (UVLO) monitors the level of VDDA.

VDDP is the power supply rail for the gate drivers and bootstrap circuit. This pin is subject to high-current spike with high-frequency content. To prevent these from polluting the analog VDDA supply, a separate capacitor is needed for VDDP pin bypassing.

An internal 10Ω resistor is provided between VDDA and VDDP allowing a switching noise attenuation RC filter with the minimum amount of external components to be implemented. It is possible − although typically not necessary − to lower the RC time constant by connecting an external resistor between VDDA and VDDP.

Enable/Delay (EN/DLY)

EN/DLY is a dual-threshold pin that turns the internal LDO ON/OFF and starts/stops the power delivery to the output. This is shown in Figure 1:
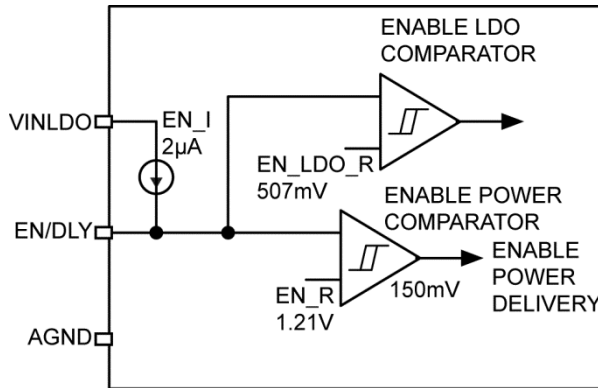
Figure 1. EN/DLY Pin Functionality

The threshold for power delivery (EN_R) is a precise 1.21V ±70mV. A 150mV typical hysteresis prevents chattering due to switching noise and/or slow edges.

A 2µA typical pull-up current with ±1µA accuracy permits the implementation of a start-up delay by means of an external capacitor. In this case, it is necessary to use an open-drain driver to disable the MIC24046-H while maintaining the start-up delay function.

Inductor (LX) and Bootstrap (BST)

The external inductor is connected to LX. The high-side MOSFET driver circuit is powered between BST and LX by means of an external capacitor (typically 100nF) that is replenished from rail VDDP during the low-side MOSFET ON-time. The bootstrap diode is internal.

Output Sensing (OUTSNS) and Compensation (COMP)

OUTSNS should be connected exactly to the desired point-of-load regulation avoiding parasitic resistive drops. The impedance seen into OUTSNS is high (tens of kΩ), therefore its loading effect is typically negligible. OUTSNS is also used by the slope compensation generator.

COMP is the connection for the external compensation network. COMP is driven by the output of the transconductance error amplifier. Care must be taken to return the compensation network ground directly to AGND.

Soft-Start

The MIC24046-H internal reference is ramped up at a 0.45V/ms rate. Note that this is the internal reference soft-start slew rate and that the actual slew rate seen at the output should take into account the internal divider attenuation as detailed in the *Application Information* section.

Switching Frequency (FREQ)

The MIC24046-H features three different selectable switching frequencies: 400kHz, 565kHz, and 790kHz.

Pre-Biased Output Start-Up

The MIC24046-H is designed to achieve safe start-up into a pre-biased output without discharging the output capacitors.

Thermal Shutdown

The MIC24046-H has thermal-shutdown protection that prevents operation at excessive temperature. The thermal-shutdown threshold is typically set at 160°C with a hysteresis of 25°C.

Overcurrent Protection (ILIM) and Hiccup Mode Short-Circuit Protection

The MIC24046-H features instantaneous cycle-by-cycle current limit with current sensing both on the low-side and high-side switches, and hiccup mode for prolonged overloads or short-circuit conditions.

Low-side cycle-by-cycle protection detects the current level of the inductor current during the low-side MOSFET ON time. The high-side MOSFET turn-on is inhibited as long as the low-side MOSFET current limit is above the current-limit threshold level. The inductor current will continue decaying until the current falls below the threshold, then the high-side MOSFET will be enabled again according to the duty cycle requirement from the PWM modulator. The mechanism is illustrated in Figure 2.
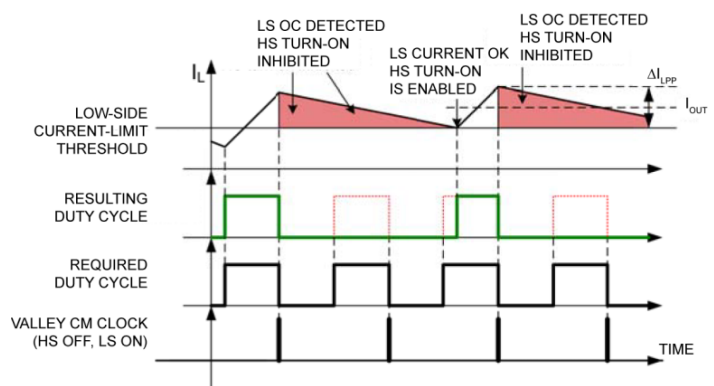

Figure 2. Low-Side Cycle-by-Cycle Current-Limit Action

The low-side current limit is programmable at three different levels (3A, 4A, and 5A loads), in order to fit different application requirements. Note that since the low-side current limit acts on the valley current, the DC output current level I_{OUT} at which the low-side cycle-by-cycle current limit is engaged is higher than the current limit value by an amount equal to $\Delta IL_{PP}/2$, where ΔIL_{PP} is the peak-to-peak inductor ripple current.

The high-side current limit is approximately $1.4 - 1.5$ times bigger than the low-side current limit (typical values). The high-side cycle-by-cycle current limit immediately truncates the high-side ON time without waiting for the OFF clocking event.

A leading-edge-blanking (LEB) timer (108ns, typical) is provided on the high-side cycle-by-cycle current limit to mask switching noise and to prevent false triggering of the protection. Before the LEB timer has expired, high-side cycle-by-cycle current limit action cannot take place.

Hiccup mode protection reduces power dissipation in permanent short circuit conditions. On each clock cycle at which a low-side cycle-by-cycle current limit event is detected, a 4-bits up/down counter is incremented. On each clock cycle without a concurrent low-side current limit event, the counter is decremented or left at zero (counter cannot wrap-around below 0000 and above 1111). Note that high-side current limit events do not increment the counter, only low-side current limit event detections do.

If the counter reaches 1111 (15 events), then the high- and low-side MOSFETs are tri-stated and power delivery to the output is inhibited for the duration of 3x the soft-start time. This digital integration mechanism provides immunity to momentary overloading of the output. After the wait time, the MIC24046-H retries entering operation and initiates a new soft-start sequence.

The flowchart of Figure 3 illustrates the hiccup mode short-circuit protection logic flow. Note that hiccup mode short-circuit protection is active at all times, including the soft-start ramp.
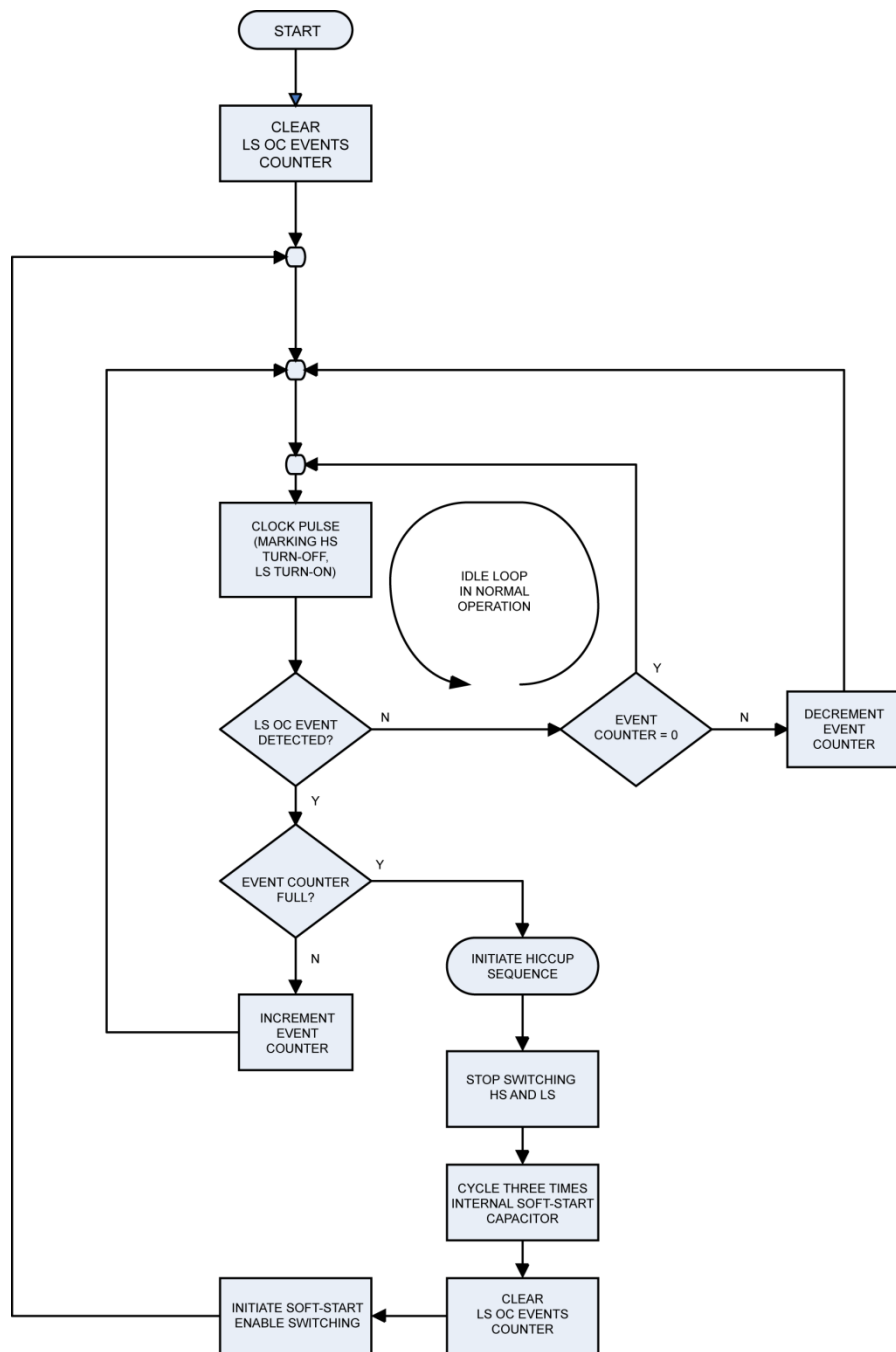
Figure 3. Hiccup Mode Short-Circuit Protection Logic

Application Information

Programming Start-Up Delay and External UVLO

The EN/DLY pin allows programming of an external start-up delay. In this case, the driver for the EN/DLY pin should be an open-drain/open-collector type as shown in Figure 4:
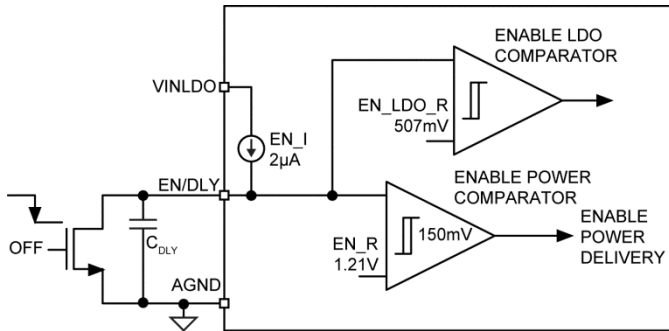

Figure 4. Programmable Start-Up Delay Function

The start-up delay is the delay time from the OFF falling edge to the assertion of the enable power delivery signal and can be calculated as shown in Equation 1:

$$t_{SU\_DLY} = \frac{EN\_R \times C_{DLY}}{EN\_I} \qquad \text{Eq. 1}$$

where:

EN_R = 1.21V

EN_I = 2µA

C_{DLY} = Delay programming external capacitor

The EN/DLY pin can also be used to program an UVLO threshold for power delivery by means of an external resistor divider, as described in the following Figure 5.
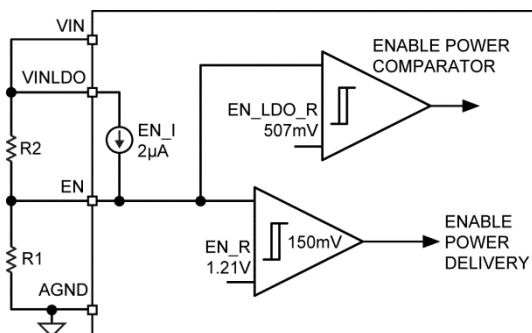
Figure 5. Programmable External UVLO Function

The programmed V_{IN} UVLO threshold V_{IN_RISE} is given by:

$$V_{IN\_RISE} = EN\_R \times \left(1 + \frac{R2}{R1}\right) - EN\_I \times R2 \qquad \text{Eq. 2}$$

where:

EN_R = 1.21V

EN_I = 2µA

R1 and R2 = External resistors.

To desensitize the V_{IN} UVLO threshold against variations of the pull-up current EN_I, it is recommended to run the R1 − R2 voltage divider at a significantly higher current level than the EN_I current.

The corresponding V_{IN} UVLO hysteresis VIN_HYS is calculated as follows:

$$V_{IN\_HYS} = 150mV \cdot \left(1 + \frac{R2}{R1}\right) \qquad \text{Eq. 3}$$

Similar calculations also apply to the internal LDO activation threshold.

Setting the Switching Frequency

The MIC24046-H switching frequency can be programmed using FREQ as shown in Table 1:

Table 1. Switching Frequency Settings

FREQ	Frequency
Hi-Z (open)	400 kHz
0 (GND)	565 kHz
1 (VDDA)	790 kHz

Setting the Output Voltage

The MIC24046-H output voltage can be programmed by means of VOSET0, VOSET1 as shown in Table 2.

Table 2. Output Voltage Settings

VOSET1	VOSET0	Output Voltage
0 (GND)	0 (GND)	3.3V
0 (GND)	1 (VDDA)	2.5V (2.49V)
1 (VDDA)	0 (GND)	1.8V
1 (VDDA)	1 (VDDA)	1.5V
0 (GND)	Hi-Z (Open)	1.2V
Hi-Z (Open)	0 (GND)	1.0V
1 (VDDA)	Hi-Z (Open)	0.9V
Hi-Z (Open)	1 (VDDA)	0.8V
Hi-Z (Open)	Hi-Z (Open)	0.7V

To achieve accurate output voltage regulation, the OUTSNS pin (internal feedback divider top terminal) shall be Kelvin-connected as close as possible to the point-of-regulation top terminal. Also, since both the internal reference and the internal feedback divider bottom terminal are referred to AGND, it is important to minimize voltage drops between the AGND and the point-of-regulation return terminal.

Setting the Current Limit

The MIC24046-H valley-mode current limit on the low-side MOSFET can be programmed by means of ILIM as shown in Table 3.

Table 3. Current-Limit Setting

ILIM	Low-Side Valley Current Limit (Typical Value)	Rated Output Current
0 (GND)	4.6 A	3A
1 (VDDA)	6.2 A	4A
Hi-Z (Open)	6.8 A	5A

Note that the programmed current-limit values act as pulse-by-pulse current-limit thresholds on the valley inductor current. If the inductor current has not decayed below the threshold at the time the PWM requires a new ON time, the high-side MOSFET turn-on is either delayed until the valley current recovers below the threshold or skipped. Each time the high-side MOSFET turn-on is skipped, a 4-bit up-down counter is incremented. When the counter reaches the configuration 1111, a hiccup sequence is invoked in order to reduce power dissipation under prolonged short-circuit conditions.

The highest current-limit setting (6.8A) is intended to comfortably accommodate a 5A application.

Ensure the maximum operating junction temperature is not exceeded in high output power applications.

Inductor Selection

When selecting an inductor, it is important to consider the following factors:

- Inductance
- Rated current value
- Size requirements
- DC resistance (DCR)
- Core losses

The inductance value is critical to the operation of MIC24046-H. Since the MIC24046-H is a valley current-mode regulator, it needs slope compensation for stable current loop operation at duty cycles below 50%. Slope compensation is internally added according to the frequency and output voltage selection, assuming a minimum inductance value for the given operating condition. According to this assumption, the minimum inductor values recommended for stable current loop operation are listed in Table 4. Note that the minimum suggested inductance values should be met when taking into account inductor tolerance and its change with bias level.

Table 4. Recommended Inductance Values at V_{IN} = 12V

V_{OUT} SELECTION	FREQUENCY	MINIMUM INDUCTANCE
0.7V, 0.8V, 0.9V, 1.0V, 1.2V	400kHz	0.97
	565kHz	0.68
	790kHz	0.49
1.5V, 1.8V	400kHz	1.51
	565kHz	1.06
	790kHz	0.76
2.49V, 3.3V	400kHz	2.42
	565kHz	1.70
	790kHz	1.21

Slope compensation is also internally adapted to input voltage, however higher inductance values than those listed in Table 4 may be required to maintain current loop stability, especially at the lower end of the input voltage range (4.5V to 8V).

Inductor current ratings are generally given in two methods: permissible DC current, and saturation current. Permissible DC current can be rated for a 20°C to 40°C temperature rise. Saturation current can be rated for a 10% to 30% loss in inductance. Make sure that the nominal current of the application is well within the permissible DC current ratings of the inductor, also depending on the allowed temperature rise. Note that the inductor permissible DC current rating typically does not include inductor core losses. These are a very important contribution to the total inductor core loss and temperature increase in high-frequency DC-to-DC converters, since core losses increase rapidly with the excitation frequency.

When saturation current is specified, make sure that there is enough design margins, so that the peak current does not cause the inductor to enter deep saturation.

Also pay attention to the inductor saturation characteristic in current limit. The inductor should not heavily saturate even in current limit operation, otherwise the current might instantaneously run away and reach potentially destructive levels. Typically, ferrite-core inductors exhibit an abrupt saturation characteristic, while powdered-iron or composite inductors have a soft-saturation characteristic. Peak current can be calculated as illustrated in Equation 4:

$$I_{L,PEAK} = \left[I_O + V_O \left(\frac{1 - V_O/V_{IN}}{2 \times f \times L} \right) \right] \qquad \text{Eq. 4}$$

As shown in Equation 4, the peak inductor current is inversely proportional to the switching frequency and the inductance. The lower the switching frequency or inductance, the higher the peak current. As input voltage increases, the peak current also increases.

Output Capacitor Selection

Two main requirements determine the size and characteristics of the output capacitor C_O:

• Steady-state ripple
• Maximum voltage deviation during load transient

For steady-state ripple calculation, the ESR and the capacitive ripple both contribute to the total ripple amplitude.

From the switching frequency, input voltage, output voltage setting, and load current the peak-to-peak inductor current ripple and the peak inductor current can be calculated as:

$$\Delta I_{L\_PP} = V_O \left(\frac{1 - V_O/V_{IN}}{f_S \times L} \right) \qquad \text{Eq. 5}$$

$$I_{L,PEAK} = I_O + \frac{\Delta I_{L\_PP}}{2} \qquad \text{Eq. 6}$$

The capacitive ripple $\Delta V_{R,\,C}$ and the ESR ripple $\Delta V_{R,\,ESR}$ are given by:

$$\Delta V_{R,C} = \frac{\Delta I_{L\_PP}}{8 \times f_s \times C_O} \qquad \text{Eq. 7}$$

$$\Delta V_{R,ESR} = ESR \times \Delta I_{L\_PP} \qquad \text{Eq. 8}$$

The total peak-to-peak output ripple is then conservatively estimated as:

$$\Delta V_R \cong \Delta V_{R,C} + \Delta V_{R,ESR} \qquad \text{Eq. 9}$$

Choose the output capacitor value and ESR such that ΔV_R is within specifications. Capacitor tolerance should be considered for worst case calculations. In case of ceramic output capacitors, also take into account the decrease of effective capacitance versus applied DC bias.

The worst-case load transient for output capacitor calculation is an instantaneous 100% to 0% load release when the inductor current is at its peak value. In this case, all the energy stored in the inductor is absorbed by the output capacitor while the converter stops switching and keeps the low-side FET ON.

The peak output voltage overshoot ΔV_{OUT} happens when the inductor current has decayed to zero, and can be calculated as in Equation 10:

$$\Delta V_O = \sqrt{V_O^2 + \frac{L}{C_O}I_{L,PEAK}^2} - V_O \qquad \text{Eq. 10}$$

The minimum output capacitance value $C_{O(MIN)}$ needed to limit the output overshoot below ΔV_{OUT} is:

$$C_{O(MIN)} = \frac{L \times I_{L,PEAK}^2}{(\Delta V_O + V_O)^2 - V_O^2} \qquad \text{Eq. 11}$$

The latter turns out to be the most stringent requirement on capacitor value in most applications. Low equivalent series resistance (ESR) ceramic output capacitors with X5R or X7R temperature characteristics are recommended.

For low output voltage applications with demanding load transient requirements, it is often more convenient to use a combination of polarized and ceramic output capacitors for smallest solution size.

Input Capacitor Selection

Two main requirements determine the size and characteristics of the input capacitor:

- Steady-state ripple
- RMS current

The buck converter input current is a pulse train with very fast rising and falling times so low-ESR ceramic capacitors are recommended for input filtering, because of their good high-frequency characteristics.

For ideal input filtering (assuming a DC input current feeding the filtered buck power stage), and by neglecting the capacitor ESR contribution to the input ripple (typically possible for ceramic input capacitors), the minimum capacitance value $C_{IN(MIN)}$ needed for a given input peak-to-peak ripple voltage $\Delta V_{r, IN}$ can be estimated as shown in Equation 12:

$$C_{IN(MIN)} = \frac{I_O \times D \times (1-D)}{\Delta V_{r,IN} \times f_S} \qquad \text{Eq. 12}$$

where:

D is the duty cycle at the given operating point.

The RMS current $I_{IN,RMS}$ of the input capacitor is estimated as in Equation 13:

$$I_{IN, RMS} = I_O \times \sqrt{D \times (1-D)} \qquad \text{Eq. 13}$$

Note that for a given output current I_O, the worst case values are obtained at D = 0.5.

Multiple input capacitors can be used to reduce input ripple amplitude and/or individual capacitor RMS current.

Compensation Design

As a simple first-order approximation, the valley-current-mode-controlled buck power stage can be modeled as a voltage-controlled current-source feeding the output capacitor and load. The inductor current state-variable is removed and the power-stage transfer function from COMP to the inductor current is modeled as a transconductance (Gm_{PS}). The simplified model of the control loop is shown in *Figure 6*. The power-stage transconductance Gm_{PS} shows some dependence on current levels and it is also somewhat affected by process variations, therefore some design margin is recommended against the typical value Gm_{PS} = 12.5 A/V (see *Electrical Characteristics*).
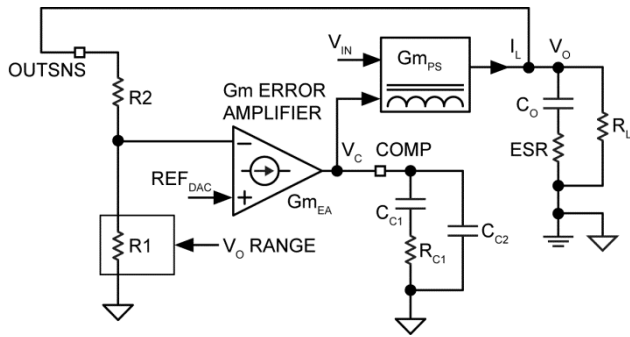
**Figure 6. Simplified Small-Signal Model
of the Voltage Regulation Loop**

This simplified approach disregards all issues related to the inner current loop, like its stability and bandwidth. This approximation is good enough for most operating scenarios, where the voltage-loop bandwidth is not pushed to aggressively high frequencies.

Based on the model shown in Figure 6, the control-to-output transfer function is:

$$G_{CO(S)} = \frac{V_{O(S)}}{V_{C(S)}} = Gm_{PS} \times R_L \times \frac{\left(1 + \frac{s}{2\pi \times f_Z}\right)}{\left(1 + \frac{s}{2\pi \times f_P}\right)} \qquad \text{Eq. 14}$$

where:

f_Z and f_P = The frequencies associated with the output capacitor ESR zero and with the load pole, respectively:

$$f_Z = \frac{1}{2\pi \times C_O \times ESR} \qquad \text{Eq. 15}$$

$$f_P = \frac{1}{2\pi \times C_O \times (ESR + R_L)} \qquad \text{Eq. 16}$$

The MIC24046-H uses a transconductance (Gm_{EA} = 1.5mA/V) error amplifier. Frequency compensation is implemented with a Type-II network (R_{C1}, C_{C1}, and C_{C2}) connected from COMP to AGND. The compensator transfer function consists of an integrator for zero DC (voltage regulation error), of one zero to boost the phase margin of the overall loop gain around the crossover frequency and one additional pole that can be used to cancel the output capacitor ESR zero, or to further attenuate switching frequency ripple. In both cases, the additional pole makes the regulation loop less susceptible to switching frequency noise. The additional pole is created by capacitor C_{C2}. The compensator transfer function $H_{C(S)}$ (from OUTSNS to COMP) is as Equation 17:

$$H_{C(S)} = -\frac{R1}{R1+R2} \times Gm_{EA} \times \frac{1}{S \times (C_{C1} + C_{C2})}$$
$$\times \frac{(1 + S \times R_{C1} \times C_{C1})}{\left(1 + S \times R_{C1} \times \frac{C_{C1} \times C_{C2}}{C_{C1} + C_{C2}}\right)} \qquad \text{Eq. 17}$$

The overall voltage loop gain $T_{V(S)}$ is the product of the control-to-output and of the compensator transfer functions:

$$T_{V(S)} = G_{CO(S)} \times H_{C(S)} \qquad \text{Eq. 18}$$

The value of the attenuation ratio R1/(R1 + R2) depends on the output voltage selection, and can be retrieved as illustrated in Table 5:

Table 5. Internal Feedback Divider Attenuation Values

V_O Range	R1/(R1 + R2)	A (A = 1 + R2/R1)
0.7V – 1.2V	1	1
1.5V – 1.8V	0.5	2
2.5V(2.49V) – 3.3V	0.333	3

The procedure for compensation design follows these steps:

1. Set the $T_{V(S)}$ loop gain crossover frequency f_{XO} in the range $f_S/20$ to $f_S/10$. Lower values of f_{XO} permit a more predictable and robust phase margin. Higher values of f_{XO} would involve additional considerations about the current loop bandwidth in order to achieve a robust phase margin, therefore a more conservative approach is highly recommended:

$$f_{XO} \approx \frac{f_S}{20} \qquad \text{Eq. 19}$$

2. Select R_{C1} to achieve the target crossover frequency f_{XO} of the overall voltage loop. This typically happens where the power stage transfer function $G_{CO(S)}$ is rolling off at -20dB/dec. The compensator transfer function $H_{C(S)}$ is in the so-called mid-band gain region where C_{C1} can be considered a DC-blocking short circuit while C_{C2} can still be considered as an open circuit, as illustrated in Equation 20:

$$R_{C1} = \left(\frac{R1+R2}{R1} \right) \cdot \frac{2\pi \times C_O \times f_{XO}}{Gm_{EA} \cdot Gm_{PS}} \qquad \text{Eq. 20}$$

3. Select capacitor C_{C1} to place the compensator zero at the load pole. The load pole moves around with load variations, so to calculate the load pole use as a load resistance R_L the value determined by the nominal output current I_O of the application, as shown in Equation 21 and Equation 22:

$$R_L = \frac{V_O}{I_O} \qquad \text{Eq. 21}$$

$$C_{C1} = \frac{C_O \times (ESR + R_L)}{R_{C1}} \qquad \text{Eq. 22}$$

4. Select capacitor C_{C2} to place the compensator pole at the frequency of the output capacitor ESR zero, or at $\geq 5\ f_{XO}$, whichever is lower.

C_{C2} is intended to place the compensator pole at the frequency of the output capacitor ESR zero, and/or to achieve additional switching ripple/noise attenuation.

If the output capacitor is a polarized one, its ESR zero will typically occur at low enough frequencies to cause the loop gain to flatten out and not roll-off at a -20 dB/decade slope around or just after the crossover frequency f_{XO}. This is undesirable, because of scarce compensation design robustness, and because of switching noise susceptibility. The compensator pole is then used to cancel the output capacitor ESR zero and to achieve a well-behaved roll-off of the loop gain above the crossover frequency.

If the output capacitors are only ceramic ones, their ESR zeroes frequencies could be very high (in many cases even above the switching frequency itself). Loop gain roll-off at -20dB/decade well beyond the crossover frequency is ensured, but even in this case, it is good practice to still make use of the compensator pole to further attenuate switching noise, while conserving phase margin at the crossover frequency. For example, setting the compensator pole at $5\ f_{XO}$, will limit its associated phase loss at the crossover frequency to about $11°$. Placement at even higher frequencies $N \times f_{XO}$ ($N > 5$) will reduce phase loss even further, at the expense of less noise/ripple attenuation at the switching frequency. Some attenuation of the switching frequency noise/ripple is achieved as long as $N \times f_{XO} < f_S$.

For polarized output capacitor, compensator pole placement at the ESR zero frequency is achieved shown in Equation 23:

$$C_{C2} = \frac{1}{\dfrac{R_{C1}}{C_O \times ESR} - \dfrac{1}{C_{C1}}} \qquad \text{Eq. 23}$$

For ceramic output capacitor, compensator pole placement at $N \times f_{XO}$ ($N \geq 5$, $N \times f_{XO} < f_S$) is achieved as detailed in Equation 24:

$$C_{C2} = \frac{1}{2\pi \times R_{C1} \times N \times f_{XO} - \dfrac{1}{C_{C1}}} \qquad \text{Eq. 24}$$

Output Voltage Soft-Start Rate

The MIC24046-H features internal analog soft-start, such that the output voltage can be smoothly increased to the target regulation voltage. The soft-start rate given in the *Electrical Characteristics* is referred to the error amplifier reference, and therefore the effective soft-start rate value seen at the output of the module has to be scaled according to the internal feedback divider attenuation values listed in Table 5. To calculate the effective output voltage soft-start slew rate SS_SR_{OUT} based on the particular output voltage setting and the reference soft-start slew rate SS_SR, use the following formula:

$$SS\_SR_{OUT} = A \cdot SS\_SR \qquad \text{Eq. 24}$$

Where:

The value of A (amplification, A =1 + R2/R1) is given in the right column of Table 5.

Typical Application Schematic

Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1	GRM31CR61E226ME15	Murata[6]	X5R, 22µF 25V 20%, Size 1206 Capacitor	1
C2, C7	GRM155R71E104KE14	Murata	X7R, 100nF 25V 10%, Size 0402 Capacitor	2
C3, C4	GRM31CR60J107ME39	Murata	X5R, 100uF 6.3V 20%, Size 1206 Capacitor	
C5, C6	GRM155R61C225KE11	Murata	X5R, 2.2µF 16V 10%, Size 0402 Capacitor	2
C8	GRM1555C1H470JA01	Murata	C0G, 47pF 50V 5%, Size 0402 Capacitor	1
C9	GRM155R71E103KA01	Murata	X7R, 10nF 25V 10%, Size 0402 Capacitor	1
R1	RC0402-2551F	ANY	Chip, 2.55kΩ 1%, Size 0402 Resistor	1
L1	XAL4020-152ME	Coilcraft[7]	SMT, 1.5µH, I_{SAT} = 7.1A I_{RMS} = 5.2A Inductor	1
U1	**MIC24046-HYFL**	**Micrel, Inc.[8]**	**Pin-Programmable, 4.5V – 19V, 5A Step-Down Converter**	**1**

Notes:

6. Murata: www.murata.com.

7. Coilcraft: www.coilcraft.com.

8. **Micrel, Inc.:** www.micrel.com.

PCB Layout Recommendations
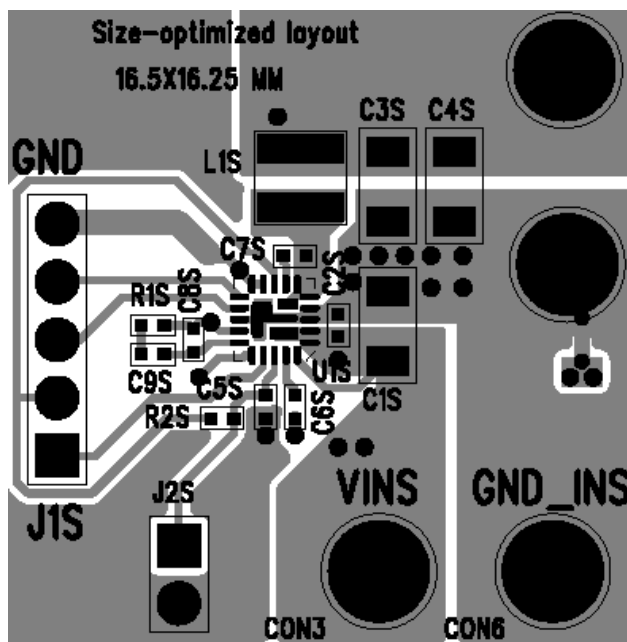
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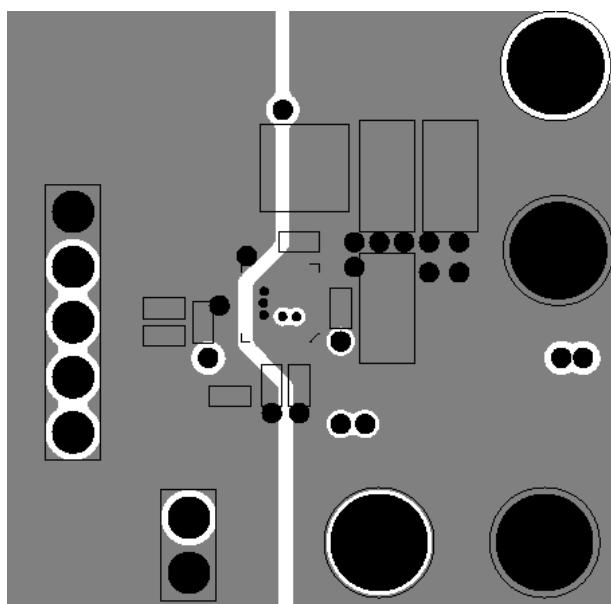
Layer 1

PCB Layout Recommendations (Continued)
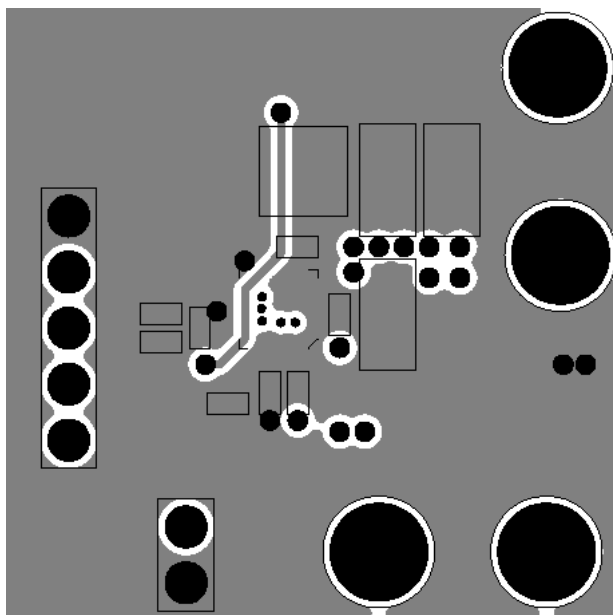
Layer 2
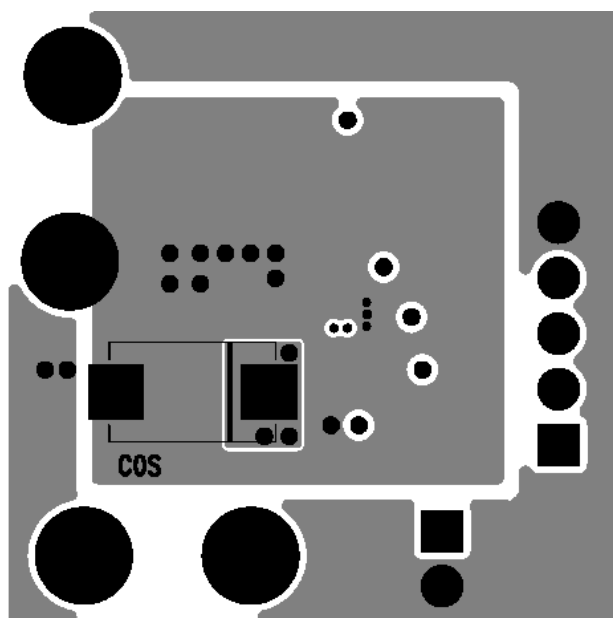
Bottom Layer

Package Information and Recommended Landing Pattern[9]

TOP VIEW
NOTE: 1, 2, 3

BOTTOM VIEW
NOTE: 1, 2, 3

SIDE VIEW
NOTE: 1, 2, 3

RECOMMENDED LAND PATTERN
NOTE: 4, 5, 6, 7
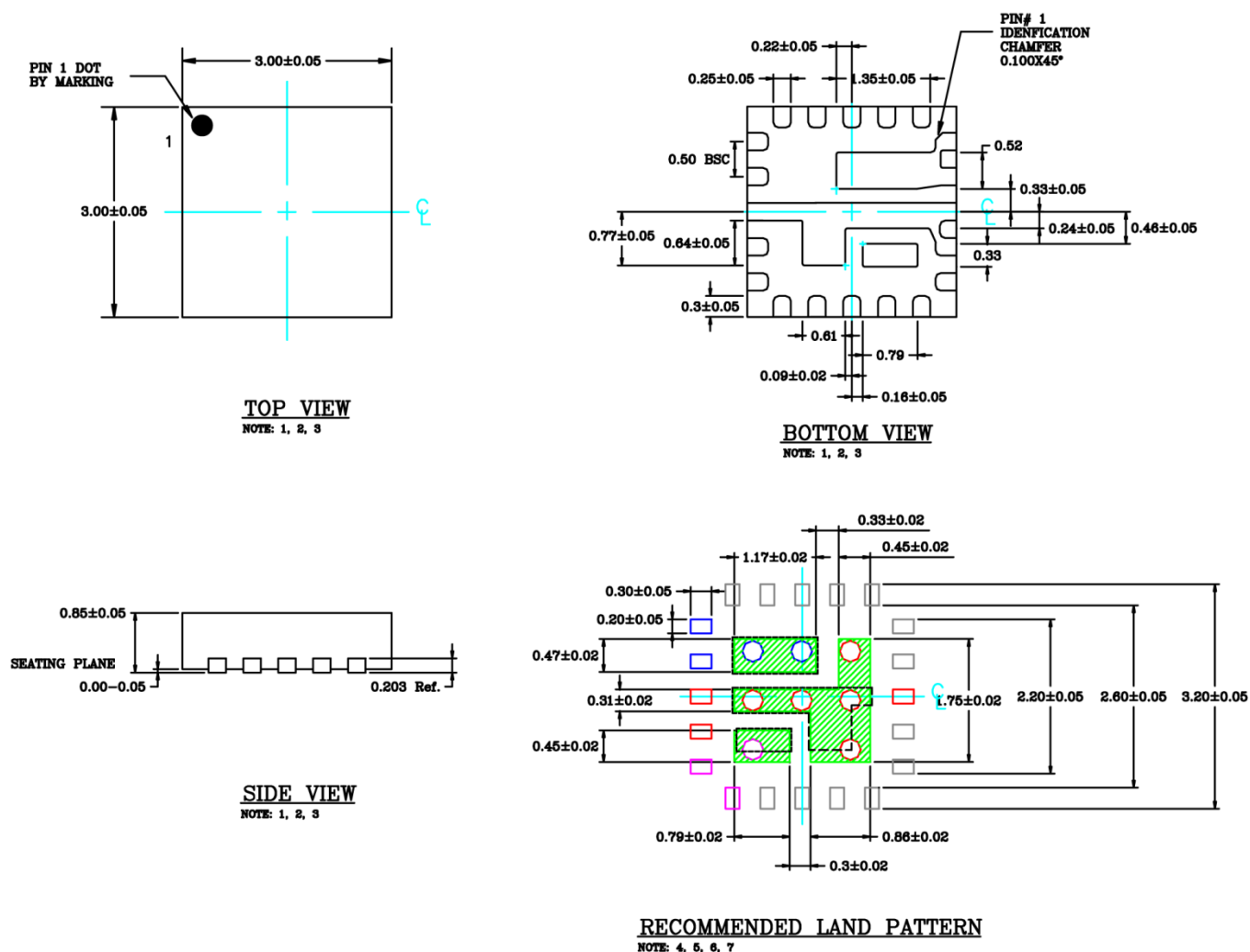
NOTE:
1. MAX PACKAGE WARPAGE IS 0.05mm.
2. MAX ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
3. PIN #1 (TOP) IS LASER MARKED.
4. RED CIRCLES IN LAND PATTERN REPRESENTS THERMAL VIA AND SHOULD BE CONNECTED TO GROUND FOR MAXIMUM PERFORMANCE.
5. GREEN RECTANGLES (SHADED AREA) ARE RECOMMENDED SOLDER STENCIL OPENNING ON EXPOSED PAD AREA.
6. BLUE COLOR AND PURPLE COLOR PADS REPRESENT DIFFERENT POTENTIALS. DO NOT CONNECT TO GROUND.
7. VIA SIZE is 0.30mm DIAMETER and 0.70mm PITCH.

20-Pin 3mm × 3mm QFN (FL)

Note:

9. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.