KSZ9692PB User Guide Brief

KSZ9692PB Evaluation Platform Rev 2.0

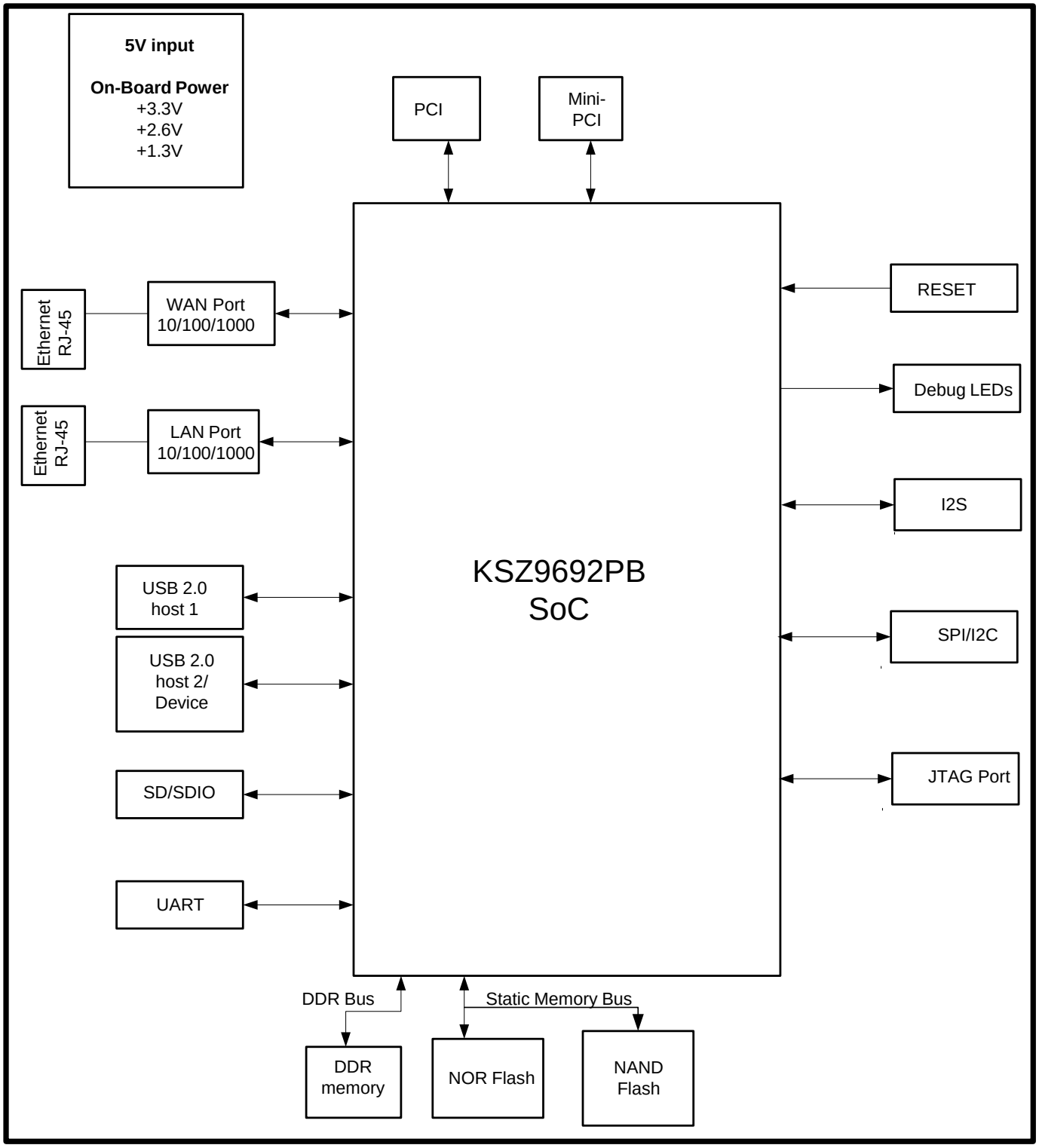
General Description

The KSZ9692PB Evaluation Platform accelerates product time-to-market by providing a hardware platform for proof-of-concept, software development, and product demonstration.

Features

- KSZ9692PB as System-on-Chip (SoC)
- 64MB of embedded DDR memory
- 8MB of embedded NOR Flash Memory
- Place-Holder for embedded NAND Flash Memory
- WAN 10/100/1000 Ethernet Port
- LAN 10/100/1000 Ethernet Port
- One standard PCI interface edge connector
- One Mini-PCI interface Type III connector
- Two standard USB 2.0 interface connectors
- SD/SDIO interface connector
- One UART DB-9 Connector
- Onboard jumper header for I2S interface
- Onboard jumper header for SPI/I2C interface
- Onboard jumper header for four GPIO interface
- Two GPIO controlled LEDs for S/W assist debug/development
- JTAG port for S/W development

Block Diagram



KSZ9692PB Evaluation Platform Block Diagram

Revision History

Revision	Date	Summary of Changes
2.0	7/28/09	Initial Release

Content

Evaluation Board Description

This User Guide Brief is a summary of the features and interfaces supported by KSZ9692PB evaluation board Rev 2.0.

Chip Select Assignments

KSZ9692 Chip Select Signal	KSZ9692 Pin #	Device
CSN0	U14	DDR Bank
RCSN0	L1	NOR FLASH Bank 0
RCSN1	K3	NOR FLASH Bank 1 (Not assigned)
NCEN0	V3	NAND FLASH Bank 0
NCEN1	T3	NAND FLASH Bank 1 (Not assigned)
ECSN0	M2	External I/O Bank 0 (Not assigned)
ECSN1	N1	External I/O Bank 1 (Not assigned)
ECSN2	L3	External I/O Bank 2 (Not assigned)

Table 1. Chip Select Assignments

DDR Memory

The evaluation board provides 64MB of DDR memory with a single Micron MT46V32M16-5B device (location U14) in a 32Mx16 bit configuration. This is DDR bank normal configuration.

Note: a second Micron MT46V32M16-5B device resides in location U15 for 32Mx32 configuration. This is for engineering test only. DDR 32-bit data width is not supported for normal operation.

NOR Flash Memory

The evaluation board provides 8MB of NOR flash memory. The part number is Spansion S29GL064N90. This device is a 4Mx16 bit configuration and mounted directly onto board at U4 location. The evaluation board is configured to boot from NOR flash.

NAND Flash Memory

The evaluation board provides a place holder for NAND flash memory at location U11. The user can solder NAND flash of their choice at this location.

PCI Interface

The evaluation board provides one standard PCI edge connector and one mini-PCI type III connector to allow for applications using existing PCI based peripherals.

The PCI interface supports 33/66MHz and is compliant with PCI Local Bus Specification 2.3. The voltages supplied to the connectors are 3.3V and 5.0V. ± 12V supply is not available.

WAN Interface

The WAN MAC of KSZ9692PB is interfaced to Micrel KSZ9021RL PHY via RGMII bus. RJ-45 connector at location RJ2 provides network connectivity at 10/100/1000 BASE-TX. There are two onboard LEDs associated with WAN port as following:

LED Location	Designation	Description
D13	LINK	Link partner establishment
D12	ACTIVITY	Network traffic activity

Table 2. WAN Port LED Description

LAN Interface

The LAN MAC of KSZ9692PB is interfaced to Micrel KSZ9021RL PHY via RGMII bus . RJ-45 connector at location RJ1 provides network connectivity at 10/100/1000 BASE-TX. There are two onboard LEDs associated with LAN port as following:

LED Location	Designation	Description
D11	LINK	Link partner establishment
D10	ACTIVITY	Network traffic activity

Table 3. LAN Port LED Description

USB Interfaces

The evaluation board provides two standard USB 2.0 host ports to allow connectivity to USB based peripherals. Each port is individually associated with 5V supply peripheral power switch (Micrel MIC2015) to power-up external peripherals. Port1 and port2 are located at JP7 and JP5 connectors respectively.

Port2 is configurable as device. To configure Port2 as device, R41 must be installed with a 0 ohm value resistor. Port2 as device is self-powered and does not need external power. Therefore external 5V power to Port2 connector must not be applied.

SD/SDIO Interface

The evaluation board provides a standard SD/SDIO host port to allow connectivity to SD/SDIO based peripherals. The SD/SDIO port is located at JP4.

I2S Interface

The evaluation board provides I2S interface at JP3 header to allow connectivity to I2S based peripherals such as an audio CODEC. The following table is map of I2S signals:

KSZ8692PB I2S Signal	JP3 Pin Assignment
SDI	1
SDO	2
LRCLK	3
BCLK	4
MCLK	5
GND	6

Table 4. I2S Interface Description

SPI/I2C Interface

The evaluation board provides SPI and I2C interface bus at JP1 header to allow connectivity to SPI or I2C-based peripherals. The following table is map of SPI/I2C signals:

KSZ8692PB SPI/I2C Signal	JP1 Pin Assignment
CS	1
RDY	2
MISO	3
MOSI/SDA	4
CK/SCL	5
GND	6

Table 5. SPI/I2C Interface Description

GPIO Interface

The evaluation board provides direct access to KSZ9692PB GPIO[7:4] pins at JP6. The following table is map of

GPIO pins:

KSZ8692PB SPI/I2C Signal	JP6 Pin Assignment
GPIO4	1
GPIO5	2
GPIO6	3
GPIO7	4
NC	5
GND	6

Table 6. GPIO[7:4] Interface Description

UART

The evaluation board provides a high speed UART interface. The UART port1 implements Maxim MAX3243 as RS232 transceiver and supports up to 120kbps. The UART interface is a male DB9, null-modem connector for use as a console port. This port also supports modem control signals.

Connector Pin No.	KSZ9692 Signal Name	KSZ9692PB I/O	KSZ9692PB Signal Description
1	UDCDN	I	UART Data Carrier Detect
2	URXD	I	UART Receive Data
3	UTXD	O	UART Transmit Data
4	UDTRN	O	Data Terminal Ready (active low)
5	N/A	N/A	Ground
6	UDSRN	I	UART Data Set Ready
7	URTSN	O	UART Request To Send
8	UCTSN	I	Clear To Send
9	URIN	I	Ring Indicator

Table 7. UART Interface Description

Multi-ICE/JTAG Connector

The KSZ9692PB JTAG interface located at JP8 header is a standard 20-pin connector for the Multi-ICE. This connector can be used to download code to flash and for software development and debugging purposes.

LEDs

The evaluation board provides two user LEDs to assist with software debug and development. These LED indicators are controlled by KSZ9692PB GPIO[9:8] pins. A logic low of an individual GPIO turns the associated LED ON and logic high turns it OFF. The following table is map of GPIO versus LED:

LED Location	GPIO Assignment
D9	GPIO8
D8	GPIO9

Table 8. User LED Description

Reset

The evaluation board implements reset at location S1 push-button. By pressing this push-button momentarily, the board experiences hard reset.

Power and Ground

Power to the evaluation board is supplied through a 5.0V DC power jack at J2 connector. The 5.0V DC power is then

converted down to the three voltage levels (1.3V, 3.3V, 2.6V) required by KSZ9692PB. The following table outlines onboard derived voltages and test points:

Voltages	Micrel Part	Test Points
V1.3 (Digital & Analog Core)	MIC4724	TP2
V3.3 (Digital & Analog Core)	MIC2193	TP1, TP5
V2.6 (Digital DDR memory)	MIC49300 (see Note 1)	TP7
GND		TP3, TP4, TP9, TP10, TP11, TP12

Table 9. Voltages and Test Points

The evaluation board features a power LED indicator at location D4 (next to power jack) so that the user may easily determine if the board is powered.

The evaluation board power consumption is typically 5V @ 1.4A with both WAN and LAN ports linked at 1000 Mbps to their respective link partners. It is recommended to use a DC power supply rated for 5VDC @ 4A. Care must be taken to insure this supply is well regulated and noise free.

Note 1: DDR device Micron MT46V32M16-5B requires 2.6V supply (See Micron Electrical Specification). MIC49300 is adjusted from 2.5V to 2.6V to meet this requirement.

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