

## 32-Channel Serial To Parallel Converter With High Voltage Push-Pull Outputs

### Ordering Information

| Device | Recommended<br>Operating<br>$V_{PP}$ max | Package Options                           |                                        |
|--------|------------------------------------------|-------------------------------------------|----------------------------------------|
|        |                                          | 44 J-Lead<br>Quad Plastic<br>Chip Carrier | Dice in<br>Waffle Pack<br>Chip Carrier |
| HV9308 | 80V                                      | HV9308PJ                                  | HV9308X                                |
| HV9408 | 80V                                      | HV9408PJ                                  | HV9408X                                |

### Features

- ❑ Processed with HVCMOS® technology
- ❑ Low power level shifting
- ❑ Shift register speed 8MHz
- ❑ Latched data outputs
- ❑ 5V CMOS compatible inputs
- ❑ Forward and reverse shifting options
- ❑ Diode to  $V_{PP}$  allows efficient power recovery
- ❑ 44-lead ceramic surface mount package
- ❑ Hi-Rel processing available

### Absolute Maximum Ratings<sup>1</sup>

|                                                                |                         |
|----------------------------------------------------------------|-------------------------|
| Supply voltage, $V_{DD}$ <sup>2</sup>                          | -0.5V to +7V            |
| Supply voltage, $V_{PP}$ <sup>2</sup>                          | -0.5V to +90V           |
| Logic input levels <sup>2</sup>                                | -0.5 to $V_{DD} + 0.5V$ |
| Ground current <sup>3</sup>                                    | 1.5A                    |
| Continuous total power dissipation <sup>4</sup>                | 1200mW                  |
| Operating temperature range                                    | -40°C to 85°C           |
| Storage temperature range                                      | -65°C to +150°C         |
| Lead temperature 1.6mm (1/16 inch)<br>from case for 10 seconds | 260°C                   |

#### Notes:

1. Device will survive (but operation may not be specified or guaranteed) at these extremes.
2. All voltages are referenced to GND<sub>1</sub>.
3. Duty cycle is limited by the total power dissipated in the package.
4. For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C.

### General Description

The HV93 and HV94 are low voltage serial to high voltage parallel converters with push-pull outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high voltage current sourcing and sinking capabilities such as driving plasma panels, vacuum fluorescent, or large matrix LCD displays.

These devices consist of a 32-bit shift register, 32 latches, and control logic to enable outputs. HV<sub>OUT1</sub> is connected to the first stage of the shift register through the Output Enable logic. Data is shifted through the shift register on the low to high transition of the clock. The HV94 shifts in the counterclockwise direction when viewed from the top of the package and the HV93 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (32). Operation of the shift register is not affected by the LE (latch enable) or the OE (output enable) inputs. Transfer of data from the shift register to the latch occurs when the LE input is high. The data in the latch is retained when LE is low.

# Electrical Characteristics ( $V_{PP} = 60V$ , $V_{DD} = 5V$ , $T_A = 25^\circ C$ )

## DC Characteristics

| Symbol                  | Parameter                                    | Min          | Max  | Units   | Conditions                                                   |
|-------------------------|----------------------------------------------|--------------|------|---------|--------------------------------------------------------------|
| $I_{PP}$                | $V_{PP}$ Supply Current                      |              | 100  | $\mu A$ | HV <sub>OUT</sub> outputs HIGH to LOW                        |
| $I_{DDQ}$               | $I_{DD}$ Supply Current (Quiescent)          |              | 100  | $\mu A$ | All inputs = $V_{DD}$ or GND                                 |
| $I_{DD}$                | $I_{DD}$ Supply Current (Operating)          |              | 15   | mA      | $V_{DD} = V_{DD} \text{ max}$ ,<br>$f_{CLK} = 8 \text{ MHz}$ |
| $V_{OH} \text{ (Data)}$ | Shift Register Output Voltage                | $V_{DD}-0.5$ |      | V       | $I_O = -100\mu A$                                            |
| $V_{OL} \text{ (Data)}$ | Shift Register Output Voltage                |              | 0.5  | V       | $I_O = 100\mu A$                                             |
| $I_{IH}$                | Current Leakage, any input                   |              | 1.0  | $\mu A$ | Input = $V_{DD}$                                             |
| $I_{IL}$                | Current Leakage, any input                   |              | -1.0 | $\mu A$ | Input = GND                                                  |
| $V_{OC}$                | HV <sub>OUT</sub> Output Clamp Diode Voltage |              | -1.5 | V       | $I_{OC} = -5mA$                                              |
| $V_{OH}$                | HV <sub>OUT</sub> Output when Sourcing       | 52           |      | V       | $I_{OH} = -20mA$ , 0 to $70^\circ C$                         |
| $V_{OL}$                | HV <sub>OUT</sub> Output when Sinking        |              | 4.0  | V       | $I_{OL} = 5mA$ , 0 to $70^\circ C$                           |

## AC Characteristics

| Symbol                   | Parameter                                   | Min | Max | Units | Conditions   |
|--------------------------|---------------------------------------------|-----|-----|-------|--------------|
| $f_{CLK}$                | Clock Frequency                             |     | 8.0 | MHz   |              |
| $t_{WL}$ or $t_{WH}$     | Clock width, HIGH or LOW                    | 62  |     | ns    |              |
| $t_{SU}$                 | Setup time before CLK rises                 | 25  |     | ns    |              |
| $t_H$                    | Hold time after CLK rises                   | 10  |     | ns    |              |
| $t_{DLH} \text{ (Data)}$ | Data Output Delay after L to H CLK          |     | 110 | ns    | $C_L = 15pF$ |
| $t_{DHL} \text{ (Data)}$ | Data Output Delay after H to L CLK          |     | 110 | ns    | $C_L = 15pF$ |
| $t_{DLE}$                | LE Delay after L to H CLK                   | 50  |     | ns    |              |
| $t_{WLE}$                | Width of LE Pulse                           | 50  |     | ns    |              |
| $t_{SLE}$                | LE Setup Time before L to H CLK             | 50  |     | ns    |              |
| $t_{ON}$                 | Delay from LE to HV <sub>OUT</sub> , L to H |     | 500 | ns    |              |
| $t_{OFF}$                | Delay from LE to HV <sub>OUT</sub> , H to L |     | 500 | ns    |              |

## Recommended Operating Conditions

| Symbol           | Parameter                      |         | Min                  | Max             | Units |
|------------------|--------------------------------|---------|----------------------|-----------------|-------|
| V <sub>DD</sub>  | Logic Voltage Supply           |         | 4.5                  | 5.5             | V     |
| V <sub>PP</sub>  | High Voltage Supply            |         | 8.0                  | 80              | V     |
| V <sub>IH</sub>  | Input HIGH Voltage             |         | V <sub>DD</sub> -0.5 | V <sub>DD</sub> | V     |
| V <sub>IL</sub>  | Input LOW Voltage              |         | 0                    | 0.5             | V     |
| f <sub>CLK</sub> | Clock Frequency                |         | 0                    | 8.0             | MHz   |
| T <sub>A</sub>   | Operating Free-Air Temperature | Plastic | -40                  | +85             | °C    |
|                  |                                | Ceramic | -55                  | +125            | °C    |

### Notes:

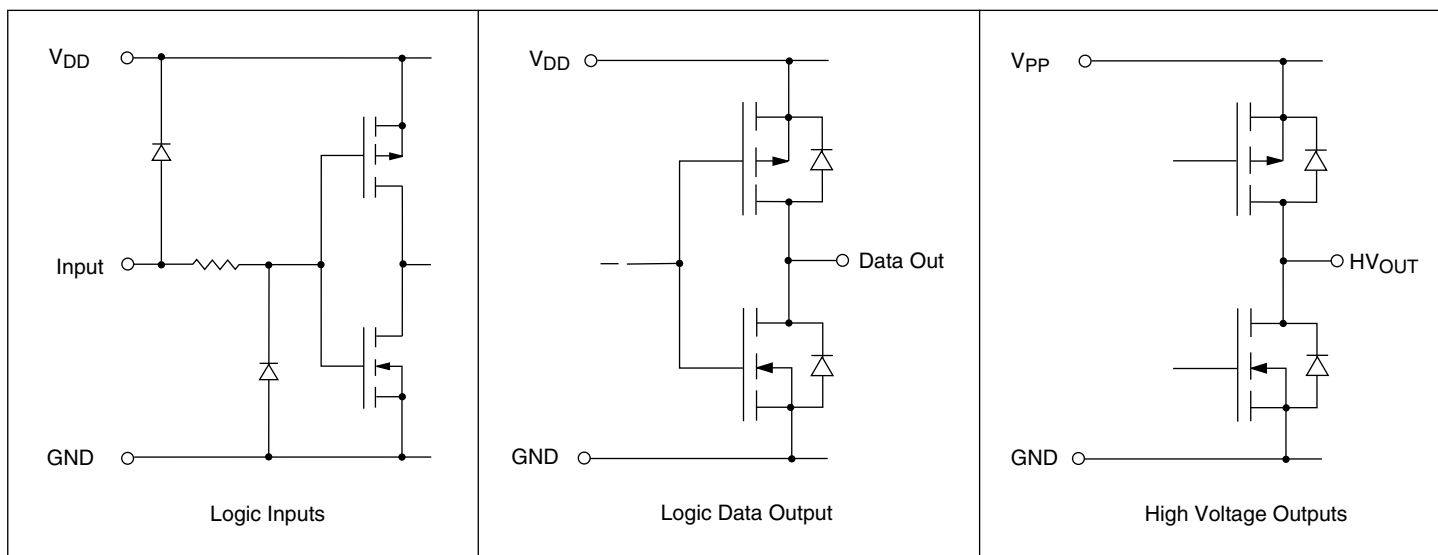
Power-up sequence should be the following:

1. Connect ground.
2. Apply  $V_{DD}$ .
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply  $V_{PP}$ .

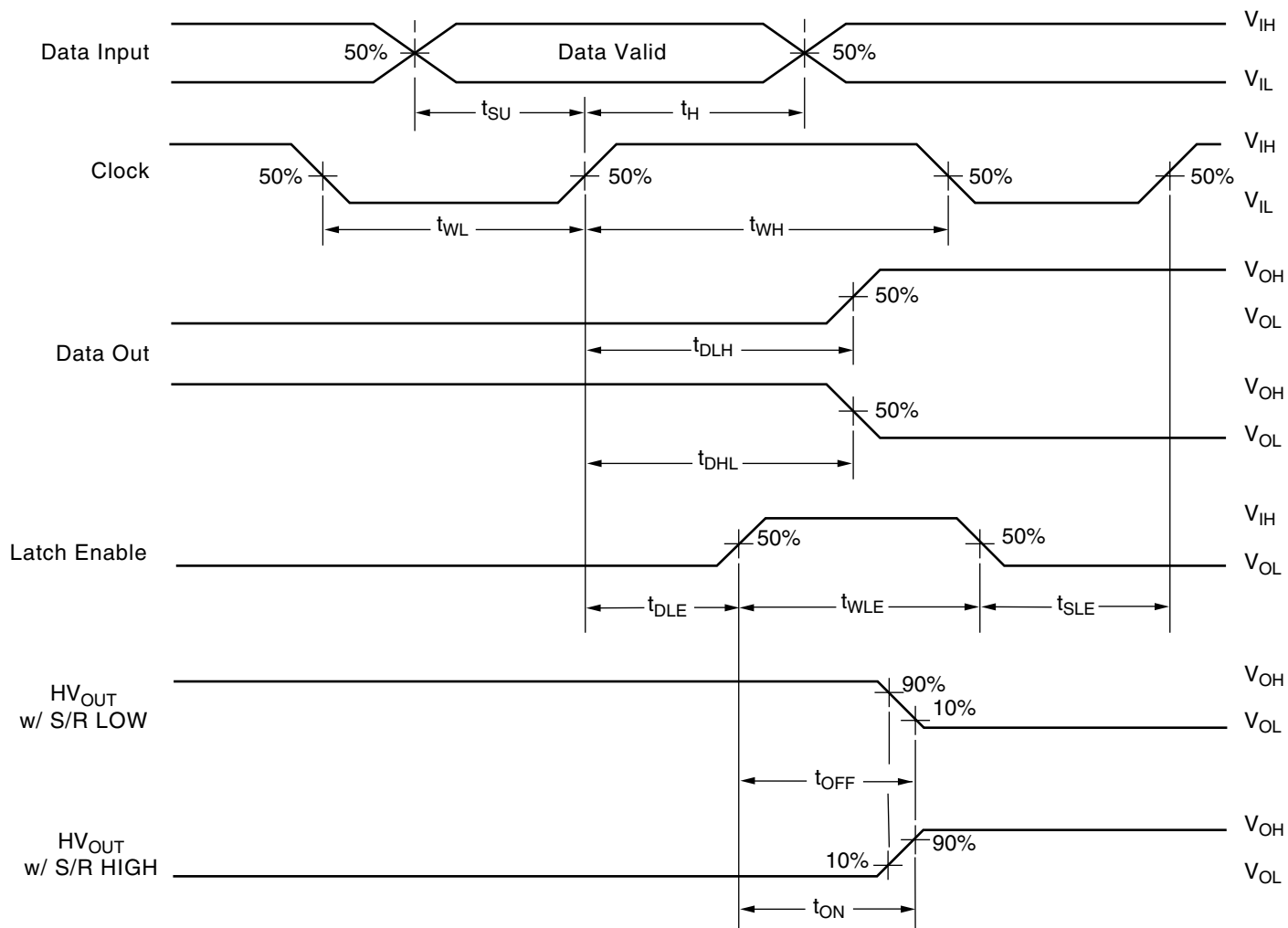
Power-down sequence should be the reverse of the above.

The  $V_{PP}$  should not drop below  $V_{DD}$  during operations.

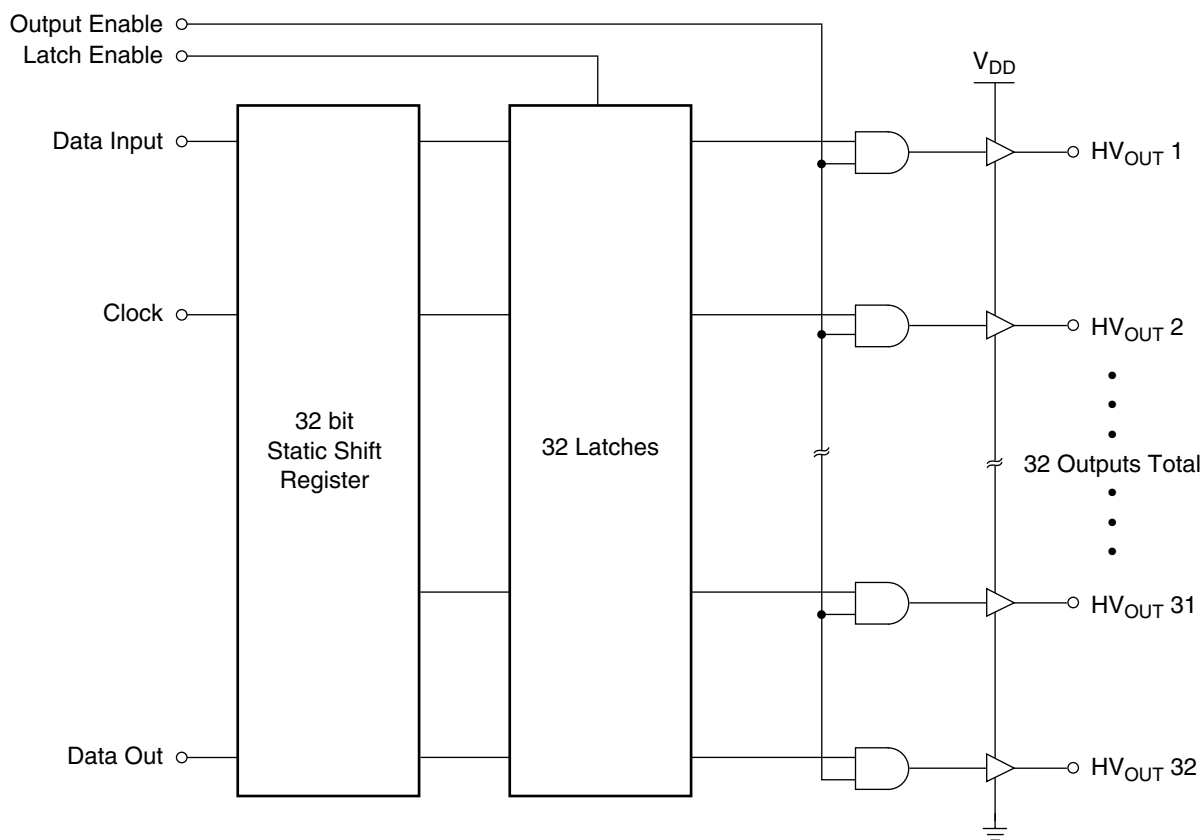
# Input and Output Equivalent Circuits



## Switching Waveforms



## Functional Block Diagram



## Function Tables

| Data Input | CLK* | Data Output |
|------------|------|-------------|
| H          |      | H           |
| L          |      | L           |
| X          | No   | No Change   |

\* = LOW-to-HIGH level transition

| Data Input | LE | OE | HV <sub>OUT</sub> Output    |
|------------|----|----|-----------------------------|
| X          | X  | L  | All HV <sub>OUT</sub> = LOW |
| X          | L  | H  | Previous Latched Data       |
| H          | H  | H  | H                           |
| L          | H  | H  | L                           |

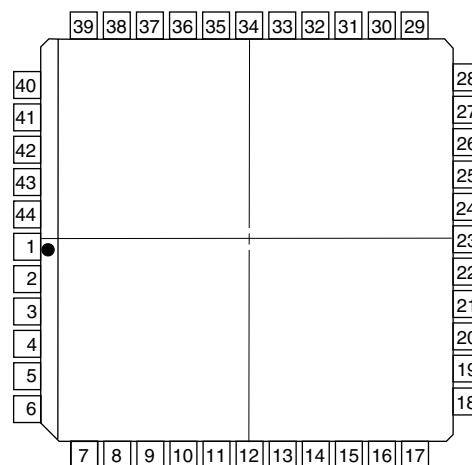
## Pin Configuration

### HV93

#### 44 Pin J-Lead Package

| Pin | Function             | Pin | Function             |
|-----|----------------------|-----|----------------------|
| 1   | HV <sub>OUT</sub> 17 | 23  | GND                  |
| 2   | HV <sub>OUT</sub> 16 | 24  | V <sub>PP</sub>      |
| 3   | HV <sub>OUT</sub> 15 | 25  | V <sub>DD</sub>      |
| 4   | HV <sub>OUT</sub> 14 | 26  | Latch Enable         |
| 5   | HV <sub>OUT</sub> 13 | 27  | Data In              |
| 6   | HV <sub>OUT</sub> 12 | 28  | Output Enable        |
| 7   | HV <sub>OUT</sub> 11 | 29  | N/C                  |
| 8   | HV <sub>OUT</sub> 10 | 30  | HV <sub>OUT</sub> 32 |
| 9   | HV <sub>OUT</sub> 9  | 31  | HV <sub>OUT</sub> 31 |
| 10  | HV <sub>OUT</sub> 8  | 32  | HV <sub>OUT</sub> 30 |
| 11  | HV <sub>OUT</sub> 7  | 33  | HV <sub>OUT</sub> 29 |
| 12  | HV <sub>OUT</sub> 6  | 34  | HV <sub>OUT</sub> 28 |
| 13  | HV <sub>OUT</sub> 5  | 35  | HV <sub>OUT</sub> 27 |
| 14  | HV <sub>OUT</sub> 4  | 36  | HV <sub>OUT</sub> 26 |
| 15  | HV <sub>OUT</sub> 3  | 37  | HV <sub>OUT</sub> 25 |
| 16  | HV <sub>OUT</sub> 2  | 38  | HV <sub>OUT</sub> 24 |
| 17  | HV <sub>OUT</sub> 1  | 39  | HV <sub>OUT</sub> 23 |
| 18  | Data Out             | 40  | HV <sub>OUT</sub> 22 |
| 19  | N/C                  | 41  | HV <sub>OUT</sub> 21 |
| 20  | N/C                  | 42  | HV <sub>OUT</sub> 20 |
| 21  | N/C                  | 43  | HV <sub>OUT</sub> 19 |
| 22  | Clock                | 44  | HV <sub>OUT</sub> 18 |

## Package Outline



top view

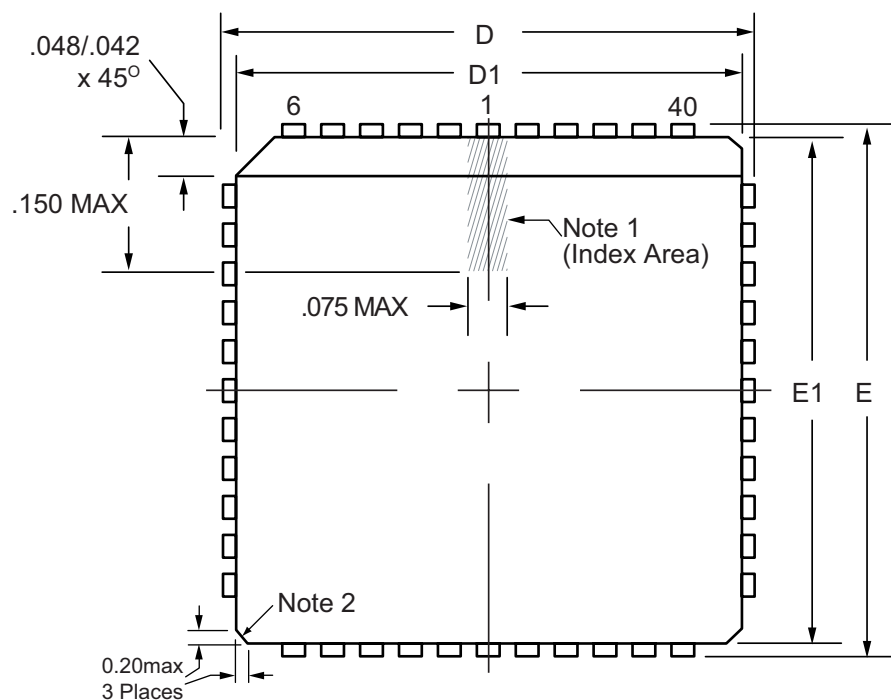
44-pin J-Lead Package

### HV94

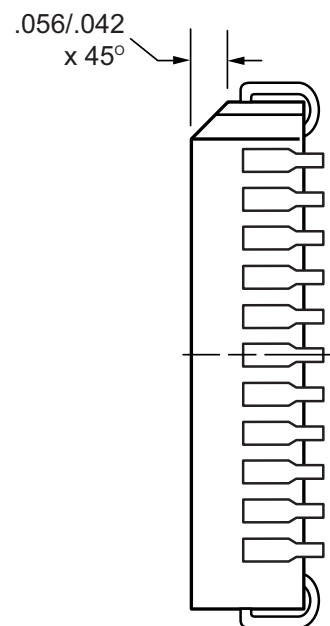
#### 44 Pin J-Lead Package

| Pin | Function             | Pin | Function             |
|-----|----------------------|-----|----------------------|
| 1   | HV <sub>OUT</sub> 16 | 23  | GND                  |
| 2   | HV <sub>OUT</sub> 17 | 24  | V <sub>PP</sub>      |
| 3   | HV <sub>OUT</sub> 18 | 25  | V <sub>DD</sub>      |
| 4   | HV <sub>OUT</sub> 19 | 26  | Latch Enable         |
| 5   | HV <sub>OUT</sub> 20 | 27  | Data In              |
| 6   | HV <sub>OUT</sub> 21 | 28  | Output Enable        |
| 7   | HV <sub>OUT</sub> 22 | 29  | N/C                  |
| 8   | HV <sub>OUT</sub> 23 | 30  | HV <sub>OUT</sub> 1  |
| 9   | HV <sub>OUT</sub> 24 | 31  | HV <sub>OUT</sub> 2  |
| 10  | HV <sub>OUT</sub> 25 | 32  | HV <sub>OUT</sub> 3  |
| 11  | HV <sub>OUT</sub> 26 | 33  | HV <sub>OUT</sub> 4  |
| 12  | HV <sub>OUT</sub> 27 | 34  | HV <sub>OUT</sub> 5  |
| 13  | HV <sub>OUT</sub> 28 | 35  | HV <sub>OUT</sub> 6  |
| 14  | HV <sub>OUT</sub> 29 | 36  | HV <sub>OUT</sub> 7  |
| 15  | HV <sub>OUT</sub> 30 | 37  | HV <sub>OUT</sub> 8  |
| 16  | HV <sub>OUT</sub> 31 | 38  | HV <sub>OUT</sub> 9  |
| 17  | HV <sub>OUT</sub> 32 | 39  | HV <sub>OUT</sub> 10 |
| 18  | Data Out             | 40  | HV <sub>OUT</sub> 11 |
| 19  | N/C                  | 41  | HV <sub>OUT</sub> 12 |
| 20  | N/C                  | 42  | HV <sub>OUT</sub> 13 |
| 21  | N/C                  | 43  | HV <sub>OUT</sub> 14 |
| 22  | Clock                | 44  | HV <sub>OUT</sub> 15 |

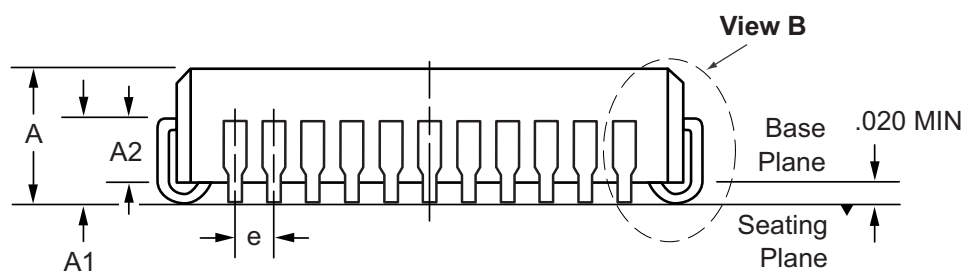
# 44-Lead PLCC Package Outline (PJ)



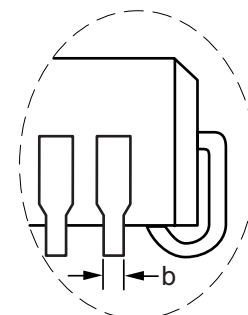
**Top View**



**Side View**



**Side View**



**View B**

- Note:**
1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.
  2. Exact shape of this feature is optional.

| Symbol             | A   | A1   | A2   | b    | D    | D1   | E    | E1   | e    |
|--------------------|-----|------|------|------|------|------|------|------|------|
| Dimension (inches) | MIN | .165 | .090 | .062 | .013 | .685 | .650 | .685 | .650 |
|                    | NOM | .172 | .105 | -    | -    | .690 | .653 | .690 | .653 |
|                    | MAX | .180 | .120 | .083 | .021 | .695 | .656 | .695 | .656 |

JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.

Drawings are not to scale.

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