## Features

- 32-kHz Crystal Oscillator
- 1.1 V to 2.2 V Operating-voltage Range
- Integrated Capacitors for Digital Trimming
- Suitable for up to 12.5 pF Quartz
- Output Pulse Formers
- Mask Options for Motor Period and Pulse Width
- Low Resistance Output for Bipolar Stepping Motor
- Motor Fast-test Function

## Description

The e1466D is an integrated circuit in CMOS Silicon Gate Technology for analog clocks. It consists of a 32-kHz oscillator, frequency divider, output pulse formers and push-pull motor drivers. Integrated capacitors are mask-selectable to accomodate the external quartz crystal. Additional capacitance can be selected through pad bonding for trimming the oscillator frequency.



32-kHz Clock CMOS IC with Digital Trimming

# e1466D

4731A-CLOCK-06/03





# **Pad Configuration**

## Figure 1. Pinning



<sup>(1)</sup> The pads VDD and OSCOUT are interchangeable per mask option
<sup>(2)</sup> The pads TEST and MOT1 are interchangeable per mask option

# **Pin Description**

Name	Description
VDD	Positive supply voltage
VSS	Negative supply voltage
OSCIN	Oscillator input
OSCOUT	Oscillator output
MOT1/2	Motor drive outputs
C1, C2, C3, C4	Oscillator trimming inputs
TEST	TEST input/output

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## **Functional Descripion**

## Oscillator

An oscillator inverter with feedback resistor is provided to generate the 32768 Hz clock frequency. Values for the fixed capacitors at OSCIN and OSCOUT are mask-selectable (see note 3 of "Operating Characteristics"). Four capacitor pads, C1 to C4, enable the users to add integrated trimming capacitors to OSCIN, providing 15 tuning steps.

TrimmingA frequency variation of typically 4 ppm for each tuning step is obtained by bonding the capac-<br/>itor pads to OSCIN. As none of these pads are bonded, the IC is in an untrimmed state. Figure<br/>3 shows the trimming curve characteristic.

Note: For applications which utilize this integrated trimming feature, Atmel will determine optimum values for the integrated capacitors COSCIN and COSCOUT.

Capacitor pads C1 to C4: 0 = open, 1 = connected to OSCIN

Combination C1 + C4 is redundant and therefore eliminated from the list

	Capacit	or Pads		
C4	C3	C2	C1	Trimming Step
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	1	0	0	3
1	0	0	0	4
0	0	1	1	5
0	1	0	1	6
0	1	1	0	7
1	0	1	0	8
1	1	0	0	9
0	1	1	1	10
1	0	1	1	11
1	1	0	1	12
1	1	1	0	13
1	1	1	1	14

Table 1. Frequency Trimming Table

## Motor Drive Output

The e1466D contains two push-pull output buffers for driving bipolar stepping motors. During a motor pulse, the N-channel device of one buffer and the P-channel device of the other buffer will be activated. Both N-channel transistors are on and conducting between output pulses. The outputs are protected against inductive voltage spikes with diodes to both supply pins. The motor output period and pulse width are mask-programmable, as listed below:

Available motor periods ( $T_M$ ): 125, 250, 500 ms and 2, 16 s

Available max. pulse widths ( $t_M$ ): 15, 6, 23.4, 31.25, 46.9 ms and 1 s

Available motor periods for motor test ( $T_{MT}$ ): 250, 500 ms and 1 s

Note: The following constraints for combination of motor period and pulse widths have to be considered:  $T_M > 4 \times t_M$ ,  $T_{MT} > 4 \times t_M$  or alternatively  $T_M = 2 \times t_M$ ,  $T_{MT} = 2 \times t_M$ 





## **Test Functions**

For test purposes, the TEST pad is open. With a high resistance probe (R  $\geq$  10 M $\Omega$ , C  $\geq$  20 pF), a test frequency f<sub>TEST</sub> of 128 Hz can be measured at the TEST pad. Connecting TEST (for at least 32 ms) to V<sub>DD</sub> changes the motor period from the selected value to T<sub>MT</sub> (mask-selectable) while the pulse width remains unaffected. This feature can be used for test-ing the mechanical parts of the clock.

## **Absolute Maximum Ratings**

Absolute maximum ratings define parameter limits which, if exceeded, may permanently change or damage the device. All inputs and outputs on Atmel's circuits are protected against electrostatic discharges. However, precautions to minimize the build-up of electrostatic charges during handling are recommended.

The circuit is protected against supply voltage reversal for typically 5 minutes.

Parameters	Symbol	Value	Unit
Supply voltage	V <sub>SS</sub>	-0.3 to 5 V	V
Input voltage range, all inputs	V <sub>IN</sub>	$(V_{SS} - 0.3 \text{ V}) \le V_{IN} \le (V_{DD} + 0.3 \text{ V})$	V
Output short-circuit duration		indefinite	
Power dissipation (DIL package)	P <sub>tot</sub>	125	mW
Operating ambient temperature range	T <sub>amb</sub>	-20 to +70	°C
Storage temperature range	T <sub>stg</sub>	-40 to +125	°C
Lead temperature during soldering at 2 mm distance, 10 s	T <sub>sld</sub>	260	۵°

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# **Operating Characteristics**

 $V_{SS} = 0 V$ ,  $V_{DD} = 1.5 V$ ,  $T_{amb} = +25^{\circ}C$ , unless otherwise specified. All voltage levels are measured with reference to  $V_{SS}$ . Test crystal as specified below.

Parameters	Test Conditions	Symbol	Min.	Тур.	Max.	Unit
Operating voltage		V <sub>DD</sub>	1.1	1.5	2.2	V
Operating temperature		T <sub>amb</sub>	-20		+70	°C
Operating current	$R_1 = \infty$ <sup>(2)</sup>	I <sub>DD</sub>		2	5	mA
Motor Drive Output						
Motor output current	$V_{DD} = 1.2 \text{ V}, \text{ R}_1 = 200 \Omega$	I <sub>M</sub>	±4.3			mA
Motor period		T <sub>M</sub>	S	ee option li	st	
Motor period during motor test		T <sub>MT</sub>	S	ee option li	st	
Motor pulse width		t <sub>M</sub>	S	ee option li	st	
Oscillator						
Startup voltage	Within 2 s	V <sub>START</sub>	1.2		2.2	V
Frequency stability	$\Delta V_{DD} = 100 \text{ mV}, V_{DD} = 1.1 \text{ to } 2.2 \text{ V}$	$\Delta f/f$		1		ppm
Integrated input capacitance	(3)	C <sub>OSCIN</sub>	See option list			
Integrated output capacitance		C <sub>OSCOUT</sub>	S	ee option li	st	
Integrated capacitance for bond option	(4)	C1 C2 C3 C4		3 4 5 6		pF pF pF pF
TEST Input						
Input current	TEST = $V_{DD}$ peak current	I <sub>TINH</sub>	0.6	3	10	μA
Input current	TEST = V <sub>SS</sub> peak current	I <sub>TINL</sub>	-0.6	-3	-10	μA
Input debounce delay		t <sub>TIN</sub>	23.4		31.2	ms

1. Typical parameters represent the statistical mean values Notes:

2. See test circuit

3. Values can be selected in 1 pF steps. A total capacitance ( $C_{OSCIN} + C_{OSCOUT}$ ) of 38 pF is available 4. These values are valid for 10 pF quartz applications. For  $C_L = 12.5$  pF these values change to 4.5, 6, 7.5, 9 pF

Figure 2. Functional Test







## Test Crystal Specification

Oscillation frequency	f <sub>OSC</sub> = 32768 Hz
Series resistance	$R_{S} = 30 \text{ k}\Omega$
Static capacitance	C <sub>0</sub> = 1.5 pF
Dynamic capacitance	C <sub>1</sub> = 3.0 fF
Load capacitance	$C_L$ optionally 10 or 12.5 pF





Figure 4. Typical Trimming Curve Characteristic for T<sub>M</sub> of 2 s



COX means frequency deviation due to production process variations.

Trimming inputs C1 ... C4 are binary weighted, i.e., C1 ... C4 = 0 corresponds to trimming step 0 C1 ... C4 = 1 corresponds to trimming step 15

LSB = C1

e1466D

# **Ordering Information**

## Table 2. Option List e1466Dx

Option		Motor			Load Capacitance					
x	Cycle (T <sub>M</sub> ) s	Pulse (t <sub>M</sub> ) ms	Test (Т <sub>мт</sub> ) ms	C <sub>OSCIN</sub> <sup>(1)</sup> pF	С <sub>оscout</sub> <sup>(1)</sup> pF	C1 pF	C2 pF	C3 pF	C4 pF	pF
Α	2	46.9	250	9	20	3	4	5	6	10
AO	2	46.9	250	9	20	3	4	5	6	10
FO	0.25	62.5	2000	9	20	3	4	5	6	10
НО	2	1000	500/ 250	9	20	3	4	5	6	10

Note: 1. On-chip stray capacitance included

Option	Pad Designation											
x	Pad 1	Pad 2	Pad 3	Pad 4	Pad 5	Pad 6	Pad 7	Pad 8	Pad 8	Pad 10	Pad 11	Pad 12
A	OSCIN	OSCOUT	MOT2	MOT1	MOT1	TEST	V <sub>SS</sub>	V <sub>DD</sub>	C4	C3	C2	C1
AO	OSCIN	OSCOUT	MOT2	MOT1	MOT1	TEST	V <sub>SS</sub>	V <sub>DD</sub>	C4	C3	C2	C1
FO	OSCIN	OSCOUT	MOT2	MOT1	MOT1	TEST	V <sub>SS</sub>	V <sub>DD</sub>	C4	C3	C2	C1
HO	OSCIN	OSCOUT	MOT2	MOT1	MOT1	TEST	V <sub>SS</sub>	V <sub>DD</sub>	C4	C3	C2	C1





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