

## Features

- 16-channel GPS Correlator
  - 8192 Search Bins with GPS Acquisition Accelerator
  - Accuracy: 2.5m CEP (Stand-Alone, S/A off)
  - Time to First Fix: 34s (Cold Start)
  - Acquisition Sensitivity: –142 dBm (Cold Start)
  - Tracking Sensitivity: –158 dBm
- Utilizes the ARM7TDMI® ARM® Thumb® Processor Core
  - High-performance 32-bit RISC Architecture
  - High-density 16-bit Instruction Set
  - EmbeddedICE™ (In-circuit Emulator)
- 128 Kbyte Internal RAM
- 384 Kbyte Internal ROM, Firmware Version V5.0
- Position TEchnology Provided by µ-blox
- 6-channel Peripheral Data Controller (PDC)
- 8-level Priority, Individually Maskable, Vectored Interrupt Controller
  - 2 External Interrupts
- 24 User-programmable I/O Lines
- 1 USB Device Port
  - Universal Serial Bus (USB) V2.0 Full-speed Device
  - Embedded USB V2.0 Full-speed Transceiver
  - Suspend/Resume Logic
  - Ping-pong Mode for Isochronous and Bulk Endpoints
- 2 USARTs
  - 2 Dedicated Peripheral Data Controller (PDC) Channels per USART
- Master/Slave SPI Interface
  - 2 Dedicated Peripheral Data Controller (PDC) Channels
  - 8-bit to 16-bit Programmable Data Length
  - 4 External Slave Chip Selects
- Programmable Watchdog Timer
- Advanced Power Management Controller (APMC)
  - Peripherals Can Be Deactivated Individually
  - Geared Master Clock to Reduce Power Consumption
  - Sleep State with Disabled Master Clock
  - Hibernate State with 32.768 kHz Master Clock
- Real Time Clock (RTC)
- 2.3V to 3.6V or 1.8V Core Supply Voltage
- Includes Power Supervisor
- 1.8V to 3.3V User-definable I/O Voltage for Several GPIOs with 5V Tolerance
- 4 Kbytes Battery Backup Memory
- 8 mm × 8 mm 56 Pin QFN56 Package
- RoHS-compliant, Green



## GPS Baseband Processor SuperSense

### ATR0625P



## 1. Description

The GPS baseband processor ATR0625P includes a 16-channel GPS correlator and is based on the ARM7TDMI processor core.

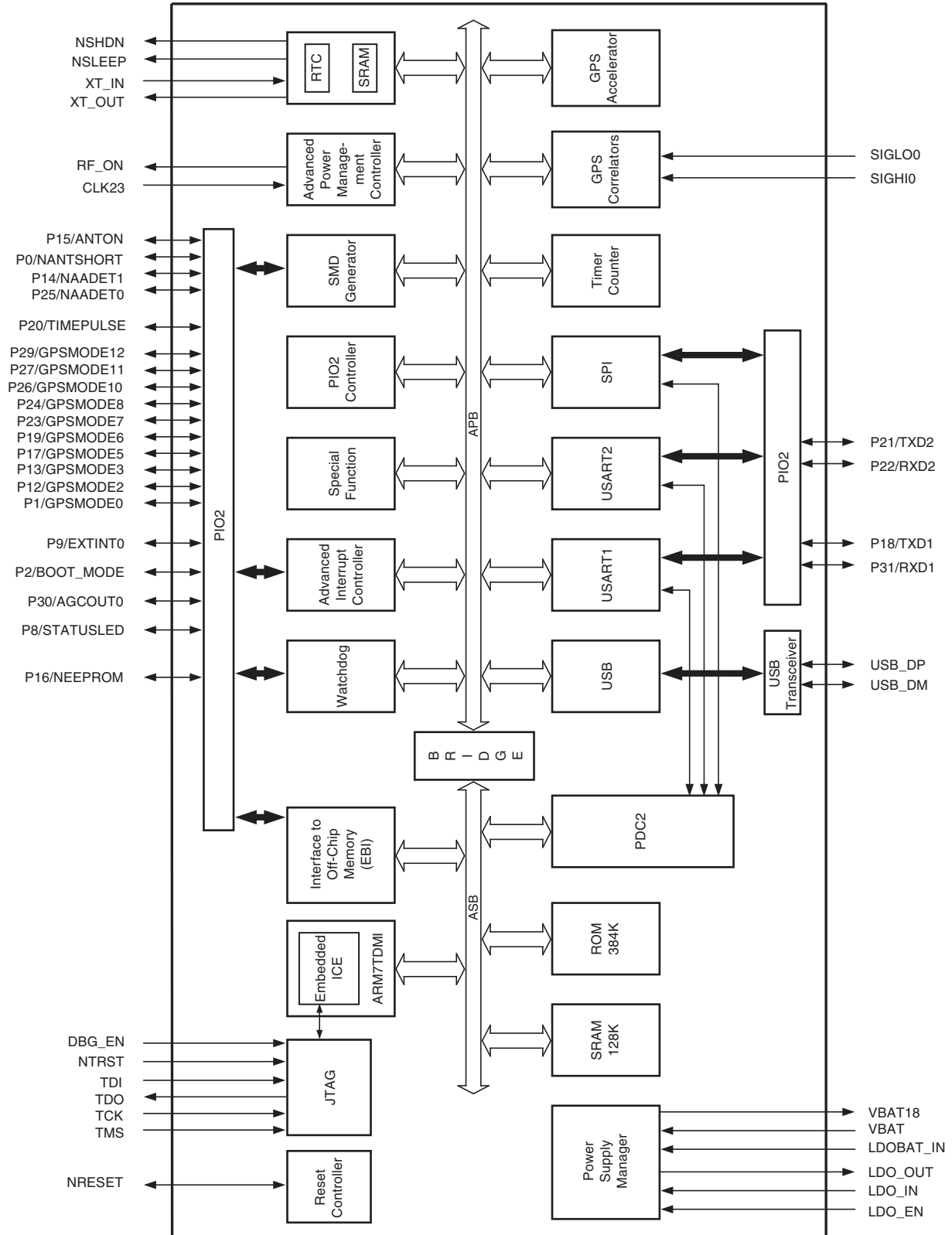
This processor has a high-performance 32-bit RISC architecture and very low power consumption. In addition, a large number of internally banked registers result in very fast exception handling, making the device ideal for real-time control applications. The ATR0625P has two USART and an USB device port. This port is compliant with the Universal Serial Bus (USB) V2.0 full-speed device specification.

The ATR0625P includes full GPS SuperSense<sup>®</sup> firmware, licensed from u-blox AG, which performs the basic GPS operation, including tracking, acquisition, navigation and position data output. For normal PVT (Position/Velocity/Time) applications, there is no need for off-chip Flash memory or ROM.

The firmware supports e.g. the NMEA<sup>®</sup> protocol (2.1 and 2.3), a binary protocol for PVT data, configuration and debugging, the RTCM protocol for DGPS, SBAS (WAAS, EGNOS and MSAS) and A-GPS (aiding). It is also possible to store the configuration settings in an optional external EEPROM.

The ATR0625P is manufactured using Atmel<sup>®</sup>'s high-density CMOS technology. By combining the ARM7TDMI microcontroller core with on-chip SRAM, 16-channel GPS correlator, and a wide range of peripheral functions on a monolithic chip, the ATR0625P provides a highly flexible and cost-effective solution for GPS applications.

Figure 1-1. ATR0625P Block Diagram



## 2. Architectural Overview

### 2.1 Description

The ATR0625P architecture consists of two main buses, the Advanced System Bus (ASB) and the Advanced Peripheral Bus (APB). The ASB is designed for maximum performance. It interfaces the processor with the on-chip 32-bit memories. The APB is designed for accesses to on-chip peripherals and is optimized for low power consumption. The AMBA™ Bridge provides an interface between the ASB and the APB.

An on-chip Peripheral Data Controller (PDC2) transfers data between the on-chip USARTs/SPI and the on-chip and off-chip memories without processor intervention. Most importantly, the PDC2 removes the processor interrupt handling overhead and significantly reduces the number of clock cycles required for a data transfer. It can transfer up to 64K contiguous bytes without reprogramming the starting address. As a result, the performance of the microcontroller is increased and the power consumption reduced.

The ATR0625P peripherals are designed to be easily programmable with a minimum number of instructions. Each peripheral has a 16 Kbyte address space allocated in the upper 3 Mbyte of the 4 Gbyte address space. (Except for the interrupt controller, which has 4 Kbyte address space.) The peripheral base address is the lowest address of its memory space. The peripheral register set is composed of control, mode, data, status, and interrupt registers.

To maximize the efficiency of bit manipulation, frequently written registers are mapped into three memory locations. The first address is used to set the individual register bits, the second resets the bits, and the third address reads the value stored in the register. A bit can be set or reset by writing a “1” to the corresponding position at the appropriate address. Writing a “0” has no effect. Individual bits can thus be modified without having to use costly read-modify-write and complex bit-manipulation instructions.

All of the external signals of the on-chip peripherals are under the control of the Parallel I/O (PIO2) Controller. The PIO2 Controller can be programmed to insert an input filter on each pin or generate an interrupt on a signal change. After reset, the user must carefully program the PIO2 Controller in order to define which peripheral signals are connected with off-chip logic.

The ARM7TDMI processor operates in little-endian mode on the ATR0625P GPS Baseband. The processor's internal architecture and the ARM and Thumb instruction sets are described in the ARM7TDMI datasheet.

The ARM standard In-Circuit Emulator (ICE) debug interface is supported via the JTAG/ICE port of the ATR0625P.

For features of the ROM firmware (SuperSense), refer to the software documentation available from u-blox AG, Switzerland.

## 3. Pin Configuration

### 3.1 Pinout

Figure 3-1. Pinout QFN56 (Top View)

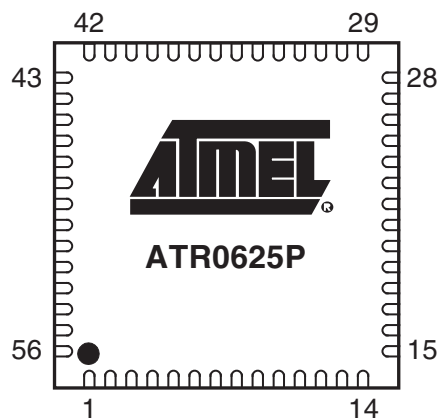


Table 3-1. ATR0625P Pinout

| Pin Name  | QFN56          | Pin Type | Pull Resistor<br>(Reset Value) <sup>(1)</sup> | Firmware Label | PIO Bank A |         |
|-----------|----------------|----------|---|----------------|------------|---------|
|           |                |          |   |                | I          | O       |
| CLK23     | 37             | IN       |   |                |            |         |
| DBG_EN    | 8              | IN       | PD  |                |            |         |
| GND       | <sup>(2)</sup> | IN       |   |                |            |         |
| LDOBAT_IN | 21             | IN       |   |                |            |         |
| LDO_EN    | 25             | IN       |   |                |            |         |
| LDO_IN    | 20             | IN       |   |                |            |         |
| LDO_OUT   | 19             | OUT      |   |                |            |         |
| NRESET    | 41             | I/O      | Open Drain PU                                 |                |            |         |
| NSHDN     | 26             | OUT      |   |                |            |         |
| NSLEEP    | 24             | OUT      |   |                |            |         |
| NTRST     | 13             | IN       | PD  |                |            |         |
| P0        | 40             | I/O      | PD  | NANTSHORT      |            |         |
| P1        | 47             | I/O      | Configurable (PD)                             | GPSMODE0       |            | AGCOUT1 |
| P2        | 46             | I/O      | Configurable (PD)                             | BOOT_MODE      |            | "0"     |
| P8        | 48             | I/O      | Configurable (PD)                             | STATUSLED      |            | "0"     |
| P9        | 29             | I/O      | PU to VBAT18                                  | EXTINT0        | EXTINT0    |         |
| P12       | 49             | I/O      | Configurable (PU)                             | GPSMODE2       |            | NPCS2   |
| P13       | 32             | I/O      | PU to VBAT18                                  | GPSMODE3       | EXTINT1    |         |

- Notes:
1. PD = internal pull-down resistor, PU = internal pull-up resistor, OH = switched to Output High at reset
  2. Ground plane
  3. VBAT18 represent the internal power supply of the backup power domain, see section "Power Supply" on page 17.
  4. VDDIO is the supply voltage for the following GPIO-pins: P1, P2, P8, P12, P14, P16, P17, P18, P19, P20, P21, P23, P24, P25, P26, P27 and P29, see section "Power Supply" on page 17.
  5. VDD\_USB is the supply voltage for following the USB-pins: USB\_DM and USB\_DP, see section "Power Supply" on page 17. For operation of the USB interface, supply of 3.0V to 3.6V is required.
  6. This pin is not connected

**Table 3-1. ATR0625P Pinout (Continued)**

| Pin Name               | QFN56  | Pin Type | Pull Resistor<br>(Reset Value) <sup>(1)</sup> | Firmware Label | PIO Bank A |         |
|------------------------|--------|----------|---|----------------|------------|---------|
|                        |        |          |   |                | I          | O       |
| P14                    | 1      | I/O      | Configurable (PD)                             | NAADET1        |            | "0"     |
| P15                    | 17     | I/O      | PD  | ANTON          |            |         |
| P16                    | 6      | I/O      | Configurable (PU)                             | NEEPROM        | SIGHI1     |         |
| P17                    | 2      | I/O      | Configurable (PD)                             | GPSMODE5       | SCK1       | SCK1    |
| P18                    | 45     | I/O      | Configurable (PU)                             | TXD1           |            | TXD1    |
| P19                    | 53     | I/O      | Configurable (PU)                             | GPSMODE6       | SIGLO1     |         |
| P20                    | 4      | I/O      | Configurable (PD)                             | TIMEPULSE      | SCK2       | SCK2    |
| P21                    | 52     | I/O      | Configurable (PU)                             | TXD2           |            | TXD2    |
| P22                    | 30     | I/O      | PU to VBAT18                                  | RXD2           | RXD2       |         |
| P23                    | 3      | I/O      | Configurable (PU)                             | GPSMODE7       | SCK        | SCK     |
| P24                    | 5      | I/O      | Configurable (PU)                             | GPSMODE8       | MOSI       | MOSI    |
| P25                    | 55     | I/O      | Configurable (PD)                             | NAADET0        | MISO       | MISO    |
| P26                    | 44     | I/O      | Configurable (PU)                             | GPSMODE10      | NSS        | NPCS0   |
| P27                    | 54     | I/O      | Configurable (PU)                             | GPSMODE11      |            | NPCS1   |
| P29                    | 50     | I/O      | Configurable (PU)                             | GPSMODE12      |            | NPCS3   |
| P30                    | 16     | I/O      | PD  | AGCOUT0        |            | AGCOUT0 |
| P31                    | 31     | I/O      | PU to VBAT18                                  | RXD1           | RXD1       |         |
| RF_ON                  | 15     | OUT      | PD  |                |            |         |
| SIGHI0                 | 38     | IN       |   |                |            |         |
| SIGLO0                 | 39     | IN       |   |                |            |         |
| TCK                    | 9      | IN       | PU  |                |            |         |
| TDI                    | 10     | IN       | PU  |                |            |         |
| TDO                    | 11     | OUT      |   |                |            |         |
| TMS                    | 12     | IN       | PU  |                |            |         |
| USB_DM                 | 34     | I/O      |   |                |            |         |
| USB_DP                 | 35     | I/O      |   |                |            |         |
| VBAT                   | 22     | IN       |   |                |            |         |
| VBAT18 <sup>(3)</sup>  | 23     | OUT      |   |                |            |         |
| VDD18                  | 7, 14  | IN       |   |                |            |         |
| VDD18                  | 18, 36 | IN       |   |                |            |         |
| VDD18                  | 51     | IN       |   |                |            |         |
| VDDIO <sup>(4)</sup>   | 43, 56 | IN       |   |                |            |         |
| VDD_USB <sup>(5)</sup> | 33     | IN       |   |                |            |         |
| XT_IN                  | 28     | IN       |   |                |            |         |
| XT_OUT                 | 27     | OUT      |   |                |            |         |
| NC <sup>(6)</sup>      | 42     |          |   |                |            |         |

- Notes:
1. PD = internal pull-down resistor, PU = internal pull-up resistor, OH = switched to Output High at reset
  2. Ground plane
  3. VBAT18 represent the internal power supply of the backup power domain, see section [“Power Supply” on page 17](#).
  4. VDDIO is the supply voltage for the following GPIO-pins: P1, P2, P8, P12, P14, P16, P17, P18, P19, P20, P21, P23, P24, P25, P26, P27 and P29, see section [“Power Supply” on page 17](#).
  5. VDD\_USB is the supply voltage for following the USB-pins: USB\_DM and USB\_DP, see section [“Power Supply” on page 17](#). For operation of the USB interface, supply of 3.0V to 3.6V is required.
  6. This pin is not connected

## 3.2 Signal Description

**Table 3-2.** ATR0625P Signal Description

| Module | Name           | Function                                     | Type   | Active Level          | Comment   |
|--------|----------------|--|--------|-----------------------|---|
| EBI    | BOOT_MODE      | Boot Mode Input                              | Input  | –                     | PIO-controlled after reset, internal pull-down resistor |
| USART  | TXD1 to TXD2   | Transmit Data Output                         | Output | –                     | PIO-controlled after reset                              |
|        | RXD1 to RXD2   | Receive Data Input                           | Input  | –                     | PIO-controlled after reset                              |
|        | SCK1 to SCK2   | External Synchronous Serial Clock            | I/O    | –                     | PIO-controlled after reset                              |
| USB    | USB_DP         | USB Data (D+)                                | I/O    | –                     |   |
|        | USB_DM         | USB Data (D-)                                | I/O    | –                     |   |
| APMC   | RF_ON          |  | Output | –                     | Interface to ATR0601                                    |
| AIC    | EXTINT0-1      | External Interrupt Request                   | Input  | High/<br>Low/<br>Edge | PIO-controlled after reset                              |
| AGC    | AGCOUT0-1      | Automatic Gain Control                       | Output | –                     | Interface to ATR0601<br>PIO-controlled after reset      |
| RTC    | NSLEEP         | Sleep Output                                 | Output | Low                   | Interface to ATR0601                                    |
|        | NSHDN          | Shutdown Output                              | Output | Low                   | Connect to pin LDO_EN                                   |
|        | XT_IN          | Oscillator Input                             | Input  | –                     | RTC oscillator  |
|        | XT_OUT         | Oscillator Output                            | Output | –                     | RTC oscillator  |
| SPI    | SCK            | SPI Clock                                    | I/O    | –                     | PIO-controlled after reset                              |
|        | MOSI           | Master Out Slave In                          | I/O    | –                     | PIO-controlled after reset                              |
|        | MISO           | Master In Slave Out                          | I/O    | –                     | PIO-controlled after reset                              |
|        | NSS/NPCS0      | Slave Select                                 | I/O    | Low                   | PIO-controlled after reset                              |
|        | NPCS1 to NPCS3 | Slave Select                                 | Output | Low                   | PIO-controlled after reset                              |
| PIO    | P0 to P31      | Programmable I/O Port                        | I/O    | –                     | Input after reset                                       |
| GPS    | SIGHI0         | Digital IF                                   | Input  | –                     | Interface to ATR0601                                    |
|        | SIGLO0         | Digital IF                                   | Input  | –                     | Interface to ATR0601                                    |
|        | SIGHI1         | Digital IF                                   | Input  | –                     | PIO-controlled after reset                              |
|        | SIGLO1         | Digital IF                                   | Input  | –                     | PIO-controlled after reset                              |
|        | TIMEPULSE      | GPS synchronized time pulse                  | Output | –                     | PIO-controlled after reset                              |
| CONFIG | GPSMODE0-12    | GPS Mode                                     | Input  | –                     | PIO-controlled after reset                              |
|        | STATUSLED      | Status LED                                   | Output | –                     | PIO-controlled after reset                              |
|        | NEEPROM        | Enable EEPROM Support                        | Input  | Low                   | PIO-controlled after reset                              |
|        | ANTON          | Active antenna power on Output               | Output | –                     | PIO-controlled after reset                              |
|        | NANTSHORT      | Active antenna short circuit detection Input | Input  | Low                   | PIO-controlled after reset                              |
|        | NAADET0-1      | Active antenna detection Input               | Input  | Low                   | PIO-controlled after reset                              |

Note: 1. The USB transceiver is disabled if VDD\_USB < 2.0V. In this case the pins USB\_DM and USB\_DP are connected to GND (internal pull-down resistors). The USB transceiver is enabled if VDD\_USB is within 3.0V and 3.6V.

**Table 3-2. ATR0625P Signal Description (Continued)**

| Module   | Name      | Function         | Type   | Active Level | Comment  |
|----------|-----------|------------------|--------|--------------|--|
| JTAG/ICE | TMS       | Test Mode Select | Input  | –            | Internal pull-up resistor                            |
|          | TDI       | Test Data In     | Input  | –            | Internal pull-up resistor                            |
|          | TDO       | Test Data Out    | Output | –            |  |
|          | TCK       | Test Clock       | Input  | –            | Internal pull-up resistor                            |
|          | NTRST     | Test Reset Input | Input  | Low          | Internal pull-down resistor                          |
|          | DBG_EN    | Debug Enable     | Input  | High         | Internal pull-down resistor                          |
| CLOCK    | CLK23     | Clock Input      | Input  | –            | Interface to ATR0601, Schmitt trigger input          |
| RESET    | NRESET    | Reset Input      | I/O    | Low          | Open drain with internal pull-up resistor            |
| POWER    | VDD18     |                  | Power  | –            | Core voltage 1.8V                                    |
|          | VDDIO     |                  | Power  | –            | Variable IO voltage 1.65V to 3.6V                    |
|          | VDD_USB   |                  | Power  | –            | USB voltage 0 to 2.0V or 3.0V to 3.6V <sup>(1)</sup> |
|          | GND       |                  | Power  | –            | Ground   |
| LDOBAT   | LDOBAT_IN |                  | Power  | –            | 2.3V to 3.6V   |
|          | VBAT      |                  | Power  | –            | 1.5V to 3.6V   |
|          | VBAT18    |                  | Out    | –            | 1.8V backup voltage                                  |
| LDO18    | LDO_IN    | LDO In           | Power  | –            | 2.3V to 3.6V   |
|          | LDO_OUT   | LDO Out          | Power  | –            | 1.8V core voltage, max. 80 mA                        |
|          | LDO_EN    | LDO Enable       | Input  | –            |  |

Note: 1. The USB transceiver is disabled if VDD\_USB < 2.0V. In this case the pins USB\_DM and USB\_DP are connected to GND (internal pull-down resistors). The USB transceiver is enabled if VDD\_USB is within 3.0V and 3.6V.



## 3.3 Setting GPSPMODE0 to GPSPMODE12

The start-up configuration of a ROM-based system without external non-volatile memory is defined by the status of the GPSPMODE pins after system reset. Alternatively, the system can be configured through message commands passed through the serial interface after start-up. This configuration of the ATR0625P can be stored in an external non-volatile memory like EEPROM. *Default* designates settings used by ROM firmware if GPSPMODE configuration is disabled (GPSPMODE0 = 0).

**Table 3-3.** GPSPMODE Functions

| Pin              | Function  |
|------------------|---|
| GPSPMODE0 (P1)   | Enable configuration with GPSPMODE pins   |
| GPSPMODE1 (P9)   | This pin (EXTINT0) is used for <i>FixNow™</i> functionality and not used for GPSPMODE configuration.  |
| GPSPMODE2 (P12)  | GPS sensitivity settings  |
| GPSPMODE3 (P13)  |   |
| GPSPMODE4 (P14)  | This pin (NAADET1) is used as active antenna supervisor input and not used for GPSPMODE configuration. This is the default selection if GPSPMODE configuration is disabled. |
| GPSPMODE5 (P17)  | Serial I/O configuration  |
| GPSPMODE6 (P19)  |   |
| GPSPMODE7 (P23)  | USB Power Mode  |
| GPSPMODE8 (P24)  | General I/O Configuration   |
| GPSPMODE9 (P25)  | This pin (NAADET0) is used as active antenna supervisor input and not used for GPSPMODE configuration.  |
| GPSPMODE10 (P26) | General I/O Configuration   |
| GPSPMODE11 (P27) |   |
| GPSPMODE12 (P29) | Serial I/O configuration  |

In the case that GPSPMODE pins with internal pull-up or pull-down resistors are connected to GND/VDD18, additional current is drawn over these resistors. Especially GPSPMODE3 can impact the back-up current.

### 3.3.1 Enable GPSPMODE Pin Configuration

**Table 3-4.** Enable Configuration with GPSPMODE Pins

| GPSPMODE0 (Reset = PD) | Description   |
|------------------------|---|
| 0 <sup>(1)</sup>       | Ignore all GPSPMODE pins. The default settings as indicated below are used. |
| 1                      | Use settings as specified with GPSPMODE[2, 3, 5 to 8, 10 to 12]             |

Note: 1. Leave open

If the GPSPMODE configuration is enabled (GPSPMODE0 = 1) and the other GPSPMODE pins are not connected externally, the reset default values of the internal pull-down and pull-up resistors will be used.

### 3.3.2 Sensitivity Settings

**Table 3-5.** GPS Sensitivity Settings

| GPSMODE3<br>(Fixed PU) | GPSMODE2<br>(Reset = PU) | Description                   |
|------------------------|--------------------------|-------------------------------|
| 0 <sup>(1)</sup>       | 0                        | Auto mode (Default ROM value) |
| 0 <sup>(1)</sup>       | 1 <sup>(2)</sup>         | Fast mode                     |
| 1 <sup>(2)</sup>       | 0                        | Normal mode                   |
| 1 <sup>(2)</sup>       | 1 <sup>(2)</sup>         | High sensitivity              |

Notes: 1. Increased back-up current  
2. Leave open

For all GPS receivers the sensitivity depends on the integration time of the GPS signals. Therefore there is a trade-off between sensitivity and the time to detect the GPS signal (Time to first fix). The three modes, “Fast Acquisition”, “Normal” and “High Sensitivity”, have a fixed integration time. The “Normal” mode, recommended for the most applications, is a trade off between the sensitivity and TTFF. The “Fast Acquisition” mode is optimized for fast acquisition, at the cost of a lower sensitivity. The “High Sensitivity” mode is optimized for higher sensitivity, at the cost of longer TTFF. The “Auto” mode adjusts the integration time (sensitivity) automatically according to the measured signal levels. That means the receiver with this setting has a fast TTFF at strong signals, a high sensitivity to acquire weak signals but some times at medium signal level a higher TTFF as the “Normal” mode. These sensitivity settings affect only the startup performance not the tracking performance.

### 3.3.3 Serial I/O Configuration

The ATR0625P features a two-stage I/O message and protocol selection procedure for the two available serial ports. At the first stage, a certain protocol can be enabled or disabled for a given USART port or the USB port. Selectable protocols are RTCM, NMEA and UBX. At the second stage, messages can be enabled or disabled for each enabled protocol on each port. In all configurations discussed below, all protocols are enabled on all ports. But output messages are enabled in a way that ports appear to communicate at only one protocol. However, each port will accept any input message in any of the three implemented protocols.

**Table 3-6.** Serial I/O Configuration

| GPSMODE12<br>(Reset = PU) | GPSMODE6<br>(Reset = PU) | GPSMODE5<br>(Reset = PD) | USART1/USB<br>(Output Protocol/<br>Baud Rate (kBaud)) | USART2<br>(Output Protocol/<br>Baud Rate (kBaud)) | Messages <sup>(1)</sup> | Information Messages         |
|---------------------------|--------------------------|--------------------------|---|---|-------------------------|------------------------------|
| 0                         | 0                        | 0 <sup>(2)</sup>         | UBX/57.6  | NMEA/19.2   | High                    | User, Notice, Warning, Error |
| 0                         | 0                        | 1                        | UBX/38.4  | NMEA/9.6  | Medium                  | User, Notice, Warning, Error |
| 0                         | 1 <sup>(2)</sup>         | 0 <sup>(2)</sup>         | UBX/19.2  | NMEA/4.8  | Low                     | User, Notice, Warning, Error |
| 0                         | 1 <sup>(2)</sup>         | 1                        | –/Auto  | –/Auto  | Off                     | None                         |
| 1 <sup>(2)</sup>          | 0                        | 0 <sup>(2)</sup>         | NMEA/19.2   | UBX/57.6  | High                    | User, Notice, Warning, Error |
| 1 <sup>(2)</sup>          | 0                        | 1                        | NMEA/4.8  | UBX/19.2  | Low                     | User, Notice, Warning, Error |
| 1 <sup>(2)</sup>          | 1 <sup>(2)</sup>         | 0 <sup>(2)</sup>         | NMEA/9.6  | UBX/38.4  | Medium                  | User, Notice, Warning, Error |
| 1 <sup>(2)</sup>          | 1 <sup>(2)</sup>         | 1                        | UBX/115.2   | NMEA/19.2   | Debug                   | All                          |

Notes: 1. See [Table 3-7](#) to [Table 3-10](#) on page 11, the messages are described in the ANTARIS®4 protocol specification  
2. Leave open

Both USART ports and the USB port accept input messages in all three supported protocols (NMEA, RTCM and UBX) at the configured baud rate. Input messages of all three protocols can be arbitrarily mixed. Response to a query input message will always use the same protocol as the query input message. The USB port does only accept NMEA and UBX as input protocol by default. RTCM can be enabled via protocol messages on demand.

In Auto Mode, no output message is sent out by default, but all input messages are accepted at any supported baud rate. Again, USB is restricted to only NMEA and UBX protocols. Response to query input commands will be given the same protocol and baud rate as it was used for the query command. Using the respective configuration commands, periodic output messages can be enabled.

The following message settings are used in the tables below:

**Table 3-7.** Supported Messages at Setting *Low*

|                  |          |             |
|------------------|----------|-------------|
| <b>NMEA Port</b> | Standard | GGA, RMC    |
| <b>UBX Port</b>  | NAV      | SOL, SVINFO |
|                  | MON      | EXCEPT      |

**Table 3-8.** Supported Messages at Setting *Medium*

|                  |          |   |
|------------------|----------|---|
| <b>NMEA Port</b> | Standard | GGA, RMC, GSA, GSV, GLL, VTG, ZDA   |
| <b>UBX Port</b>  | NAV      | SOL, SVINFO, POSECEF, POSLLH, STATUS, DOP, VELECEF, VELNED, TIMEGPS, TIMEUTC, CLOCK |
|                  | MON      | EXCEPT  |

**Table 3-9.** Supported Messages at Setting *High*

|                  |             |   |
|------------------|-------------|---|
| <b>NMEA Port</b> | Standard    | GGA, RMC, GSA, GSV, GLL, VTG, ZDA, GRS, GST   |
|                  | Proprietary | PUBX00, PUBX03, PUBX04  |
| <b>UBX Port</b>  | NAV         | SOL, SVINFO, POSECEF, POSLLH, STATUS, DOP, VELECEF, VELNED, TIMEGPS, TIMEUTC, CLOCK |
|                  | MON         | SCHD, IO, IPC, EXCEPT   |

**Table 3-10.** Supported Messages at Setting *Debug* (Additional Undocumented Message May be Part of Output Data)

|                  |             |   |
|------------------|-------------|---|
| <b>NMEA Port</b> | Standard    | GGA, RMC, GSA, GSV, GLL, VTG, ZDA, GRS, GST   |
|                  | Proprietary | PUBX00, PUBX03, PUBX04  |
| <b>UBX Port</b>  | NAV         | SOL, SVINFO, POSECEF, POSLLH, STATUS, DOP, VELECEF, VELNED, TIMEGPS, TIMEUTC, CLOCK |
|                  | MON         | SCHD, IO, IPC, EXCEPT   |
|                  | RXM         | RAW (RAW message support requires an additional license)                            |

The following settings apply if GPSMODE configuration is not enabled, that is, GPSMODE = 0 (ROM-Defaults):

**Table 3-11.** Serial I/O Default Setting if GPSMODE Configuration is Deselected (GPSMODE0 = 0)

|  | USB NMEA                     | USART1 NMEA                  | USART2 UBX                      |
|--|------------------------------|------------------------------|---------------------------------|
| Baud Rate (kBaud)                          |                              | 57.6                         | 57.6                            |
| Input Protocol                             | UBX, NMEA                    | UBX, NMEA, RTCM              | UBX, NMEA, RTCM                 |
| Output Protocol                            | NMEA                         | NMEA                         | UBX                             |
| Messages                                   | GGA, RMC, GSA, GSV           | GGA, RMC, GSA, GSV           | NAV: SOL, SVINFO<br>MON: EXCEPT |
| Information Messages (UBX INF or NMEA TXT) | User, Notice, Warning, Error | User, Notice, Warning, Error | User, Notice, Warning, Error    |

### 3.3.4 USB Power Mode

For correct response to the USB host queries, the device has to know its power mode. This is configured via GPSMODE7. If set to *bus powered*, an upper current limit of 100 mA is reported to the USB host; that is, the device classifies itself as a “low-power bus-powered function” with no more than one USB power unit load.

**Table 3-12.** USB Power Modes

| GPSMODE7 (Reset = PU) | Description  |
|-----------------------|--|
| 0                     | USB device is bus-powered (maximum current limit 100 mA) |
| 1 <sup>(1)</sup>      | USB device is self-powered (default ROM value)           |

Note: 1. Leave open

### 3.3.5 Active Antenna Supervisor

The two pins P0/NANTSHORT and P15/ANTON plus one pin of P25/NAADET0/MISO or P14/NAADET1 are always initialized as general purpose I/Os and used as follows:

- P15/ANTON is an output which can be used to switch on and off antenna power supply.
- Input P0/NANTSHORT will indicate an antenna short circuit, i.e. zero DC voltage at the antenna, to the firmware. If the antenna is switched off by output P15/ANTON, it is assumed that also input P0/NANTSHORT will signal zero DC voltage, i.e. switch to its active low state.
- Input P25/NAADET0/MISO or P14/NAADET1 will indicate a DC current into the antenna. In case of short circuit, both P0 and P25/P14 will be active, i.e. at low level. If the antenna is switched off by output P15/ANTON, it is assumed that also input P25/NAADET0/MISO will signal zero DC current, i.e. switch to its active low state. Which pin is used as NAADET (P14 or P25) depends on the settings of GPSMODE11 and GPSMODE10 (see [Table 3-14 on page 13](#)).

**Table 3-13.** Pin Usage of Active Antenna Supervisor

| Pin                                      | Usage     | Meaning  |
|--|-----------|--|
| P0/NANTSHORT                             | NANTSHORT | Active antenna short circuit detection<br>High = No antenna DC short circuit present<br>Low = Antenna DC short circuit present                 |
| P25/NAADDET0/<br>MISO or<br>P14/NAADDET1 | NAADDET   | Active antenna detection input<br>High = No active antenna present<br>Low = Active antenna is present  |
| P15/ANTON                                | ANTON     | Active antenna power on output<br>High = Power supply to active antenna is switched on<br>Low = Power supply to active antenna is switched off |

**Table 3-14.** Antenna Detection I/O Settings

| GPSMODE11<br>(Reset = PU) | GPSMODE10<br>(Reset = PU) | GPSMODE8<br>(Reset = PU) | Location of NAADET                  | Comment   |
|---------------------------|---------------------------|--------------------------|-------------------------------------|---|
| 0                         | 0                         | 0                        | P25/NAADDET0/MISO                   |   |
| 0                         | 0                         | 1 <sup>(1)</sup>         | P25/NAADDET0/MISO                   |   |
| 0                         | 1 <sup>(1)</sup>          | 0                        | P14/NAADDET1                        | Reserved for further use.<br>Do not use this setting. |
| 0                         | 1 <sup>(1)</sup>          | 1 <sup>(1)</sup>         | P14/NAADDET1<br>(Default ROM value) |   |
| 1 <sup>(1)</sup>          | 0                         | 0                        | P14/NAADDET1                        | Reserved for further use.<br>Do not use this setting. |
| 1 <sup>(1)</sup>          | 0                         | 1 <sup>(1)</sup>         | P14/NAADDET1                        | Reserved for further use.<br>Do not use this setting. |
| 1 <sup>(1)</sup>          | 1 <sup>(1)</sup>          | 0                        | P25/NAADDET0/MISO                   |   |
| 1 <sup>(1)</sup>          | 1 <sup>(1)</sup>          | 1 <sup>(1)</sup>         | P25/NAADDET0/MISO                   |   |

Note: 1. Leave open

The Antenna Supervisor Software will be configured as follows:

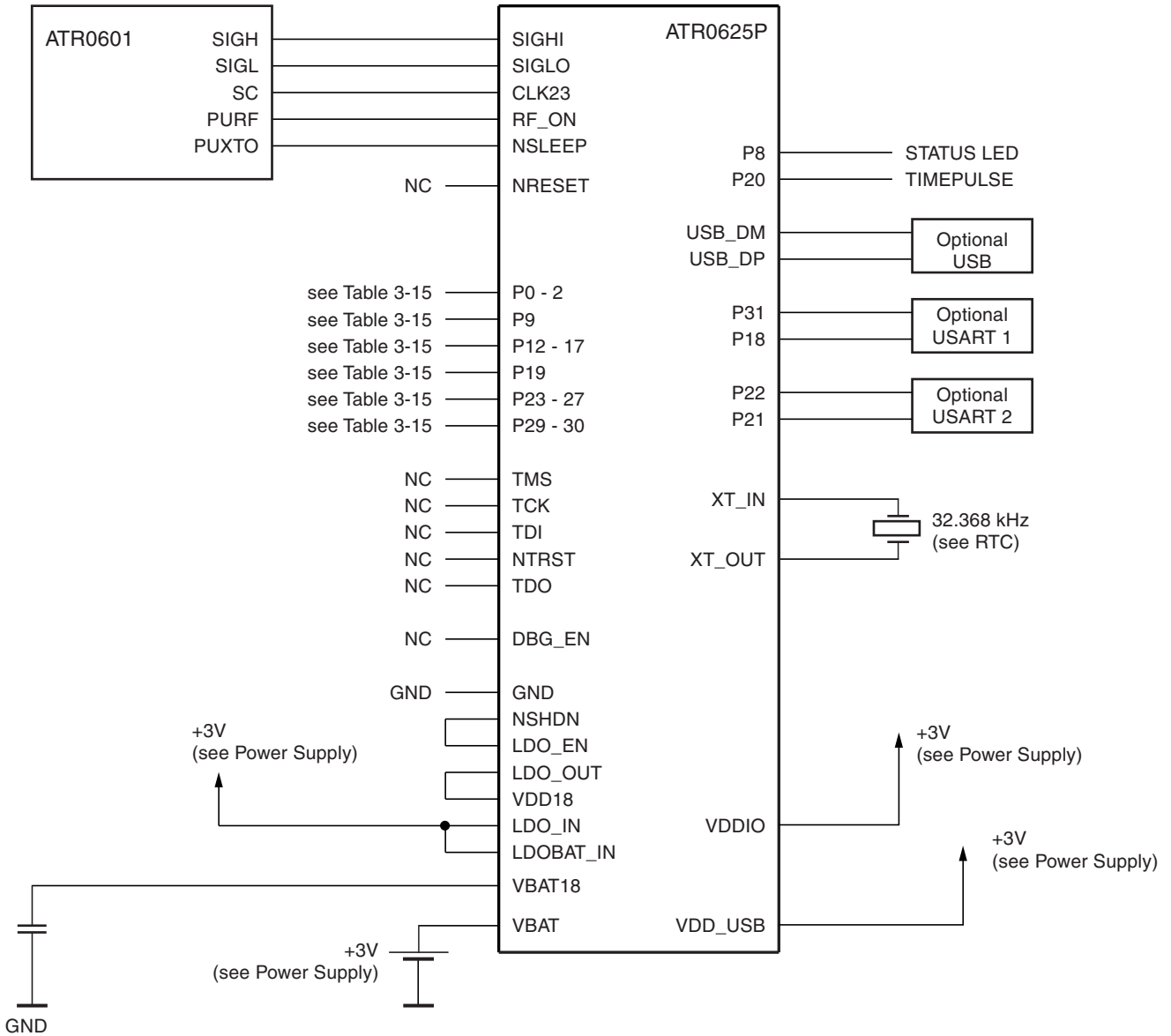
1. Enable Control Signal
2. Enable Short Circuit Detection (power down antenna via ANTON if short is detected via NANTSHORT)
3. Enable Open Circuit Detection via NAADET

The antenna supervisor function may not be disabled by GPSMODE pin selection.

If the antenna supervisor function is not used, please leave open ANTON, NANTSHORT and NAADET.

### 3.4 External Connections for a Working GPS System

Figure 3-2. Example of an External Connection



NC: Not connected

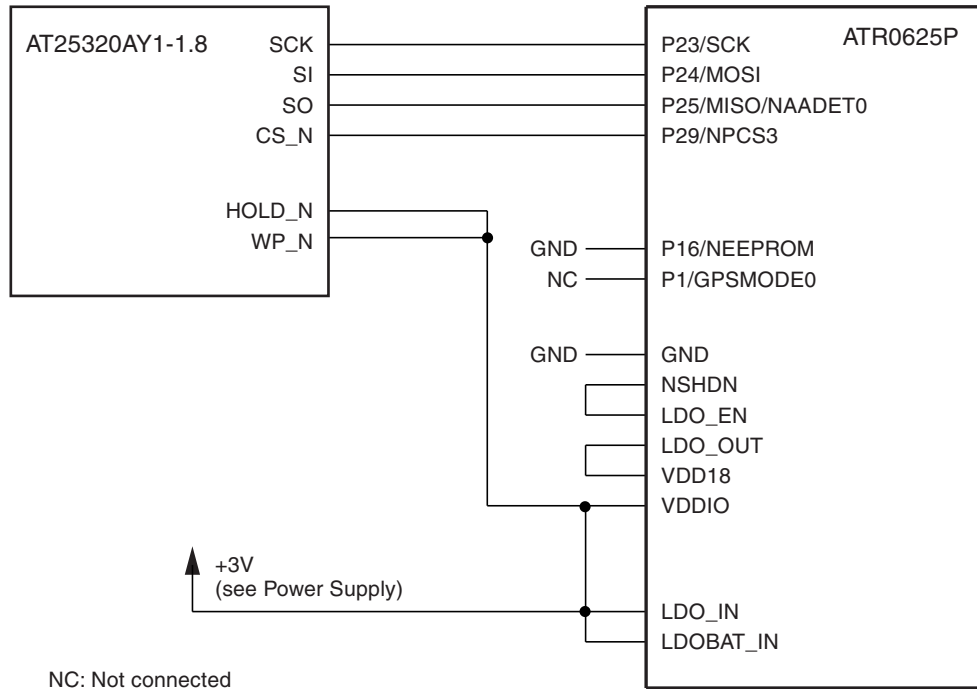
**Table 3-15.** Recommended Pin Connection

| Pin Name                | Recommended External Circuit   |
|-------------------------|--|
| P0/NANTSHORT            | Internal pull-down resistor, leave open if Antenna Supervision functionality is unused.  |
| P1/GPSMODE0             | Internal pull-down resistor, leave open, in order to disable the GPSMODE pin configuration feature. Connect to VDD18 to enable the GPSMODE pin configuration feature. Refer to GPSMODE definitions in section <a href="#">“Setting GPSMODE0 to GPSMODE12” on page 9.</a> |
| P2/BOOT_MODE            | Internal pull-down resistor, leave open.   |
| P8/STATUSLED            | Output in default ROM firmware: leave open if not used   |
| P9/EXTINT0              | Internal pull-up resistor, leave open if unused.   |
| P12/GPSMODE2/NPCS2      | Internal pull-up resistor, can be left open if the GPSMODE feature is not used. Refer to GPSMODE definitions in section <a href="#">“Setting GPSMODE0 to GPSMODE12” on page 9.</a>   |
| P13/GPSMODE3/EXTINT1    | Internal pull-up resistor, can be left open if the GPSMODE feature is not used. Refer to GPSMODE definitions in section <a href="#">“Setting GPSMODE0 to GPSMODE12” on page 9.</a>   |
| P14/NAADET1             | Internal pull-down resistor, leave open if Antenna Supervision functionality is unused.  |
| P15/ANTON               | Internal pull-down resistor, leave open if Antenna Supervision functionality is unused.  |
| P16/NEEPROM             | Internal pull-up resistor, leave open if no serial EEPROM is connected. Otherwise connect to GND.  |
| P17/GPSMODE5/SCK1       | Internal pull-down resistor, can be left open if the GPSMODE feature is not used. Refer to GPSMODE definitions in section <a href="#">“Setting GPSMODE0 to GPSMODE12” on page 9.</a>   |
| P18/TXD1                | Output in default ROM firmware: leave open if serial interface is not used.  |
| P19/GPSMODE6/SIGLO1     | Internal pull-up resistor, can be left open if the GPSMODE feature is not used. Refer to GPSMODE definitions in section <a href="#">“Setting GPSMODE0 to GPSMODE12” on page 9.</a>   |
| P20/TIMEPULSE/SCK2      | Output in default ROM firmware: leave open if timepulse feature is not used.   |
| P21/TXD2                | Output in default ROM firmware: leave open if serial interface not used.   |
| P22/RXD2                | Internal pull-up resistor, leave open if serial interface is not used.   |
| P23/GPSMODE7/SCK        | Internal pull-up resistor, can be left open if the GPSMODE feature is not used. Refer to GPSMODE definitions in section <a href="#">“Setting GPSMODE0 to GPSMODE12” on page 9.</a>   |
| P24/GPSMODE8/MOSI       | Internal pull-up resistor, can be left open if the GPSMODE feature is not used. Refer to GPSMODE definitions in section <a href="#">“Setting GPSMODE0 to GPSMODE12” on page 9.</a>   |
| P25/NAADET0/MISO        | Internal pull-down resistor, leave open if Antenna Supervision functionality is unused.  |
| P26/GPSMODE10/NSS/NPCS0 | Internal pull-up resistor, can be left open if the GPSMODE feature is not used. Refer to GPSMODE definitions in section <a href="#">“Setting GPSMODE0 to GPSMODE12” on page 9.</a>   |
| P27/GPSMODE11/NPCS1     | Internal pull-up resistor, can be left open if the GPSMODE feature is not used. Refer to GPSMODE definitions in section <a href="#">“Setting GPSMODE0 to GPSMODE12” on page 9.</a>   |
| P29/GPSMODE12/NPCS3     | Internal pull-up resistor, can be left open if the GPSMODE feature is not used. Refer to GPSMODE definitions in section <a href="#">“Setting GPSMODE0 to GPSMODE12” on page 9.</a>   |
| P30/AGCOUT0             | Internal pull-down resistor, leave open.   |
| P31/RXD1                | Internal pull-up resistor, leave open if serial interface is not used.   |

### 3.4.1 Connecting an Optional Serial EEPROM

The ATR0625P offers the possibility to connect an external serial EEPROM. The internal ROM firmware supports to store the configuration of the ATR0625P in serial EEPROM. The pin P16/NEEPROM signals the firmware that a serial EEPROM is connected with the ATR0625P. The 32-bit RISC processor of the ATR0625P accesses the external memory with SPI (Serial Peripheral Interface). Atmel recommend to use 32 Kbit 1.8V serial EEPROM, e.g. the Atmel AT25320AY1-1.8. [Figure 3-3](#) shows an example of the serial EEPROM connection.

**Figure 3-3.** Example of a Serial EEPROM Connection



Note: The GPSMODE pin configuration feature can be disabled, because the configuration can be stored in the serial EEPROM. VDDIO is the supply voltage for the pins: P23, P24, P25 and P29.



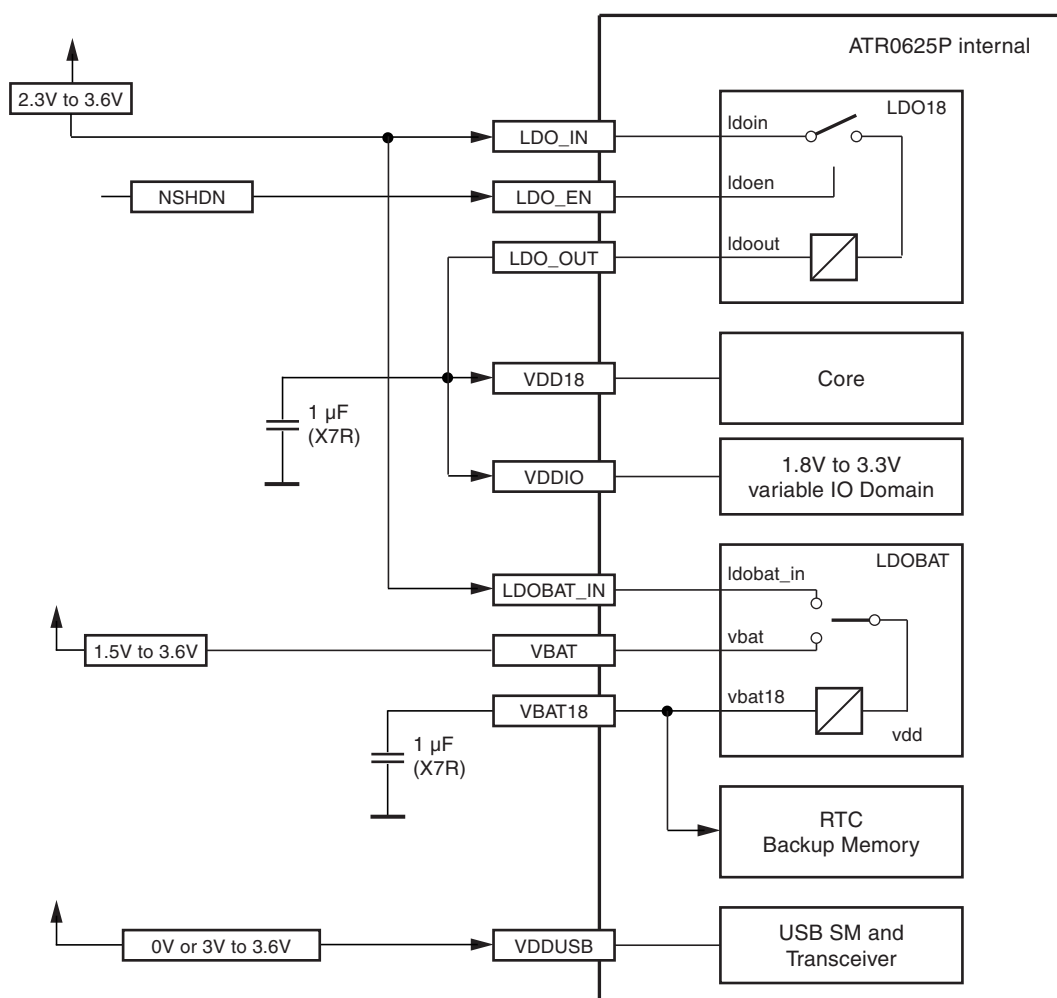
## 4. Power Supply

The baseband IC is supplied with four distinct supply voltages:

- VDD18, the nominal 1.8V supply voltage for the core, the RF-I/O pins, the memory interface and the test pins and all GPIO-pins not mentioned in next item.
- VDDIO, the variable supply voltage within 1.8V to 3.6V for following GPIO-pins: P1, P2, P8, P12, P14, P16, P17, P18, P19, P20, P21, P23, P24, P25, P26, P27 and P29 In input mode, these pins are 5V input tolerant.
- VDD\_USB, the power supply of the USB pins: USB\_DM and USB\_DP.
- VBAT18 to supply the backup domain: RTC, backup SRAM and the pins NSLEEP, NSHDN, LDO\_EN, VBAT18, P9/EXTIN0, P13/EXTINT1, P22/RXD2 and P31/RXD1 and the 32kHz oscillator. In input mode, the four GPIO-pins are 5V input tolerant.

Figure 4-1, Figure 4-2, and Figure 4-3 show examples of the wiring of ATR0625P power supply.

**Figure 4-1.** External Wiring Example Using Internal LDOs and Backup Power Supply



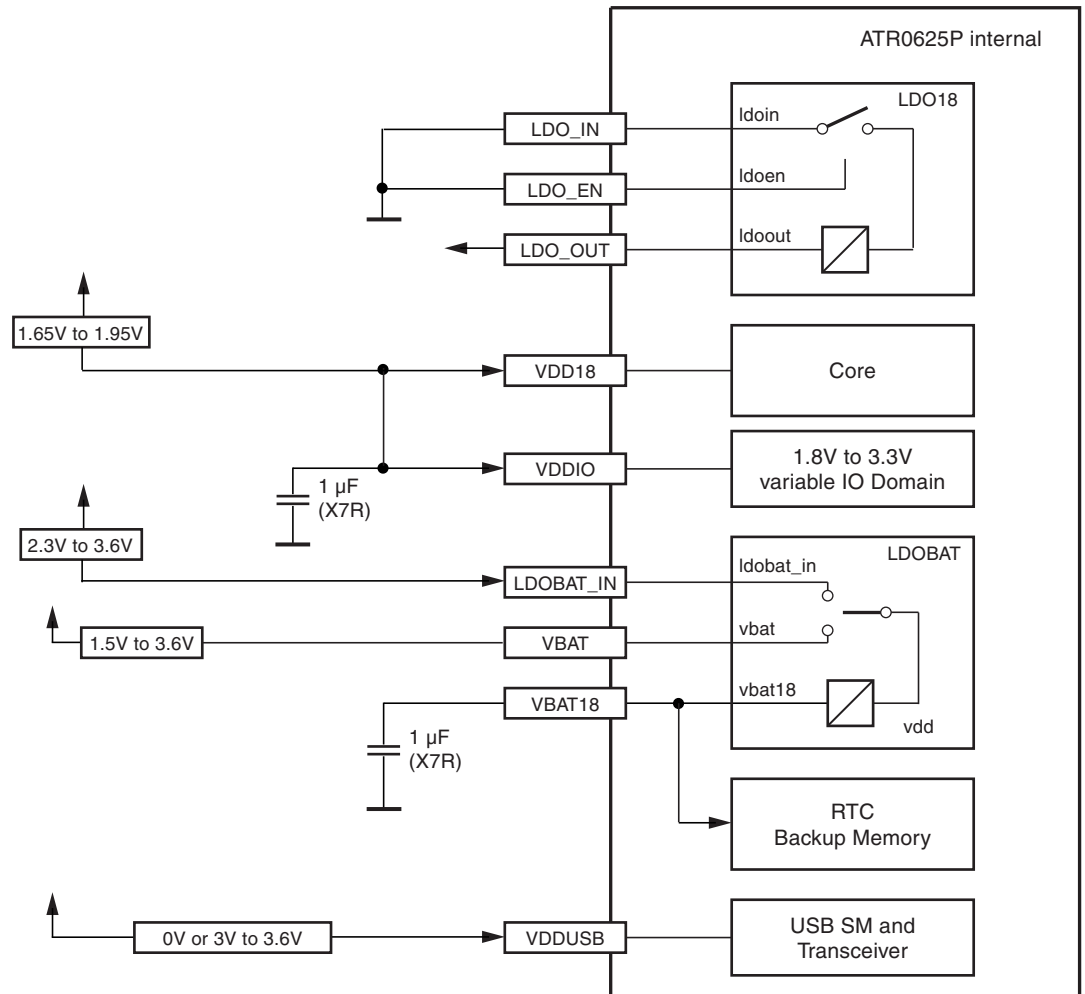
The baseband IC contains a built in low dropout voltage regulator LDO18. This regulator can be used if the host system does not provide the core voltage VDD18 of 1.8V nominal. In such case, LDO18 will provide a 1.8V supply voltage from any input voltage VDD between 2.3V and 3.6V. The LDO\_EN input can be used to shut down VDD18 if the system is in standby mode.

If the host system does however supply a 1.8V core voltage directly, this voltage has to be connected to the VDD18 supply pins of the baseband IC. LDO\_EN must be connected to GND. LDO\_IN can be connected to GND. LDO\_OUT must not be connected.

A second built in low dropout voltage regulator LDOBAT provides the supply voltage for the RTC and backup SRAM from any input voltage LDOBAT\_IN between 2.3V and 3.6V or from VBAT between 1.5V and 3.6V. The backup battery connected to VBAT is only discharged if the supply connected to LDOBAT\_IN is shut-down.

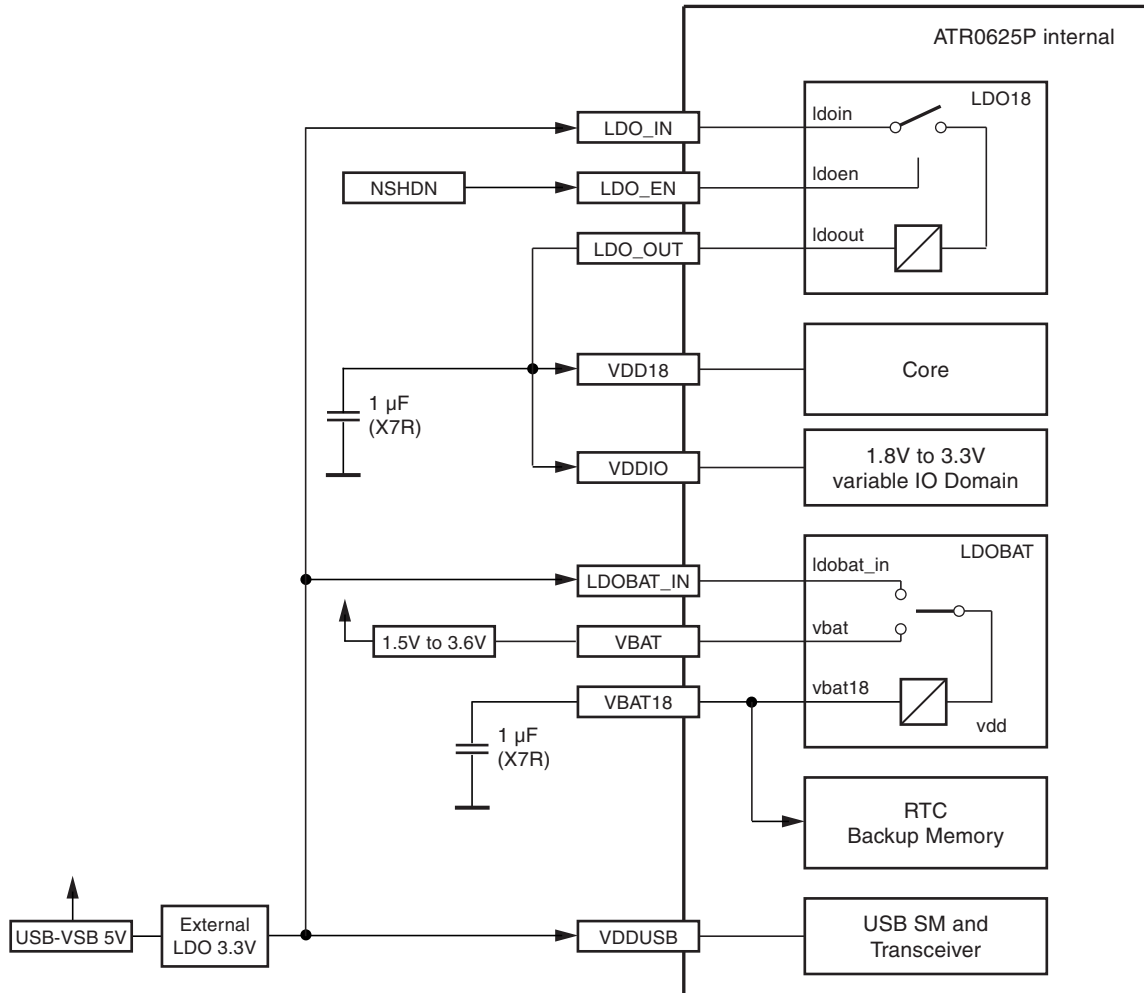
Only after VDD18 has been supplied to ATR0625P the RTC section will be initialized properly. If only VBAT is applied first, the current consumption of the RTC and backup SRAM is undetermined.

**Figure 4-2.** External Wiring Example Using 1.8V from Host System and Backup Power Supply



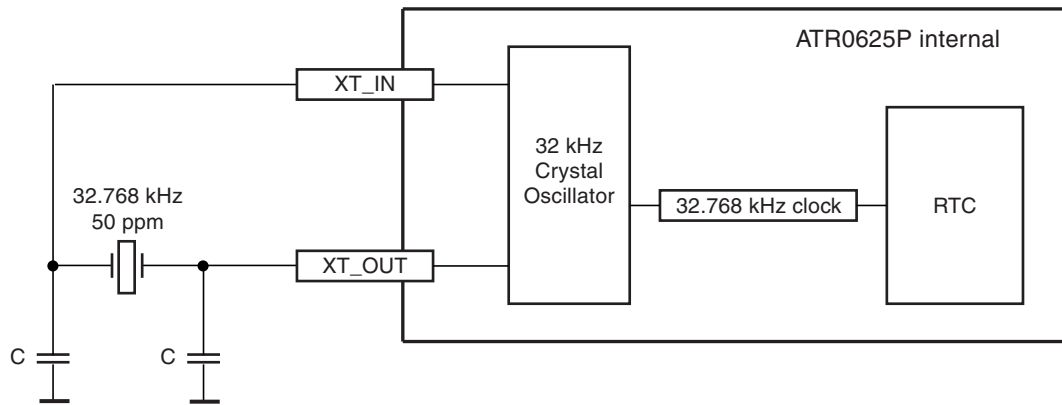
The USB Transceiver is disabled if VDD\_USB < 2.0V. In this case the pins USB\_DM and USB\_DP are connected to GND (internal pull-down resistors). The USB Transceiver is enabled if VDD\_USB within 3.0V and 3.6V.

**Figure 4-3.** External Wiring Example Using Internal LDOs, USB Supply Voltage and Backup Power Supply



## 5. Oscillator

Figure 5-1. Crystal Connection



$C = 2 \times C_{load}$ ,  $C_{load}$  can be derived from the crystal datasheet. Maximum value for C is 25 pF.

## 6. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Parameters                           | Pin  | Symbol | Min. | Max.  | Unit |
|--------------------------------------|--|--------|------|-------|------|
| Operating free air temperature range |  |        | -40  | +85   | °C   |
| Storage temperature                  |  |        | -60  | +150  | °C   |
| DC supply voltage                    | VDD18  |        | -0.3 | +1.95 | V    |
|                                      | VDDIO  |        | -0.3 | +3.6  | V    |
|                                      | VDD_USB  |        | -0.3 | +3.6  | V    |
|                                      | LDO_IN   |        | -0.3 | +3.6  | V    |
|                                      | LDOBAT_IN  |        | -0.3 | +3.6  | V    |
|                                      | VBAT   |        | -0.3 | +3.6  | V    |
| DC input voltage                     | P0, P15, P30, SIGHI, SIGLO, CLK23, XT_IN, TMS, TCK, TDI, NTRST, DBG_EN, LDO_EN, NRESET |        | -0.3 | +1.95 | V    |
|                                      | USB_DM, USB_DP   |        | -0.3 | +3.6  | V    |
|                                      | P1, P2, P8, P9, P12 to P14, P16 to P27, P29, P31                                       |        | -0.3 | +5.0  | V    |

Note: Minimum/maximum limits are at +25°C ambient temperature, unless otherwise specified

## 7. Thermal Resistance

| Parameters                               | Symbol     | Value | Unit |
|--|------------|-------|------|
| Junction ambient, according to JEDEC51-5 | $R_{thJA}$ | 24.2  | K/W  |

## 8. Electrical Characteristics

If no additional information is given in column Test Conditions, the values apply to a temperature range from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

| No.  | Parameters                                     | Test Conditions  | Pin               | Symbol           | Min.                      | Typ.    | Max.                      | Unit | Type* |
|------|--|--|-------------------|------------------|---------------------------|---------|---------------------------|------|-------|
| 1.1  | DC supply voltage core                         |  | VDD18             | VDD18            | 1.65                      | 1.8     | 1.95                      | V    | D     |
| 1.2  | DC supply voltage VDDIO domain <sup>(1)</sup>  |  | VDDIO             | VDDIO            | 1.65                      | 1.8/3.3 | 3.6                       | V    | D     |
| 1.3  | DC supply voltage USB <sup>(2)</sup>           |  | VDD_USB           | VDDUSB           | 3.0                       | 3.3     | 3.6                       | V    | D     |
| 1.4  | DC supply voltage backup domain <sup>(3)</sup> |  | VBAT18            | VBAT18           | 1.65                      | 1.8     | 1.95                      | V    | D     |
| 1.5  | DC output voltage VDD18                        |  |                   | $V_{O,18}$       | 0                         |         | VDD18                     | V    | D     |
| 1.6  | DC output voltage VDDIO                        |  |                   | $V_{O,IO}$       | 0                         |         | VDDIO                     | V    | D     |
| 1.7  | Low-level input voltage VDD18 domain           | VDD18 = 1.65V to 1.95V   |                   | $V_{IL,18}$      | -0.3                      |         | $0.3 \times \text{VDD18}$ | V    | C     |
| 1.8  | High-level input voltage VDD18 domain          | VDD18 = 1.65V to 1.95V   |                   | $V_{IH,18}$      | $0.7 \times \text{VDD18}$ |         | $\text{VDD18} + 0.3$      | V    | C     |
| 1.9  | Schmitt trigger threshold rising               | VDD18 = 1.65V to 1.95V   | CLK23             | $V_{th+,CLK23}$  |                           |         | $0.7 \times \text{VDD18}$ | V    | C     |
| 1.10 | Schmitt trigger threshold falling              | VDD18 = 1.65V to 1.95V   | CLK23             | $V_{th-,CLK23}$  | $0.3 \times \text{VDD18}$ |         |                           | V    | C     |
| 1.11 | Schmitt trigger hysteresis                     | VDD18 = 1.65V to 1.95V   | CLK23             | $V_{hyst,CLK23}$ | 0.2                       |         | 0.55                      | V    | C     |
| 1.12 | Schmitt trigger threshold rising               | VDD18 = 1.65V to 1.95V   | NRESET            | $V_{th+,NRESET}$ | 0.8                       |         | 1.3                       | V    | C     |
| 1.13 | Schmitt trigger threshold falling              | VDD18 = 1.65V to 1.95V   | NRESET            | $V_{th-,NRESET}$ | 0.46                      |         | 0.77                      | V    | C     |
| 1.14 | Low-level input voltage VDDIO domain           | VDDIO = 1.65V to 3.6V  |                   | $V_{IL,IO}$      | -0.3                      |         | +0.41                     | V    | C     |
| 1.15 | High-level input voltage VDDIO domain          | VDDIO = 1.65V to 3.6V  |                   | $V_{IH,IO}$      | 1.46                      |         | 5.0                       | V    | C     |
| 1.16 | Low-level input voltage VBAT18 domain          | VBAT18 = 1.65V to 1.95V  | P9, P13, P22, P31 | $V_{IL,BAT}$     | -0.3                      |         | +0.41                     | V    | C     |
| 1.17 | High-level input voltage VBAT18 domain         | VBAT18 = 1.65V to 1.95V  | P9, P13, P22, P31 | $V_{IH,BAT}$     | 1.46                      |         | 5.0                       | V    | C     |
| 1.18 | Low-level input voltage USB                    | VDD_USB = 3.0V to 3.6V, 39 $\Omega$ source resistance + 27 $\Omega$ external series resistor | DP, DM            | $V_{IL,USB}$     | -0.3                      |         | +0.8                      | V    | C     |
| 1.19 | High-level input voltage USB                   | VDD_USB = 3.0V to 3.6V   | DP, DM            | $V_{IH,USB}$     | 2.0                       |         | 4.6                       | V    | C     |
| 1.20 | Low-level output voltage VDD18 domain          | $I_{OL} = 1.5 \text{ mA}$ , VDD18 = 1.65V  |                   | $V_{OL,18}$      |                           |         | 0.4                       | V    | A     |
| 1.21 | High-level output voltage VDD18 domain         | $I_{OH} = -1.5 \text{ mA}$ , VDD18 = 1.65V   |                   | $V_{OH,18}$      | VDD18 - 0.45              |         |                           | V    | A     |
| 1.22 | Low-level output voltage VDDIO domain          | $I_{OL} = 1.5 \text{ mA}$ , VDDIO = 3.0V   |                   | $V_{OL,IO}$      |                           |         | 0.4                       | V    | A     |

- Notes:
1. VDDIO is the supply voltage for the following GPIO pins: P1, P2, P8, P12, P14, P16, P17, P18, P19, P20, P21, P23, P24, P25, P26, P27 and P29
  2. Values defined for operating the USB interface. Otherwise VDD\_USB may be connected to ground
  3. Supply voltage VBAT18 for backup domain is generated internally by the LDOBAT

## 8. Electrical Characteristics (Continued)

If no additional information is given in column Test Conditions, the values apply to a temperature range from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

| No.  | Parameters  | Test Conditions  | Pin   | Symbol       | Min.        | Typ. | Max.  | Unit          | Type* |
|------|---|--|---|--------------|-------------|------|-------|---------------|-------|
| 1.23 | High-level output voltage VDDIO domain                | $I_{OH} = -1.5\text{ mA}$ , VDDIO = 3.0V   |   | $V_{OH,IO}$  | VDDIO - 0.5 |      |       | V             | A     |
| 1.24 | Low-level output voltage VBAT18 domain                | $I_{OL} = 1\text{ mA}$   | P9, P13, P22, P31                             | $V_{OL,BAT}$ |             |      | 0.4   | V             | A     |
| 1.25 | High-level output voltage VBAT18 domain               | $I_{OH} = -1\text{ mA}$  | P9, P13, P22, P31                             | $V_{OH,BAT}$ | 1.2         |      |       | V             | A     |
| 1.26 | Low-level output voltage USB                          | $I_{OL} = 2.2\text{ mA}$ , VDD_USB = 3.0V to 3.6V, 27 $\Omega$ external series resistor  | DP, DM  | $V_{OL,USB}$ |             |      | 0.3   | V             | A     |
| 1.27 | High-level output voltage USB                         | $I_{OH} = -0.2\text{ mA}$ , VDD_USB = 3.0V to 3.6V, 27 $\Omega$ external series resistor | DP, DM  | $V_{OH,USB}$ | 2.8         |      |       | V             | A     |
| 1.28 | Input-leakage current (standard inputs and I/Os)      | VDD18 = 1.95V<br>$V_{IL} = 0V$   |   | $I_{LEAK}$   | -1          |      | +1    | $\mu\text{A}$ | C     |
| 1.29 | Input capacitance                                     |  |   | $I_{CAP}$    |             |      | 10    | pF            | D     |
| 1.30 | Input pull-up resistor                                |  | NRESET  | $R_{PU}$     | 0.7         |      | 1.8   | k $\Omega$    | C     |
| 1.31 | Input pull-up resistor                                |  | TCK, TDI, TMS                                 | $R_{PU}$     | 7           |      | 18    | k $\Omega$    | C     |
| 1.32 | Input pull-up resistor                                |  | P9, P13, P22, P31                             | $R_{PU}$     | 100         |      | 235   | k $\Omega$    | C     |
| 1.33 | Input pull-down resistor                              |  | DBG_EN, NTRST,                                | $R_{PD}$     | 7           |      | 18    | k $\Omega$    | C     |
| 1.34 | Input pull-down resistor                              |  | P0, P15, P30                                  | $R_{PD}$     | 100         |      | 235   | k $\Omega$    | C     |
| 1.35 | Configurable input pull-up resistor                   | VDDIO = 3.6V<br>$V_{PAD} = 0V$   | P1, P2, P8, P12, P14, P[16-21], P[23-27], P29 | $R_{CPU}$    | 50          |      | 160   | k $\Omega$    | C     |
| 1.36 | Configurable input pull-down resistor                 | VDDIO = 3.6V<br>$V_{PAD} = 3.6V$   | P1, P2, P8, P12, P14, P[16-21], P[23-27], P29 | $R_{CPD}$    | 40          |      | 160   | k $\Omega$    | C     |
| 1.37 | Configurable input pull-up resistor (Idle state)      |  | USB_DP  | $R_{CPU}$    | 0.9         |      | 1.575 | k $\Omega$    | C     |
| 1.38 | Configurable input pull-up resistor (operation state) |  | USB_DP  | $R_{CPU}$    | 1.425       |      | 3.09  | k $\Omega$    | C     |
| 1.39 | Input pull-down resistor                              |  | USB_DP<br>USB_DM                              | $R_{PD}$     | 10          |      | 500   | k $\Omega$    | C     |

- Notes:
1. VDDIO is the supply voltage for the following GPIO pins: P1, P2, P8, P12, P14, P16, P17, P18, P19, P20, P21, P23, P24, P25, P26, P27 and P29
  2. Values defined for operating the USB interface. Otherwise VDD\_USB may be connected to ground
  3. Supply voltage VBAT18 for backup domain is generated internally by the LDOBAT

## 9. Power Consumption

**Table 9-1.** Core Power Consumption

| Mode     | Conditions  | Typ.  | Unit | Type* |
|----------|---|-------|------|-------|
| Sleep    | At 1.8V, no CLK23   | 0.065 | mA   | C     |
| Shutdown | RTC, backup SRAM and LDOBAT   | 0.007 |      | C     |
| Normal   | Satellite acquisition   | 25    |      | C     |
|          | Normal tracking on 6 channels with 1 fix/s; each additional active tracking channel adds 0.5 mA | 14    |      | C     |
|          | All channels disabled   | 11    |      | C     |

\*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

## 10. ESD Sensitivity

The ATR0625P is an ESD sensitive device. The current ESD values are to be defined.

Observe precautions for handling.

**Table 10-1.** ESD- Sensitivity

| Test Model             | Max. | Unit |
|------------------------|------|------|
| Human Body Model (HBM) | TBD  | V    |

## 11. LDO18

The LDO18 is a built in low dropout voltage regulator which can be used if the host system does not provide the core voltage VDD18.

**Table 11-1.** Electrical Characteristics of LDO18

| Parameter                | Conditions                                     | Min. | Typ. | Max. | Unit | Type* |
|--------------------------|--|------|------|------|------|-------|
| Supply voltage LDO_IN    |  | 2.3  |      | 3.6  | V    | D     |
| Output voltage (LDO_OUT) |  | 1.65 | 1.8  | 1.95 | V    | A     |
| Output current (LDO_OUT) |  |      |      | 30   | mA   | A     |
| Current consumption      | After startup, no load, at room temperature    |      |      | 80   | µA   | A     |
| Current consumption      | Standby mode (LDO_EN = 0), at room temperature |      | 1    | 5    | µA   | A     |

\*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

For well defined start-up of LDO18, LDO\_IN needs to be connected to LDOBAT\_IN.

## 12. LDOBAT and Backup Domain

The LDOBAT is a built in low dropout voltage regulator which provides the supply voltage VBAT18 for the RTC, backup SRAM, P9, P13, P22, P31, NSLEEP and NSHDN. The LDOBAT voltage regulator switches in battery mode if LDOBAT\_IN falls below 1.5V.

**Table 12-1.** Electrical Characteristics of LDOBAT

| Parameter                                    | Conditions  | Min. | Typ. | Max. | Unit | Type* |
|--|---|------|------|------|------|-------|
| Supply voltage LDOBAT_IN                     |   | 2.3  |      | 3.6  | V    | D     |
| Supply voltage VBAT                          |   | 1.5  |      | 3.6  | V    | D     |
| Output voltage (VBAT18)                      | If switch connects to LDOBAT_IN.                                    | 1.65 | 1.8  | 1.95 | V    | A     |
| Output current (VBAT18)                      | No external load allowed  |      |      | 1.5  | mA   | D     |
| Current consumption LDOBAT_IN <sup>(1)</sup> | After startup (sleep/backup mode), at room temperature              |      |      | 15   | μA   | A     |
| Current consumption VBAT <sup>(1)</sup>      | After startup (backup mode and LDOBAT_IN = 0V), at room temperature |      |      | 10   | μA   | A     |
| Current consumption                          | After startup (normal mode), at room temperature                    |      |      | 1.5  | mA   | C     |

\*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. If no current is caused by outputs (pad output current as well as current across internal pull-up resistors)



### 13. Ordering Information

| Extended Type Number | Package | MPQ  | Remarks  |
|----------------------|---------|------|--|
| ATR0625P-PYQW        | QFN56   | 2000 | 8 mm × 8 mm, 0.50 mm pitch, RoHS-compliant, green    |
| ATR0625-EK1          | -       | 1    | Evaluation kit/Road test kit                         |
| ATR0625-DK1          | -       | 1    | Development kit including example design information |

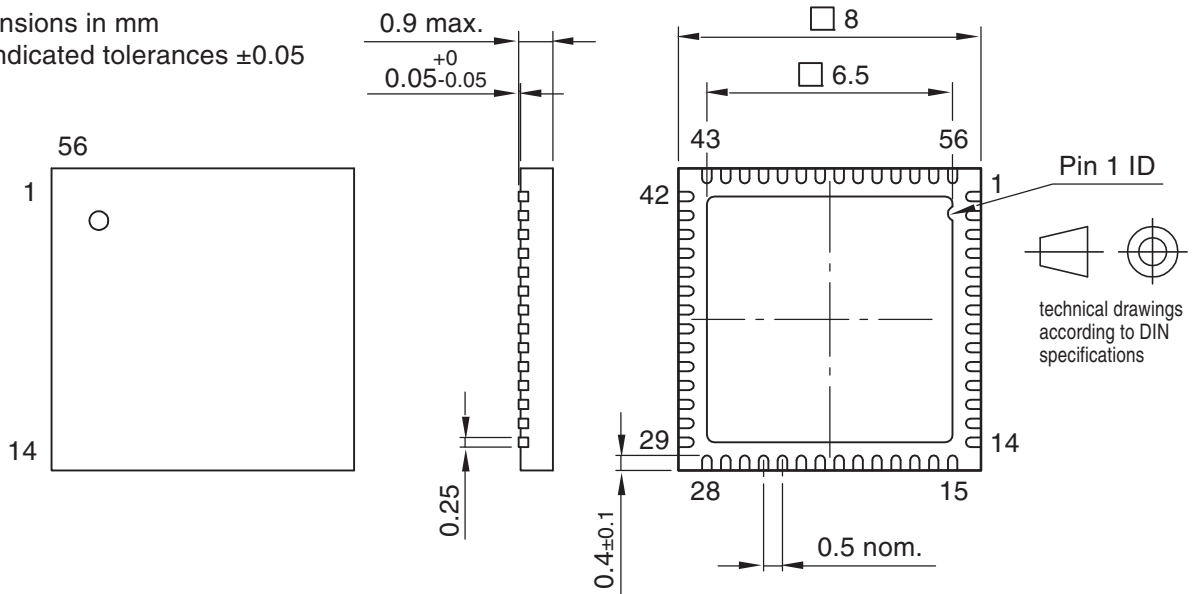
### 14. Package QFN56

Package: QFN56 8 x 8

Exposed pad 6.5 x 6.5

Dimensions in mm

Not indicated tolerances ±0.05



Drawing-No.: 6.543-5121.01-4

Issue: 1; 02.09.05

Moisture sensitivity level (MSL) = 3

## 15. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, and not to this document.

| Revision No.    | History   |
|-----------------|---|
| 4925G-GPS-05/08 | <ul style="list-style-type: none"> <li>• Table 3-1 “ATR0625P Pinout” on page 5: Pin type of pin CLK23 changed</li> <li>• Section 8 “Electrical Characteristics” numbers 1.11, 1.34 and 1.35 on pages 21 to 22 changed</li> <li>• Table 11-1 ““Electrical Characteristics of LDO18” on page 23 changed</li> </ul>  |
| 4925F-GPS-09/07 | <ul style="list-style-type: none"> <li>• Table 3-1 “ATR0625P Pinout” on page 5: Pin type of pin CLK23 changed</li> </ul>  |
| 4925E-GPS-06/07 | <ul style="list-style-type: none"> <li>• Section 8 “Table Electrical Characteristics” numbers 1.35 and 1.36 on page 22 changed</li> </ul>   |
| 4925D-GPS-12/06 | <ul style="list-style-type: none"> <li>• All pages: Part number changed in ATR0625P</li> <li>• Page 20: Abs. Max. Ratings table: some changes</li> <li>• Page 21-22: El. Characteristics table: Type column added</li> <li>• Page 23: Power Consumption table: Type column added</li> <li>• Page 23: ESD Sensitivity table: Type column added</li> <li>• Page 23: LDO18 table: Type column added</li> <li>• Page 24: LDOBAT and Backup Domain table: Type column added</li> </ul> |
| 4925C-GPS-10/06 | <ul style="list-style-type: none"> <li>• Section 7 “Thermal Resistance” on page 20 added</li> <li>• Section 13 “Ordering Information” on page 25 changed</li> </ul>   |



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